Curriculum Vitae
SARAJU P. MOHANTY

CONTACT INFORMATION

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RESEARCH INTERESTS

My research is in Smart Electronic Systems which can be classified to the following inter-related categories:

(1) Consumer Electronics for Smart Cities
(2) Application-Specific Things for Efficient Edge Computing
(3) Methodologies for Digital and Mixed-Signal Hardware

PROFESSIONAL PREPARATION

Institutes	Major	Degree	Year
University of South Florida Tampa, USA	Computer Science and Engineering *Dissertation*: Energy and Transient Power Minimization During Behavioral Synthesis. *Advisor*: Prof. N. Ranganathan.	Ph.D.	2003
Indian Institute of Science Bangalore, India	Systems Science and Automation *Thesis*: Watermarking of Digital Images. *Advisor*: Prof. K. R. Ramakrishnan.	M.E.	1999
Orissa University of Agriculture & Tech. Bhubaneswar, India	Electrical Engineering *Project*: Study of the Effects of High-Voltage on Communications & Biological Systems. *Advisor*: Prof. B. Sahu.	B.Tech. (Honors)	1995

APPOINTMENTS

Year	Position	Institutes
June 2015 - Present	Professor	Computer Science & Engineering, Univ. of North Texas
April 2015 - Aug 2017	Technical Consultant	Chen Malin LLP, Dallas, TX 75201.
June 2010 - May 2015	Associate Professor	Computer Science & Engineering, Univ. of North Texas
Sep 2004 - May 2010	Assistant Professor	Computer Science & Engineering, Univ. of North Texas
Jan 2000 - Dec 2003	Instructor / TA	Computer Science & Engineering, Univ. of South Florida
Aug 1996 - Apr 1997	Trainee Manager	Orissa Mining Corporation, India
Aug 1995 - July 1996	Lecturer	Orissa Univ. of Agriculture and Technology, Bhubaneswar

AWARDS and HONORS

1. Glorious India Award - Rich and Famous NRIs of America for exemplary contributions to the discipline in 2017.
2. Society for Technical Communication (STC) Award of Merit for outstanding contributions to the IEEE Consumer Electronics Magazine (CEM) in 2017.
3. IEEE Distinguished Lecturer by the Consumer Electronics Society (CESoc), 2017–2018.
4. IEEE Consumer Electronics Magazine Best Paper Award for the year 2016.
5. Best Poster Award (First place with a cash prize of $1000) at the 30th IEEE MetroCon Conference, 2017.
6. Best Poster Award (Second place with a cash prize of $500) at the 30th IEEE MetroCon Conference, 2017.
7. The PROSE Award for best Textbook in Physical Sciences & Mathematics from the Association of American Publishers (AAP) in 2016.
8. The UNT Toulouse Scholars Award for outstanding scholarship and teaching achievements in 2016-2017.
9. Editor-in-Chief (EiC), IEEE Consumer Electronics Magazine, 2016–Present.
10. Editor-in-Chief (EiC), IEEE-CS-TCVLSI VLSI Circuits and Systems Letter (VCAL), 2015–Present.
11. Chair of the IEEE-CS Technical Committee on Very Large Scale Integration (TCVLSI), 2014–Present.
12. Distinguished Alumnus Award from the Government College of Engineering and Technology, Bhubaneswar, India in 2016.
13. Best Ph.D. Forum Paper Award at the 14th IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2015.
14. President's Scout Award by the Honorable President of India for Social Work in 1988.
15. Governor's Scout Award by the Honorable Governor of Orissa for Social Work in 1988.
16. UNT Provost's Thank a Teacher Recognition in 2016, 2015, 2014.
17. UNT Honors Day Recognition as Inspirational Faculty in 2016, 2014, 2012, 2011, 2009, 2008.
18. Elected to the grade of Senior Member of ACM in 2010.
19. Elected to the grade of Senior Member of IEEE in 2008.
20. Listed in:
    (a) Marquis Who's Who in American Education: 7th Edition 2005.
    (b) Marquis Who's Who of Emerging Leaders: 1st Edition 2006.
    (c) Marquis Who's Who in Science and Engineering: 9th Edition 2006 and 10th Edition 2007.
    (d) Marquis Who's Who in America: 60th Edition 2005, 61st Edition 2006, and 64th Edition 2009.
21. Computing Research Association (CRA) funding Award for Academic Career Workshop 2004.
22. USF Provost's Certificate of Recognition for outstanding performance as a Teaching Assistant in 2003 and 2002.
23. ACM SIGDA Design Automation Summer School (DASS) Fellowship Award for 2001.
24. 139th Ranking in all India level Graduate Aptitude Test in Engineering (GATE) in Electrical Engineering, 1997.
25. 44th Ranking in all India level Graduate Aptitude Test in Engineering (GATE) in Electrical Engineering, 1996.
26. 3rd Ranking in the University during Bachelors degree in Electrical Engineering, Orissa University of Agriculture and Technology, Bhubaneswar, India, 1995.
27. Council of Scientific and Industrial Research (CSIR), India Junior Research Fellowship Award i 1995.
28. Orissa University of Agriculture and Technology, India University Merit Scholarship Award during 1992-1995.
29. 98th Ranking in Orissa Joint Engineering Entrance Examination (OJEE), India in 1991.

GRANTS and PROJECTS

No.	Project Title	Agency	Total Amount	Duration	Role
01	Technical Committee on VLSI (TCVLSI)	IEEE-CS	$11,977	2017	PI
02	Memory Design Optimization for Low-Latency Embedded Vision Processor (LLEVS)	Air Force STTR (NanoWatt Design Inc.)	$150,000 (UNT - $45,000)	2015-2016	Principal Investigator
03	Exploring Emerging Technology based Energy Efficient IoT Sensors for Smart Cities	IUSSTF	$25,000 (Estimated)	2016	Senior Personnel
04	Technical Committee on VLSI (TCVLSI)	IEEE-CS	$15,312	2016	PI
05	Asian Faculty Mentoring Network UNT Team Mentoring Grants	UNT	$2,000	2015-2016	Co-Principal Investigator
06	International Outreach for Nanoelectronic and Information Systems	IEEE CASS	$2,000	2015	Principal Investigator
07	Technical Committee on VLSI (TCVLSI)	IEEE-CS	$6,400	2015	PI
08	Power and Thermal Aware Design of 3D ICs and Network-on-Chips	UGC (India)	$50,000 (Estimated)	2013-2014	Senior Personnel
09	Introduction of Nanoelectronics Courses in Undergraduate Computer Science and Computer Engineering Curricula	NSF	$180,000 (UNT - $90,000)	2010-2013	Principal Investigator
10	Infrastructure Acquisition for Statistical Power, Leakage, and Timing Modeling Towards Realization of Robust Complex Nanoelectronics Circuits	NSF	$269,265 ($20,000 match)	2009-2012	Principal Investigator
11	Fast PVT-Tolerant Physical Design of RF IC Components	SRC	$134,140 ($29,140 match)	2009-2012	Principal Investigator
12	Process Variation Aware Synthesis of Nano-CMOS Circuits	EPSRC (UK)	$400,000 (Estimated)	2009-2012	Senior Personnel
13	International Symposium on Electronic System Design (ISED)	NSF	$14,000 ($4,000 match)	2010-2011	Principal Investigator
14	A Comprehensive Methodology for Early Power-Performance Estimation of Nano-CMOS Digital Systems	NSF	$200,000 (UNT - $112,764)	2007-2010	Principal Investigator
15	Nanoelectronics Unified Fault Modeling and Experimentation - From Devices to Systems	UNT	$24,000	2008-2009	Principal Investigator
16	Watermarking Algorithms for Real-Time Copyright Protection and Subtitling during Digital Video Broadcasting in Internet Protocol Television (IP-TV)	UNT	$5,000	2008-2009	Principal Investigator
17	Secure Digital Camera (SDC) for Biometric Authentication	UNT	$5,000	2007	Principal Investigator
18	VLSI Architecture and Implementation of a Digital Video Broadcasting Network Processor (VNP) with Digital Rights Management (DRM) Facility	UNT	$5,000	2006	Principal Investigator

No.	Project Title	Agency	Total Amount	Duration	Role
19	Leakage Current Reduction in Nanometer VLSI Circuits using Dual Gate Dielectrics	UNT	$4,000	2005-2006	Principal Investigator
20	A Low Power Smart VLSI Controller for Nano-Characterization in Atomic Force Microscope (AFM)	UNT	$5,000	2005	Principal Investigator

PATENTS

1. **S. P. Mohanty** and E. Kougianos, Methodology for Nanoscale Technology based Mixed-Signal System Design, US Patent Number: 9,053,276, Issued on: 9th June 2015.
2. **S. P. Mohanty**, E. Kougianos, and G. Zheng, Intelligent Metamodel Integrated Verilog-AMS for Fast and Accurate Analog Block Design Exploration, US Patent Number: 9,026,964, Issued on: 5th May 2015.
3. **S. P. Mohanty**, Apparatus and Method for Transmitting Secure and/or Copyrighted Digital Video Broadcasting Data Over Internet Protocol Network, US Patent Number: 8,423,778, Issued on: 16th Apr 2013.
4. **S. P. Mohanty**, Methods and Devices for Enrollment and Verification of Biometric Information in Identification Documents, US Patent Number: 8,058,972, Issued on: 15th Nov 2011.

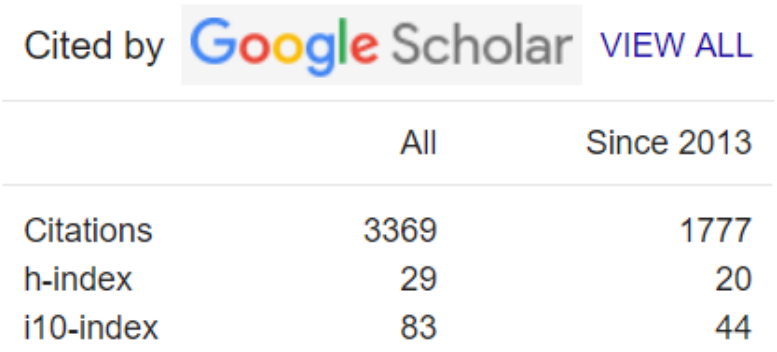
BOOKS

1. **S. P. Mohanty**, Nanoelectronic Mixed-Signal System Design, McGraw-Hill, 2015, ISBN-10: 0071825711, ISBN-13: 978-0071825719.
2. **S. P. Mohanty** and A. Srivastava (Editors), Nano-CMOS and Post-CMOS Electronics: Devices and Modelling, The Institute of Engineering and Technology (IET), 2016, ISBN-10: 1849199973, ISBN-13: 978-1849199971.
3. **S. P. Mohanty** and A. Srivastava (Editors), Nano-CMOS and Post-CMOS Electronics: Circuits and Design, The Institute of Engineering and Technology (IET), 2016, ISBN-10: 184919999X, ISBN-13: 978-1849199995.
4. J. Singh, **S. P. Mohanty**, and D. K. Pradhan, Robust SRAM Designs and Analysis, Springer, 2012, ISBN-10: 1461408172, ISBN-13: 978-1461408178.
5. **S. P. Mohanty**, A. Singh, and B. Panda (Editors), Proceedings of 12th International Conference on Information Technology (ICIT), McGraw-Hill, 2009, ISBN: 978-0-07-068014-2.
6. **S. P. Mohanty**, N. Ranganathan, E. Kougianos, and P. Patra, Low-Power High-Level Synthesis for Nanoscale CMOS Circuits, Springer, 2008, ISBN-10: 0387764739, ISBN-13: 978-0387764733.

BOOK CHAPTERS

1. A. Sengupta and **S. P. Mohanty**, "High-Level Synthesis of Digital Integrated Circuits in the Nanoscale Mobile Electronics Era", in Nano-CMOS and Post-CMOS Electronics: Circuits and Design, Edited by S. P. Mohanty and A. Srivastava, The Institute of Engineering and Technology (IET), 2016, ISBN-10: 184919999X, ISBN-13: 978-1849199995.
2. E. Kougianos and **S. P. Mohanty**, "SPICEless RTL Design Optimization of Nanoelectronic Digital Integrated Circuits", in Nano-CMOS and Post-CMOS Electronics: Circuits and Design, Edited by S. P. Mohanty and A. Srivastava, The Institute of Engineering and Technology (IET), 2016, ISBN-10: 184919999X, ISBN-13: 978-1849199995.
3. V. P. Yanambaka, **S. P. Mohanty**, E. Kougianos, and D. Ghai, "Nanoscale High-κ/Metal-Gate CMOS and FinFET based Logic Libraries", in Nano-CMOS and Post-CMOS Electronics: Devices and Modelling, Edited by S. P. Mohanty and A. Srivastava, The Institute of Engineering and Technology (IET), 2016, ISBN-10: 1849199973, ISBN-13: 978-1849199971.

4. **S. P. Mohanty** and E. Kougianos, "Polynomial Metamodel-Based Fast Optimization of Nanoscale PLL Components", in Models, Methods, and Tools for Complex Chip Design: Selected Contributions from FDL 2012, Edited by J. Haase, Springer, 2014, ISBN: 978-3-319-01417-3.
5. B. Joshi, D. K. Pradhan, and **S. P. Mohanty**, "Fault Tolerant Nano-Computing", in Robust Computing with Nano-scale Devices: Progresses and Challenges, Edited by C. Huang, Springer, 2010, ISBN: 978-90-481-8539-9.



Citations received by my articles as calculated by the Google Scholar.

REFEREED JOURNAL PUBLICATIONS

Year 2018:

1. **S. P. Mohanty**, E. Kougianos, and P. Guturu, "SBPG: Secure Better Portable Graphics for Trustworthy Media Communications in the IoT (Invited Paper)", *IEEE Access Journal*, Volume 6, 2018, pp. Accepted on 11 Jan 2018.
2. A. Sengupta, D. Roy, and **S. P. Mohanty**, "Triple-Phase Watermarking for Reusable IP Core Protection during Architecture Synthesis", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Volume X, Issue Y, 2017, pp. Accepted on 13 July 2017.
3. A. Sengupta, D. Roy, **S. P. Mohanty**, and P. Corcoran, "A Framework for Hardware Efficient Reusable IP Core for Grayscale Image CODEC", *IEEE Access Journal*, Volume 6, 2018, pp. 871–882.
4. P. Sundaravadivel, E. Kougianos, **S. P. Mohanty**, and M. Ganapathiraju, "Everything You Wanted to Know about Smart Healthcare", *IEEE Consumer Electronics Magazine (CEM)*, Volume 7, Issue 1, January 2018, pp. 18–28.
5. H. Thapliyal, R. K. Nath, and **S. P. Mohanty**, "Smart Home Environment for Mild Cognitive Impairment Population", *IEEE Consumer Electronics Magazine (CEM)*, Volume 7, Issue 1, January 2018, pp. 68–76.
6. D. Puthal, M. S. Obaidat, P. Nanda, M. Prasad, **S. P. Mohanty**, and A. Y. Zomaya, "Secure and Sustainable Load Balancing of Edge Datacenters in Fog Computing", *IEEE Communications Magazine*, Volume X, Issue Y, XX 2018, pp. Accepted on 05 Nov 2017.
7. D. Puthal, N. Malik, **S. P. Mohanty**, E. Kougianos, and C. Yang, "The Blockchain as a Decentralized Security Framework", *IEEE Consumer Electronics Magazine (CEM)*, Volume 7, Issue 2, March 2018, pp. 18–21.
8. S. S. Roy, D. Puthal, S Sharma, **S. P. Mohanty**, and A. Y. Zomaya, "Building a Sustainable Internet of Things", *IEEE Consumer Electronics Magazine (CEM)*, Volume 7, Issue 2, March 2018, pp. 42–49.
9. A. S. Sengupta, S. Satpathy, **S. P. Mohanty**, D. Baral, and B. K. Bhattacharyya, "A Supercapacitor Powered Novel Battery-Less Buck Converter for Efficient Power Delivery to CE Systems", *IEEE Consumer Electronics Magazine (CEM)*, Volume 7, Issue 5, September 2018, pp. xx-yy.
10. Z. Zhao, A. Srivastava, L. Peng, and **S. P. Mohanty**, "A Novel Calibration Method to Reduce the Error in Logarithmic Conversion with Its Circuit Implementation", *IET Circuits, Devices & Systems (CDS)*, Volume XX, Issue YY, ZZ 2018, pp. Accepted on 04 Jan 2018.

11. **S. P. Mohanty**, "Smart Technologies: The Key for Sustainable Smart Cities", Editorial, *IEEE Consumer Electronics Magazine (CEM)*, Volume 7, Issue 2, March 2018, pp. 3–4.
12. **S. P. Mohanty**, "Smart Health Care is Here to Improve Quality of Life", Editorial, *IEEE Consumer Electronics Magazine (CEM)*, Volume 7, Issue 1, January 2018, pp. 3–4.
13. **S. P. Mohanty**, M. Huebner, C. J. Xue, X. Li, and H. Li, "Circuit and System Design Automation for Internet of Things", Editorial, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Volume 37, Issue 1, January 2018, pp. 3–6.

Year 2017:

14. A. Sengupta, D. Roy, **S. P. Mohanty**, and P. Corcoran, "DSP Design Protection in CE through Algorithmic Transformation Based Structural Obfuscation", *IEEE Transactions on Consumer Electronics (TCE)*, Volume 63, Issue 4, November 2017, pp. 467–476.
15. A. Sengupta, S. Bhadauria, and **S. P. Mohanty**, "TL-HLS: Methodology for Low Cost Hardware Trojan Security Aware Scheduling with Optimal Loop Unrolling Factor during High Level Synthesis", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Volume 36, Issue 4, April 2017, pp. 655–668.
16. D. Puthal, **S. P. Mohanty**, P. Nanda, and U. Choppali, "Building Security Perimeters to Protect Network Systems Against Cyber Threats", *IEEE Consumer Electronics Magazine (CEM)*, Volume 6, Issue 4, October 2017, pp. 24–27.
17. C. Yang, D. Puthal, **S. P. Mohanty**, and E. Kougianos, "Big-Sensing-Data Curation for the Cloud is Coming", *IEEE Consumer Electronics Magazine (CEM)*, Volume 6, Issue 4, October 2017, pp. 48–56.
18. S. Joshi, **S. P. Mohanty**, and E. Kougianos, "Everything You Wanted to Know about PUFs", *IEEE Potentials Magazine*, Volume 36, Issue 6, November-December 2017, pp. 38–46.
19. **S. P. Mohanty**, A. Sengupta, P. Guturu, and E. Kougianos, "Everything You Want to Know About Watermarking", *IEEE Consumer Electronics Magazine (CEM)*, Volume 6, Issue 3, July 2017, pp. 83–91.
20. A. Majumder, J. Goswami, S. Ghosh, R. Shrivastawa, **S. P. Mohanty**, and B. K. Bhattacharyya, "Pay-Cloak: A Biometric Back Cover for Smartphone with Tokenization Principle for Cashless Payment", *IEEE Consumer Electronics Magazine (CEM)*, Volume 6, Issue 2, April 2017, pp. 78–88.
21. S. Ghosh, J. Goswami, A. Majumder, A. Kumar, **S. P. Mohanty**, and B. K. Bhattacharyya, "Swing-Pay: One Card Meets All User Payment and Identity Needs", *IEEE Consumer Electronics Magazine (CEM)*, Volume 6, Issue 1, January 2017, pp. 82–93.
22. M. Sarkar, P. Ghosal, and **S. P. Mohanty**, "Exploring the Feasibility of a DNA Computer: Design of an ALU using Sticker Based DNA Model", *IEEE Transactions on NanoBioscience (TNB)*, Volume 16, Issue 6, September 2017, pp. 383–399.
23. V. P. Yanambaka, **S. P. Mohanty**, E. Kougianos, D. Ghai, and G. Ghai, "Process Variation Analysis and Optimization of a FinFET based VCO", *IEEE Transactions on Semiconductor Manufacturing (TSM)*, Volume 30, Issue 02, May 2017, pp. 126-134.
24. A. Sengupta, S. Bhadauria, and **S. P. Mohanty**, "Low-cost security aware HLS methodology", *IET Computers & Digital Techniques (CDT)*, Volume 11, Issue 2, March 2017, pp. 68–79.
25. V. P. Yanambaka, **S. P. Mohanty**, and E. Kougianos, "Making Use of Semiconductor Manufacturing Process Variations: FinFET-based Physical Unclonable Functions for Efficient Security Integration in the IoT", *Springer Analog Integrated Circuits and Signal Processing Journal*, Volume 93, Issue 3, December 2017, pp. 429–441.
26. U. Albalawi, **S. P. Mohanty**, and E. Kougianos, "A New Region Aware Invisible Robust Blind Watermarking Approach", *Springer Multimedia Tools and Applications Journal*, Volume 76, Issue 20, October 2017, pp. 21303–21337.
27. Z. Zhao, A. Srivastava, L. Peng, S. Chen, and **S. P. Mohanty**, "A Novel Switchable Pin Method for Regulating Power in Chip-Multiprocessor", *Special Issue on Hardware Assisted Techniques for IoT and Bigdata Applications, Elsevier The VLSI Integration Journal*, Volume 58, June 2017, pp. 329–338.

28. M. Sarkar, P. Ghosal, and **S. P. Mohanty**, "Minimal Reversible Circuit Synthesis on a DNA Computer", *Springer Natural Computing Journal*, Volume 16, Issue 3, September 2017, pp. 463–472.
29. **S. P. Mohanty**, "Light to Serve as an Effective Wireless Communications Medium", Editorial, *IEEE Consumer Electronics Magazine (CEM)*, Volume 6, Issue 4, October 2017, pp. 3–5.
30. **S. P. Mohanty**, "Information Security and IP Protection are Increasingly Critical in the Current Global Context", Editorial, *IEEE Consumer Electronics Magazine (CEM)*, Volume 7, Issue 3, July 2017, pp. 3–5.
31. **S. P. Mohanty**, "Deep Learning Can Be Crucial for Smart Consumer Electronics", Editorial, *IEEE Consumer Electronics Magazine (CEM)*, Volume 7, Issue 2, April 2017, pp. 3–4.
32. **S. P. Mohanty**, "Consumer Electronics Can Help Improve Life", Editorial, *IEEE Consumer Electronics Magazine (CEM)*, Volume 7, Issue 1, January 2017, pp. 3–5.
33. **S. P. Mohanty**, X. Li, H. Li, and Y. Cao, "Nanoelectronic Devices and Circuits for Next Generation Sensing and Information Processing", Editorial, *IEEE Transactions on Nanotechnology (TNANO)*, Volume 16, Issue 3, May 2017, pp. 383–386.
34. A. Todri-Sanial, **S. P. Mohanty**, M. Comte, and M. Belleville, "Nanoelectronic Circuit and System Design Methods for the Mobile Computing Era", Editorial, *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, Volume 13, Issue 2, March 2017, pp. 12:1–12:2.
35. **S. P. Mohanty**, A. Srivastava, S. Hu, and P. Ghosal, "Hardware Assisted Techniques for IoT and Bigdata Applications", Editorial, *Elsevier The VLSI Integration Journal*, Volume 58, June 2017, pp. 263–266.

Year 2016:

36. E. Kougianos, **S. P. Mohanty**, G. Coelho, U. Albalawi, and P. Sundaravadivel, "Design of a High-Performance System for Secure Image Communication in the Internet of Things (Invited Paper)", *IEEE Access Journal*, Volume 4, 2016, pp. 1222–1242.
37. **S. P. Mohanty**, U. Choppali, and E. Kougianos, "Everything You Wanted to Know about Smart Cities", *IEEE Consumer Electronics Magazine (CEM)*, Volume 5, Issue 3, July 2016, pp. 60–70 (**Awarded Best Paper of the IEEE Consumer Electronics Magazine for the Year 2016.**).
38. M. L. Rajaram, E. Kougianos, **S. P. Mohanty**, and U. Choppali, "Wireless Sensor Network Simulation Frameworks: A Tutorial Review", *IEEE Consumer Electronics Magazine (CEM)*, Volume 5, Issue 2, April 2016, pp. 63–69.
39. M. Panchore, J. Singh, and **S. P. Mohanty**, "Impact of Channel Hot Carrier Effect in Junction and Doping-free Devices and Circuits", *IEEE Transactions on Electron Devices (TED)*, Volume 63, Issue 12, December 2016, pp. 5068–5071.
40. S. Joshi, **S. P. Mohanty**, and E. Kougianos, "Simscape based Ultra-Fast Design Exploration: Graphene-Nanoelectronic Circuit Case Studies", *Springer Analog Integrated Circuits and Signal Processing Journal*, Volume 87, Issue 3, June 2016, pp. 407–420.
41. A. Sengupta, **S. P. Mohanty**, F. Lombardi, and M. Zwolinski, "Security and Reliability Aware System Design for Mobile Computing Devices", Editorial, *IEEE Access Journal*, Volume 4, 2016, pp. 2976–2980.
42. **S. P. Mohanty**, "My First Issue as Editor-in-Chief", Editorial, *IEEE Consumer Electronics Magazine (CEM)*, Volume 5, Issue 4, October 2016, pp. 5–8.

Year 2015:

43. D. Roy, P. Ghosal, and **S. P. Mohanty**, "FuzzRoute: A Thermally Efficient Congestion-Free Global Routing Method for Three-Dimensional Integrated Circuits", *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Volume 21, Issue 1, November 2015, pp. 1:1–1:38.
44. E. Kougianos and **S. P. Mohanty**, "A Nature-Inspired Firefly Algorithm Based Approach for Nanoscale Leakage Optimal RTL Structure", *Elsevier The VLSI Integration Journal*, Volume 51, September 2015, pp. 46-60.
45. **S. P. Mohanty** and S. Kundu, "Circuit and System Design Methodologies for Emerging Technologies",

Editorial, *IEEE Transactions on Emerging Topics in Computing (TETC)*, Volume 3, Issue 4, December 2015, pp. 456–457.

Year 2014:

46. O. Okobiah, **S. P. Mohanty**, and E. Kougianos, "Fast Layout Optimization through Simple Kriging Metamodeling: A Sense Amplifier Case Study", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Volume 22, Issue 4, April 2014, pp. 932–937.
47. **S. P. Mohanty** and E. Kougianos, "Incorporating Manufacturing Process Variation Awareness in Fast Design Optimization of Nanoscale CMOS VCOs", *IEEE Transactions on Semiconductor Manufacturing (TSM)*, Volume 27, Issue 1, February 2014, pp. 22–31.
48. **S. P. Mohanty** and E. Kougianos, "Polynomial Metamodel Based Fast Optimization of Nano-CMOS Oscillator Circuits", *Springer Analog Integrated Circuits and Signal Processing Journal*, Volume 79, Issue 3, June 2014, pp. 437–453.
49. **S. P. Mohanty**, M. Gomathisankaran, and E. Kougianos, "Variability-Aware Architecture Level Optimization Techniques for Robust Nanoscale Chip Design", *Elsevier International Journal on Computers and Electrical Engineering (IJCEE)*, Volume 40, Issue 1, January 2014, pp. 168–193.
50. O. Okobiah, **S. P. Mohanty**, and E. Kougianos, "Nano-CMOS Thermal Sensor Design Optimization for Efficient Temperature Measurement", *Elsevier The VLSI Integration Journal*, Volume 47, Issue 2, March 2014, pp. 195–203.

Year 2013:

51. **S. P. Mohanty**, "Memristor: From Basics to Deployment", *IEEE Potentials*, Volume 32, No. 3, May/June 2013, pp. 34–39.
52. O. Okobiah, **S. P. Mohanty**, and E. Kougianos, "Geostatistical-Inspired Fast Layout Optimization of a Nano-CMOS Thermal Sensor", *IET Circuits, Devices & Systems (CDS)*, Volume 7, No. 5, September 2013, pp. 253–262.
53. D. Ghai, **S. P. Mohanty**, and G. Thakral, "Fast Optimization of Nano-CMOS Voltage-Controlled Oscillator using Polynomial Regression and Genetic Algorithm", *Elsevier Microelectronics Journal (MEJ)*, Volume 44, Issue 8, August 2013, pp. 631–641.
54. J. Mathew, **S. P. Mohanty**, S. Banerjee, D. K. Pradhan, and A. M. Jabir, "Attack Tolerant Cryptographic Hardware Design by Combining Galois Field Error Correction and Uniform Switching Activity", *Elsevier International Journal on Computers and Electrical Engineering (IJCEE)*, Volume 39, No. 4, May 2013, pp. 1077–1087.
55. S. Nimgaonkar, M. Gomathisankaran, and **S. P. Mohanty**, "TSV: A Novel Energy Efficient Memory Integrity Verification Scheme for Embedded Systems", *Elsevier Journal of Systems Architecture (JSA)*, Vol. 59, No. 7, August 2013, pp. 400–411.
56. S. Nimgaonkar, M. Gomathisankaran, and **S. P. Mohanty**, "MEM-DnP: A Novel Energy Efficient Approach for Memory Integrity Detection and Protection in Embedded Systems", *Springer Circuits, Systems, and Signal Processing Journal (CSSP)*, Volume 32, Issue 6, December 2013, pp. 2581–2604.
57. U. Choppali, E. Kougianos, **S. P. Mohanty**, and B. Gorman, "Influence of Annealing on Polymeric Precursor Derived ZnO Thin Films on Sapphire", *Elsevier Journal of Thin Solid Films (TSF)*, Vol. 545, pp. 466–470, October 2013.
58. P. K. Meher, **S. P. Mohanty**, A. P. Vinod, "Advanced Techniques for Efficient Electronic System Design", Editorial, *Springer Circuits, Systems, and Signal Processing Journal (CSSP)*, Volume 32, Issue 6, December 2013, pp. 2539–2541.
59. S. Kundu, **S. P. Mohanty**, and N. Ranganathan, "Design Methodologies for Nanoelectronic Digital and Analogue Circuits", Editorial, *IET Circuits, Devices & Systems (CDS)*, Volume 7, No. 5, September 2013, pp. 221–222.

Year 2012:

60. O. Garitselov, **S. P. Mohanty**, and E. Kougianos, "A Comparative Study of Metamodels for Fast and Accurate Simulation of Nano-CMOS Circuits", *IEEE Transactions on Semiconductor Manufacturing (TSM)*, Vol. 25, No. 1, February 2012, pp. 26–36.
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54. G. Zheng, **S. P. Mohanty**, E. Kougianos, and O. Okobiah, "iVAMS: Intelligent Metamodel-Integrated Verilog-AMS for Circuit-Accurate System-Level Mixed-Signal Design Exploration", in *Proceedings of the 24th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, 2013, pp. 75–78. (24 full, 15 short, and 22 poster papers accepted out of 125 submissions, acceptance rate – 48.8%)
55. D. Ghai, **S. P. Mohanty**, and G. Thakral, "Comparative Analysis of Double Gate FinFET Configurations for Analog Circuit Design", in *Proceedings of the 56th IEEE International Midwest Symposium on Circuits & Systems (MWSCAS)*, 2013, pp. 809–812.
56. D. Ghai, **S. P. Mohanty**, and G. Thakral, "Double Gate FinFET based Mixed-Signal Design: A VCO Case Study", in *Proceedings of the 56th IEEE International Midwest Symposium on Circuits & Systems (MWSCAS)*, 2013, pp. 177–180.
57. M. Sarkar, P. Ghosal, and **S. P. Mohanty**, "Reversible Circuit Synthesis Using ACO and SA based Quinne-McCluskey Method", in *Proceedings of the 56th IEEE International Midwest Symposium on Circuits & Systems (MWSCAS)*, 2013, pp. 416–419.
58. **S. P. Mohanty**, "DfX for Nanoelectronic Embedded Systems", Keynote Abstract, *International Conference on Control, Automation, Robotics and Embedded System (CARE)*, Indian Institute of Information Technology, Design and Manufacturing Jabalpur, India, 2013.

59. G. Zheng, **S. P. Mohanty**, E. Kougianos, "Verilog-AMS-POM: Verilog-AMS Integrated POlynomial Metamodelling of a Memristor-based Oscillator", *Work-in-Progress Session Poster, Design Automation Conference (DAC)*, 2013.
60. G. Zheng, **S. P. Mohanty**, E. Kougianos, "iVAMS: Intelligent Metamodel-Integrated Verilog-AMS for Fast Analog Block Optimization", *Work-in-Progress Session Poster, Design Automation Conference (DAC)*, 2013.

Year 2012:

61. O. Okobiah, **S. P. Mohanty**, E. Kougianos, and O. Garitselov, "Kriging-Assisted Ultra-Fast Simulated-Annealing Optimization of a Clamped Bitline Sense Amplifier", in *Proceedings of the 25th International Conference on VLSI Design (VLSID)*, pp. 310–315, 2012 (**blind review**, 71 papers accepted out of 223 submissions, acceptance rate – 31.8%).
62. O. Garitselov, **S. P. Mohanty**, and E. Kougianos, "Fast-Accurate Non-Polynomial Metamodeling for nano-CMOS PLL Design Optimization", in *Proceedings of the 25th International Conference on VLSI Design (VLSID)*, pp. 316–321, 2012 (**blind review**, 71 papers accepted out of 223 submissions, acceptance rate – 31.8%).
63. O. Okobiah, **S. P. Mohanty**, and E. Kougianos, "Ordinary Kriging Metamodel-Assisted Ant Colony Algorithm for Fast Analog Design Optimization", in *Proceedings of the 13th International Symposium on Quality Electronic Design (ISQED)*, pp. 458–463, 2012 (**blind review**).
64. O. Garitselov, **S. P. Mohanty**, E. Kougianos, and O. Okobiah, "Metamodel-Assisted Ultra-Fast Memetic Optimization of a PLL for WiMax and MMDS Applications", in *Proceedings of the 13th International Symposium on Quality Electronic Design (ISQED)*, pp. 580–585, 2012 (**blind review**).
65. G. Zheng, **S. P. Mohanty**, E. Kougianos, and O. Garitselov, "Verilog-AMS-PAM: Verilog-AMS integrated with Parasitic-Aware Metamodels for Ultra-Fast and Layout-Accurate Mixed-Signal Design Exploration", in *Proceedings of the 21st ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 351–356, 2012 (**blind review**, 23 full and 18 short papers accepted out of 144 submissions, acceptance rate – 28.5%).
66. G. Zheng, **S. P. Mohanty**, and E. Kougianos, "Metamodel-Assisted Fast and Accurate Optimization of an OP-AMP for Biomedical Applications", in *Proceedings of the 11th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 273–278, 2012 (**blind review**).
67. O. Okobiah, **S. P. Mohanty**, and E. Kougianos, "Geostatistical-Inspired Metamodeling and Optimization of Nano-CMOS Circuits", in *Proceedings of the 11th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 326–331, 2012 (**blind review**).
68. O. Garitselov, **S. P. Mohanty**, E. Kougianos, and G. Zheng, "Particle Swarm Optimization over Non-Polynomial Metamodels for Fast Process Variation Resilient Design of Nano-CMOS PLL", in *Proceedings of the 21st ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 255–258, 2012 (**blind review**, 23 full, 18 short, and 30 poster papers accepted out of 144 submissions, acceptance rate – 49.3%).
69. O. Okobiah, **S. P. Mohanty**, E. Kougianos, O. Garitselov, and G. Zheng, "Stochastic Gradient Descent Optimization for Low Power Nanoscale CMOS Thermal Sensor Design", in *Proceedings of the 11th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 285–290, 2012 (**blind review**).
70. **S. P. Mohanty**, E. Kougianos, O. Garitselov, and J. M. Molina, "Polynomial-Metamodel Assisted Fast Power Optimization of Nano-CMOS PLL Components", in *Proceedings of the Forum on specification and Design Languages (FDL)*, pp. 233–238, 2012.
71. M. Poolakkaparambil, J. Mathew, A. M. Jabir, and **S. P. Mohanty**, "Low Complexity Cross Parity Codes for Multiple and Random Bit Error Correction", in *Proceedings of the 13th International Symposium on Quality Electronic Design (ISQED)*, pp. 57–62, 2012 (**blind review**).
72. M. Poolakkaparambil, J. Mathew, A. M. Jabir, and **S. P. Mohanty**, "An Investigation of Concurrent Error Detection over Binary Galois Fields in CNTFET and QCA Technologies", in *Proceedings of the 11th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 141–146, 2012 (**blind review**).
73. G. K. Reddy, K. Jainwal, J. Singh, and **S. P. Mohanty**, "Process Variation Tolerant 9T SRAM Bitcell Design", in *Proceedings of the 13th International Symposium on Quality Electronic Design (ISQED)*, pp.

492–496, 2012 (**blind review**).

74. P. Yeolekar, R. A. Shafik, J. Mathew, D. K. Pradhan, and **S. P. Mohanty**, "STEP: A Unified Design Methodology for Secure Test and IP Core Protection", in *Proceedings of the 21st ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 333–338, 2012 (**blind review**, 23 full and 18 short papers accepted out of 144 submissions, acceptance rate – 28.5%).
75. R. A. Shafik, B. M. Al-Hashimi, J. Mathew, D. K. Pradhan, and **S. P. Mohanty**, "RAEF: A Power Normalized System-Level Reliability Analysis and Estimation Framework", in *Proceedings of the 11th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 189–194, 2012 (**blind review**).
76. G. Zheng, **S. P. Mohanty**, and E. Kougianos, "Design and Modeling of a Continuous-Time Delta-Sigma Modulator for Biopotential Signal Acquisition: Simulink Vs Verilog-AMS Perspective", in *Proceedings of the 3rd International Conference on Computing, Communication and Networking Technologies (ICCCNT)*, pp. 1–6, 2012.

Year 2011:

77. S. Banerjee, J. Mathew, D. K. Pradhan, **S. P. Mohanty**, and M. Ciesielski, "Variation-Aware TED-Based Approach for Nano-CMOS RTL Leakage Optimization", in *Proceedings of the 24th International Conference on VLSI Design (VLSID)*, pp. 304–309, 2011 (**blind review**, 66 papers accepted out of 330 submissions, acceptance rate – 20.0%).
78. O. Okobiah, **S. P. Mohanty**, and E. Kougianos, M. Poolakkaparambil, "Towards Robust Nano-CMOS Sense Amplifier Design: A Dual-Threshold versus Dual-Oxide Perspective", in *Proceedings of the 21st ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 145–150, 2011 (**blind review**, 57 papers accepted out of 207 submissions, acceptance rate - 27.5%).
79. **S. P. Mohanty** and E. Kougianos, "PVT-Tolerant 7-Transistor SRAM Optimization via Polynomial Regression", in *Proceedings of the 2nd International Symposium on Electronic System Design (ISED)*, pp. 39–44, 2011 (**blind review**, 62 papers accepted out of 146 submissions, acceptance rate – 42.4%).
80. O. Garitselov, **S. P. Mohanty**, E. Kougianos, and P. Patra, "Bee Colony Inspired Metamodeling Based Fast Optimization of a Nano-CMOS PLL", in *Proceedings of the 2nd International Symposium on Electronic System Design (ISED)*, pp. 6–11, 2011 (**blind review**, 62 papers accepted out of 146 submissions, acceptance rate – 42.4%).
81. M. Poolakkaparambil, J. Mathew, A. Jabir, D. K. Pradhan, and **S. P. Mohanty**, "BCH Code Based Multiple Bit Error Correction in Finite Field Multiplier Circuits", in *Proceedings of the 12th International Symposium on Quality Electronic Design (ISQED)*, pp. 615–620, 2011 (**blind review**, 92 regular papers accepted out of 290 submissions, acceptance rate - 31.7%).
82. O. Garitselov, **S. P. Mohanty**, and E. Kougianos, "Fast Optimization of Nano-CMOS Mixed-Signal Circuits Through Accurate Metamodeling", in *Proceedings of the 12th International Symposium on Quality Electronic Design (ISQED)*, pp. 405–410, 2011 (**blind review**, 92 regular papers and 34 poster papers accepted out of 290 submissions, acceptance rate - 43.4%).
83. L. Sun, J. Mathew, D. K. Pradhan, and **S. P. Mohanty**, "Statistical Blockade Method for Fast Robustness Estimation and Compensation of Nano-CMOS Arithmetic Circuits", in *Proceedings of the 2nd International Symposium on Electronic System Design (ISED)*, pp. 194–199, 2011 (**blind review**, 62 papers accepted out of 146 submissions, acceptance rate – 42.4%).
84. M. Hosseinabady, P. Lotfi-Kamran, J. Mathew, **S. P. Mohanty**, and D. K. Pradhan, "Single-Event Transient Analysis in High Speed Circuits", in *Proceedings of the 2nd International Symposium on Electronic System Design (ISED)*, pp. 112–117, 2011 (**blind review**, 62 papers accepted out of 146 submissions, acceptance rate – 42.4%).

Year 2010:

85. **S. P. Mohanty**, D. Ghai, and E. Kougianos, "A P4VT (Power-Performance-Process-Parasitic-Voltage-

Temperature) Aware Dual-V_{Th} Nano-CMOS VCO", in *Proceedings of the 23rd International Conference on VLSI Design (VLSID)*, pp. 99-104, 2010 (**blind review**, 70 papers accepted out of 320 submissions, acceptance rate - 21.8%).

86. G. Thakral, **S. P. Mohanty**, D. Ghai, and D. K. Pradhan, "A Combined DOE-ILP Based Power and Read Stability Optimization in Nano-CMOS SRAM", in *Proceedings of the 23rd International Conference on VLSI Design (VLSID)*, pp. 45-50, 2010 (**blind review**, 70 papers accepted out of 320 submissions, acceptance rate - 21.8%).
87. G. Thakral, **S. P. Mohanty**, D. Ghai, and D. K. Pradhan, "A DOE-ILP Assisted Conjugate-Gradient Approach for Power and Stability Optimization in High-κ/Metal-Gate SRAM", in *Proceedings of the 20th ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 323-328, 2010 (**blind review**, 30 full papers accepted out of 165 submissions, acceptance rate - 18.1%).
88. S. K. Mandal, R. Denton, **S. P. Mohanty**, and R. N. Mahapatra, "Low Power Nanoscale Buffer Management for Network on Chip Routers", in *Proceedings of the 20th ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 245-250, 2010 (**blind review**, 30 full papers accepted out of 165 submissions, acceptance rate - 18.1%).
89. J. Singh, D. S. Aswar, **S. P. Mohanty**, and D. K. Pradhan, "A 2-Port 6T SRAM Bitcell Design with Multi-Port Capabilities at Reduced Area Overhead", in *Proceedings of the 11th International Symposium on Quality Electronic Design (ISQED)*, pp. 131-138, 2010 (**blind review**, 84 regular papers accepted out of 270 submissions, acceptance rate - 31.1%).
90. S. Banerjee, J. Mathew, D. K. Pradhan, and **S. P. Mohanty**, "Layout-Aware Illinois Scan Design for High Fault Coverage", in *Proceedings of the 11th International Symposium on Quality Electronic Design (ISQED)*, pp. 683-688, 2010 (**blind review**, 84 regular papers accepted out of 270 submissions, acceptance rate - 31.1%).
91. J. Mathew, S. Banerjee, H. Rahaman, D. K. Pradhan, **S. P. Mohanty**, and A. M. Jabir, "On the Synthesis of Attack Tolerant Cryptographic Hardware", in *Proceedings of the 18th IEEE/IFIP International Conference on VLSI and System-on-Chip (VLSI-SoC)*, pp. 286-291, 2010 (41 full papers accepted out of 199 submissions, acceptance rate - 20.6%).
92. O. Garitselov, **S. P. Mohanty**, E. Kougianos, and P. Patra, "Nano-CMOS Mixed-Signal Circuit Metamodeling Techniques: A Comparative Study", in *Proceedings of the 1st International Symposium on Electronic System Design (ISED)*, pp. 191–196, 2010 (**blind review**, 41 papers accepted out of 120 submissions, acceptance rate - 34.1%).
93. S. Banerjee, J. Mathew, D. K. Pradhan, **S. P. Mohanty**, and M. Ciesielski, "A Taylor Expansion Diagram Approach for Nano-CMOS RTL Leakage Optimization", in *Proceedings of the 1st International Symposium on Electronic System Design (ISED)*, pp. 71–76, 2010 (**blind review**, 41 papers accepted out of 120 submissions, acceptance rate - 34.1%).
94. L. Sun, J. Mathew, D. K. Pradhan, and **S. P. Mohanty**, "Algorithms for Rare Event Analysis in Nano-CMOS Circuits Using Statistical Blockade", in *Special Session on New Horizons in SoC and ASIC Design, Proceedings of the International SoC Design Conference (ISOCC)*, pp. 162–165, 2010.
95. G. Thakral, **S. P. Mohanty**, D. Ghai, and D. K. Pradhan, "P3 (Power-Performance-Process) Optimization of Nano-CMOS SRAM using Statistical DOE-ILP", in *Proceedings of the 11th International Symposium on Quality Electronic Design (ISQED)*, pp. 176-183, 2010 (**blind review**, 84 regular papers and 40 poster papers accepted out of 270 submissions, acceptance rate - 45.9%).
96. J. Mathew, H. Rahaman, A. Jabir, **S. P. Mohanty**, and D. K. Pradhan, "On the Design of Different Concurrent EDC Schemes for S-box and GF(P)", in *Proceedings of the 11th International Symposium on Quality Electronic Design (ISQED)*, pp. 211-218, 2010 (**blind review**, 84 regular papers and 40 poster papers accepted out of 270 submissions, acceptance rate - 45.9%).
97. R. R. Bani, **S. P. Mohanty**, E. Kougianos, and G. Thakral, "Design of a Reconfigurable Embedded Data Cache", in *Proceedings of the 1st International Symposium on Electronic System Design (ISED)*, pp. 163–168, 2010 (**blind review**, 41 papers accepted out of 120 submissions, acceptance rate - 34.1%).
98. J. Mathew, S. Banerjee, M. Poolakkaparambil, **S. P. Mohanty**, A. Jabir, and D. K. Pradhan, "Multiple-Bit Error Detection and Correction in GF Arithmetic Circuits", in *Proceedings of the 1st International*

Symposium on Electronic System Design (ISED), pp. 101–106, 2010 (**blind review**, 41 papers accepted out of 120 submissions, acceptance rate - 34.1%).

99. E. Kougianos and **S. P. Mohanty**, and P. Patra, "Digital Nano-CMOS VLSI Design Courses in Electrical and Computer Engineering Through Open-Source/Free Tools", in *Proceedings of the 1st International Symposium on Electronic System Design (ISED)*, pp. 265–270, 2010.

Year 2009:

100. J. Singh, D. K. Pradhan, S. Hollis, **S. P. Mohanty**, and J. Mathew, "Single Ended 6T SRAM with Isolated Read-Port for Low-Power Embedded Systems", in *Proceedings of the 12th IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 917-922, 2009 (**blind review**, 226 papers accepted out of 965 submissions, acceptance rate - 23.4%).
101. J. Singh, J. Mathew, **S. P. Mohanty**, and D. K. Pradhan, "Single Ended Static Random Access Memory for Low-V_{dd}, High-Speed Embedded Systems", in *Proceedings of the 22nd International Conference on VLSI Design (VLSID)*, pp. 307-312, 2009 (**blind review**, 57 regular papers and 22 short papers accepted out of 320 submissions, acceptance rate - 24.6%).
102. **S. P. Mohanty**, D. Ghai, E. Kougianos, and B. Joshi, "A Universal Level Converter Towards the Realization of Energy Efficient Implantable Drug Delivery Nano-Electro-Mechanical-Systems", in *Proceedings of the 10th International Symposium on Quality Electronic Design (ISQED)*, pp. 673-679, 2009 (**blind review**, 87 regular papers accepted out of 300 submissions, acceptance rate - 29%).
103. D. Ghai, **S. P. Mohanty**, E. Kougianos, and P. Patra, "A PVT Aware Accurate Statistical Logic Library for High- Metal-Gate Nano-CMOS", in *Proceedings of the 10th International Symposium on Quality Electronic Design (ISQED)*, pp. 47-54, 2009 (**blind review**, 87 regular papers accepted out of 300 submissions, acceptance rate - 29%).
104. D. Ghai, **S. P. Mohanty**, and E. Kougianos, "Unified P4 (Power-Performance-Process-Parasitic) Fast Optimization of a Nano-CMOS VCO", in *Proceedings of the 19th ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 303-308 , 2009 (**blind review**, 62 regular papers accepted out of 215 submissions, acceptance rate - 29%).
105. D. Ghai, **S. P. Mohanty**, and E. Kougianos, "Variability-Aware Optimization of Nano-CMOS Active Pixel Sensors using Design and Analysis of Monte Carlo Experiments", in *Proceedings of the 10th International Symposium on Quality Electronic Design (ISQED)*, pp. 172-178, 2009 (**blind review**, 87 regular papers and 50 poster papers accepted out of 300 submissions, acceptance rate - 45.7%).
106. **S. P. Mohanty**, E. Kougianos, Wei Cai, and M. Ratnani, "VLSI Architectures of Perceptual Based Video Watermarking for Real-Time Copyright Protection", in *Proceedings of the 10th International Symposium on Quality Electronic Design (ISQED)*, pp. 527-534, 2009 (**blind review**, 87 regular papers and 50 poster papers accepted out of 300 submissions, acceptance rate - 45.7%).
107. **S. P. Mohanty**, "GPU-CPU Multi-Core For Real-Time Signal Processing", in *Proceedings of the 27th IEEE International Conference on Consumer Electronics (ICCE)*, pp. 55-56, 2009.
108. **S. P. Mohanty**, D. Ghai, E. Kougianos, and P. Patra, "A Combined Packet Classifier and Scheduler Towards Net-Centric Multimedia Processor Design", in *Proceedings of the 27th IEEE International Conference on Consumer Electronics (ICCE)*, pp. 11-12, 2009.
109. **S. P. Mohanty** and D. K. Pradhan, "Tabu Search Based Gate Leakage Optimization using DKCMOS Library in Architecture Synthesis", in *Proceedings of the 12th International Conference on Information Technology (ICIT)*, pp. 3-9, 2009 (**blind review**, 54 papers accepted out of 148 submissions, acceptance rate - 36.4%).
110. **S. P. Mohanty** and B. K. Panigrahi, "ILP Based Leakage Optimization During Nano-CMOS RTL Synthesis: A DOXCMOS Versus DTCMOS Perspective", in *Proceedings of the International Symposium on Biologically Inspired Computing And Applications (BICA)*, pp. 1367-1372, 2009 (70 papers accepted out of 130 submissions, acceptance rate - 53.8%).
111. E. Kougianos, **S. P. Mohanty**, and D. K. Pradhan, "Simulink Based Architecture Prototyping of Compressed Domain MPEG-4 Watermarking", in *Proceedings of the 12th International Conference on Information*

Technology (ICIT), pp. 10-16, 2009 (**blind review**, 54 papers accepted out of 148 submissions, acceptance rate - 36.4%).

112. **S. P. Mohanty**, "Unified Challenges in Nano-CMOS High-Level Synthesis", Abstract, Invited Talk, in *Proceedings of the 22nd International Conference on VLSI Design (VLSID)*, pp. 531-531, 2009.

Year 2008:

113. S. K. Mandal, P. Bhojwani, **S. P. Mohanty**, and R. N. Mahapatra, "IntellBatt: Towards Smarter Battery Design", in *Proceedings of the 45th ACM/IEEE Design Automation Conference (DAC)*, pp. 872-877, 2008 (**blind review**, 147 papers accepted out of 639 submissions, acceptance rate - 23%).
114. **S. P. Mohanty**, "ILP based Gate Leakage Optimization using DKCMOS Library during RTL Synthesis", in *Proceedings of the 9th International Symposium on Quality Electronic Design (ISQED)*, pp. 174-177, 2008 (**blind review**, 90 regular papers accepted out of 300 submissions, acceptance rate - 30%).
115. D. Ghai, **S. P. Mohanty**, and E. Kougianos, "A Process and Supply Variation Tolerant Nano-CMOS Low Voltage, High Speed, A/D Converter for System-on-Chip", in *Proceedings of the 18th ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 47-52, 2008 (**blind review**, 40 regular papers accepted out of 220 submissions, acceptance rate - 18.2%).
116. D. Ghai, **S. P. Mohanty**, and E. Kougianos, "A Dual Oxide CMOS Universal Voltage Converter for Power Management in Multi-VDD SoCs", in *Proceedings of the 9th International Symposium on Quality Electronic Design (ISQED)*, pp. 257-260, 2008 (**blind review**, 90 regular papers and 65 poster papers accepted out of 300 submissions, acceptance rate - 51.6%).
117. D. Ghai, **S. P. Mohanty**, and E. Kougianos, "Parasitic Aware Process Variation Tolerant Voltage Controlled Oscillator (VCO) Design", in *Proceedings of the 9th International Symposium on Quality Electronic Design (ISQED)*, pp. 330-333, 2008 (**blind review**, 90 regular papers and 65 poster papers accepted out of 300 submissions, acceptance rate - 51.6%).
118. J. Singh, J. Mathew, D. K. Pradhan, and **S. P. Mohanty**, "A Subthreshold Single Ended I/O SRAM Cell Design for Nanometer CMOS Technologies", in *Proceedings of the IEEE International SOC Conference (SOCC)*, pp. 243-246, 2008 (**blind review**).
119. J. Singh, J. Mathew, D. K. Pradhan, and **S. P. Mohanty**, "Failure Analysis for Ultra Low Power Nano-CMOS SRAM Under Process Variations", in *Proceedings of the IEEE International SOC Conference (SOCC)*, pp. 251-254, 2008 (**blind review**).
120. J. Singh, J. Mathew, **S. P. Mohanty**, and D. K. Pradhan, "A Nano-CMOS Process Variation Induced Read Failure Tolerant SRAM Cell", in *Proceedings of the 40th IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 3334-3337, 2008 (911 papers accepted out of 1858 submissions, acceptance rate - 49%).
121. Y. -T. Pai, L. -T. Lee, S. -J. Ruan, Y. -H. Chen, **S. P. Mohanty**, and E. Kougianos, "Honeycomb Model Based Skin Color Detector for Face Detection", in *Proceedings of the 15th International Conference on Mechatronics and Machine Vision in Practice (M2VIP)*, pp. 11-16, 2008.

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122. **S. P. Mohanty** and E. Kougianos, "Simultaneous Power Fluctuation and Average Power Minimization during Nano-CMOS Behavioral Synthesis", in *Proceedings of the 20th International Conference on VLSI Design (VLSID)*, pp. 577-582, 2007 (**blind review**, 141 papers accepted out of 444 submissions, acceptance rate - 31.7%).
123. E. Kougianos and **S. P. Mohanty**, "Metrics to Quantify Steady and Transient Gate Leakage in Nanoscale Transistors: NMOS Vs PMOS Perspective", in *Proceedings of the 20th International Conference on VLSI Design (VLSID)*, pp. 195-200, 2007 (**blind review**, 141 papers accepted out of 444 submissions, acceptance rate - 31.7%).
124. **S. P. Mohanty**, N. Pati, and E. Kougianos, "A Watermarking Co-Processor for New Generation Graphics

Processing Units", in *Proceedings of the 25th IEEE International Conference on Consumer Electronics (ICCE)*, pp. 303-304, 2007.

125. **S. P. Mohanty**, O. B. Adamo, and E. Kougianos, "VLSI Architecture of an Invisible Watermarking Unit for a Biometric-Based Security System in a Digital Camera", in *Proceedings of the 25th IEEE International Conference on Consumer Electronics (ICCE)*, pp. 485-486, 2007.
126. **S. P. Mohanty**, E. Kougianos, and R. N. Mahapatra, "A Comparative Analysis of Gate Leakage and Performance of High-K Nanoscale CMOS Logic Gates", in *Proceedings of the 16th ACM/IEEE International Workshop on Logic and Synthesis (IWLS)*, pp. 31-38, 2007.
127. **S. P. Mohanty**, E. Kougianos, D. Ghai, and P. Patra, "Interdependency Study of Process and Design Parameter Scaling for Power Optimization of Nano-CMOS Circuits under Process Variation", in *Proceedings of the 16th ACM/IEEE International Workshop on Logic and Synthesis (IWLS)*, pp. 207-213, 2007.
128. J. Singh, J. Mathew, **S. P. Mohanty**, and D. K. Pradhan, "Statistical Analysis of Steady State Leakage Currents in Nano-CMOS Devices", in *Proceedings of the 25th IEEE Norchip Conference (NORCHIP)*, pp. 1-4, 2007.
129. **S. P. Mohanty**, S. T. Vadlamudi, and E. Kougianos, "A Universal Voltage Level Converter for Multi-V_{DD} Based Low-Power Nano-CMOS Systems-on-Chips (SoCs)", in *Proceedings of the 13th NASA Symposium on VLSI Design*, 2007, CD-ROM Electronic Proceedings paper # 2.2 (7 pages).
130. D. Ghai, **S. P. Mohanty**, and E. Kougianos, "A $45nm$ Flash Analog to Digital Converter for Low Voltage High Speed System on Chips", in *Proceedings of the 13th NASA Symposium on VLSI Design*, 2007, CD-ROM Electronic Proceedings paper # 2.4 (6 pages).
131. **S. P. Mohanty** and E. Kougianos, "Impact of Gate Leakage on Mixed Signal Design and Simulation of Nano-CMOS Circuits", in *Proceedings of the 13th NASA Symposium on VLSI Design*, 2007, CD-ROM Electronic Proceedings paper # 3.1 (10 pages).
132. **S. P. Mohanty**, R. Sheth, A. Pinto, and M. Chandy, "CryptMark: A Novel Secure Invisible Watermarking Technique for Double Layer Protection of Color Images", in *Proceedings of the 11th IEEE International Symposium on Consumer Electronics (ISCE)*, 2007, pp. 1-6.

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133. **S. P. Mohanty**, R. Velagapudi, and E. Kougianos, "Physical-Aware Simulated Annealing Optimization of Gate Leakage in Nanoscale Datapath Circuits", in *Proceedings of the 9th IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 1191-1196, 2006 (**blind review**, 233 papers accepted out of 834 submissions, acceptance rate - 27.9%).
134. **S. P. Mohanty** and E. Kougianos, "Steady and Transient State Analysis of Gate Leakage Current in Nanoscale CMOS Logic Gates", in *Proceedings of the 24th IEEE International Conference on Computer Design (ICCD)*, pp. 210-215, 2006 (**blind review**, 72 papers accepted out of 231 submissions, acceptance rate - 31%).
135. **S. P. Mohanty** and E. Kougianos, "Modeling and Reduction of Gate Leakage during Behavioral Synthesis of NanoCMOS Circuits", in *Proceedings of the 19th International Conference on VLSI Design (VLSID)*, pp. 83-88, 2006 (**blind review**, 88 regular papers accepted out of 328 submissions, acceptance rate - 26.8%).
136. **S. P. Mohanty**, R. Velagapudi, and E. Kougianos, "Dual-K Versus Dual-T Technique for Gate Leakage Reduction: A Comparative Perspective", in *Proceedings of the 7th International Symposium on Quality Electronic Design (ISQED)*, pp. 564-569, 2006 (**blind review**, 93 regular papers accepted out of 256 submissions, acceptance rate - 36.3%).
137. O. B. Adamo, **S. P. Mohanty**, E. Kougianos, and M. Varanasi, "VLSI Architecture for Encryption and Watermarking Units Towards the Making of a Secure Digital Camera", in *Proceedings of the IEEE International SOC Conference (SOCC)*, pp. in press, 2006 (**blind review**, 53 regular papers accepted out of 169 submissions, acceptance rate - 31.3%).
138. N. M. Kosaraju, M. Varanasi, and **S. P. Mohanty**, "A High-Performance VLSI Architecture for Advanced Encryption Standard (AES) Algorithm", in *Proceedings of the 19th International Conference on VLSI Design*

(VLSID), pp. 481-484, 2006 (**blind review**, 88 regular papers and 48 short papers accepted out of 328 submissions, acceptance rate - 41.5%).

139. **S. P. Mohanty**, P. Guturu, E. Kougianos, and N. Pati, "A Novel Invisible Color Image Watermarking Scheme using Image Adaptive Watermark Creation and Robust Insertion-Extraction", in *Proceedings of the IEEE International Symposium on Multimedia (ISM)*, pp. 153-160, 2006 (acceptance rate - 35%).
140. **S. P. Mohanty**, E. Kougianos, R. Velagapudi, and V. Mukherjee, "Scheduling and Binding for Low Gate Leakage NanoCMOS Datapath Circuit Synthesis", in *Proceedings of the 38th IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 5291-5294, 2006 (1439 papers accepted out of 2429 submissions, acceptance rate - 59%).
141. E. Kougianos and **S. P. Mohanty**, "Effective Tunneling Capacitance: A New Metric to Quantify Transient Gate Leakage Current", in *Proceedings of the 38th IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2937-2940, 2006 (1439 papers accepted out of 2429 submissions, acceptance rate - 59%).
142. Y. Zhuo, H. Li, and **S. P. Mohanty**, "A Congestion Driven Placement Algorithm for FPGA Synthesis", in *Proceedings of the 16th IEEE International Conference on Field Programmable Logic and Applications (FPL)*, pp. 683-686, 2006 (85 full papers and 80 poster papers accepted out of 307 submissions, acceptance rate - 53.7%).
143. W. Li, **S. P. Mohanty**, and K. Kavi, "A Hardware Assisted High Performance PHK Memory Manager", in *Proceedings of the ISCA 19th International Conference on Parallel and Distributed Computing Systems (PDCS)*, pp. 229-234, 2006.
144. V. Mukherjee, **S. P. Mohanty**, E. Kougianos, R. Allawadhi, and R. Velagapudi, "Gate Leakage Current Analysis in READ/WRITE/IDLE States of a SRAM Cell", in *Proceedings of IEEE Region 5 Technology and Science Conference*, pp. 196-200, 2006.
145. O. B. Adamo, **S. P. Mohanty**, E. Kougianos, M. Varanasi, and W. Cai, "VLSI Architecture and FPGA Prototyping of a Digital Camera for Image Security and Authentication", in *Proceedings of IEEE Region 5 Technology and Science Conference*, pp. 154-158, 2006.
146. C. A. Kincaid, **S. P. Mohanty**, A. R. Mikler, E. Kougianos, and B. Parker, "A High Performance ASIC for Cellular Automata (CA) Applications", in *Proceedings of the 9th International Conference on Information Technology (ICIT)*, pp. 289-290, 2006 (**blind review**, 83 papers accepted out of 231 submissions, acceptance rate - 35.9%).
147. G. Sarivisetti, E. Kougianos, **S. P. Mohanty**, A. Palakodety, and A. K. Ale, "Optimization of a $45nm$ CMOS Voltage Controlled Oscillator using Design of Experiments", in *Proceedings of IEEE Region 5 Technology and Science Conference*, pp. 87-90, 2006.

Year 2005:

148. V. Mukherjee, **S. P. Mohanty**, and E. Kougianos, "A Dual Dielectric Approach for Performance Aware Gate Tunneling Reduction in Combinational Circuits", in *Proceedings of the 23rd IEEE International Conference on Computer Design (ICCD)*, pp. 431-436, 2005 (**blind review**, 101 papers accepted out of 313 submissions, acceptance rate - 32%).
149. **S. P. Mohanty**, N. Ranganathan, and K. Balakrishnan, "Design of a Low Power Image Watermarking Encoder using Dual Voltage and Frequency", in *Proceedings of the 18th International Conference on VLSI Design (VLSID)*, pp. 153-158, 2005 (**blind review**, 97 regular papers accepted out of 352 submissions, acceptance rate - 28%).
150. **S. P. Mohanty**, V. Mukherjee, and R. Velagapudi, "Analytical Modeling and Reduction of Direct Tunneling Current during Behavioral Synthesis of Nanometer CMOS Circuits", in *Proceedings of the 14th ACM/IEEE International Workshop on Logic and Synthesis (IWLS)*, 2005, pp. 249-256.
151. **S. P. Mohanty**, R. Velagapudi, V. Mukherjee, and H. Li , "Reduction of Direct Tunneling Power Dissipation during Behavioral Synthesis of Nanometer CMOS Circuits", in *Proceedings of the IEEE CS Annual Symposium on VLSI (ISLVSI)*, 2005 (37 regular papers and 31 poster papers accepted out of 126 submissions, acceptance rate - 53.9%).

Year 2004:

152. **S. P. Mohanty**, N. Ranganathan, and R. K. Namballa, "VLSI Implementation of Visible Watermarking for a Secure Digital Still Camera Design", in *Proceedings of the 17th International Conference on VLSI Design (VLSID)*, pp. 1063-1068, 2004 (**blind review**, 92 full papers accepted out of 330 submissions, acceptance rate - 27.8%).
153. **S. P. Mohanty**, N. Ranganathan, and S. K. Chappidi, "ILP Models for Energy and Transient Power Minimization During Behavioral Synthesis", in *Proceedings of the 17th International Conference on VLSI Design (VLSID)*, pp. 745-748, 2004 (**blind review**, 92 full papers and 46 short papers accepted out of 330 submissions, acceptance rate - 41.8%).
154. **S. P. Mohanty**, R. Kumara C., and S. Nayak, "FPGA Based Implementation of an Invisible-Robust Image Watermarking Encoder", *Lecture Notes in Computer Science (LNCS), Internal Conference on Information Technology 2004*, Springer-Verlag, Vol. 3356, pp. 344-353, 2004 (**blind review**, 44 full papers accepted out of 200 submissions, acceptance rate - 22%).

Year 2003:

155. **S. P. Mohanty**, N. Ranganathan, and S. K. Chappidi, "Power Fluctuation Minimization During Behavioral Synthesis using ILP-Based Datapath Scheduling", in *Proceedings of the 21st IEEE International Conference on Computer Design (ICCD)*, pp. 441-443, 2003 (**blind review**, 61 full papers and 17 short papers accepted out of 233 submissions, acceptance rate - 33.4%).
156. **S. P. Mohanty** and N. Ranganathan, "A Framework for Energy and Transient Power Reduction during Behavioral Synthesis", in *Proceedings of the 16th International Conference on VLSI Design 2003 (VLSID)*, pp. 539-545, 2003 (**blind review**, 84 accepted out of 210 submissions, acceptance rate - 40%) **(Nominated for best paper award; ranked within top 5 out of 210 submissions.)**.
157. **S. P. Mohanty** and N. Ranganathan, "Energy Efficient Scheduling for Datapath Synthesis", in *Proceedings of the 16th International Conference on VLSI Design 2003 (VLSID)*, pp. 446-451, 2003 (**blind review**, 84 accepted out of 210 submissions, acceptance rate - 40%).
158. **S. P. Mohanty**, N. Ranganathan, and S. K. Chappidi, "Simultaneous Peak and Average Power Minimization during Datapath Scheduling for DSP Processors", in *Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 215-220, 2003 (**blind review**, 17 full papers accepted out of 136 submissions, acceptance rate - 12.5%).
159. **S. P. Mohanty**, N. Ranganathan, and S. K. Chappidi, "An ILP-Based Scheduling Scheme for Energy Efficient High Performance Datapath Synthesis", in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, Vol. 5, pp. 313-316, 2003.
160. **S. P. Mohanty**, N. Ranganathan, and S. K. Chappidi, "Transient Power Minimization Through Datapath Scheduling in Multiple Supply Voltage Environment", in *Proceedings of the 10th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Vol. 1, pp. 300-303, 2003.
161. **S. P. Mohanty**, N. Ranganathan, and S. K. Chappidi, "Peak Power Minimization Through Datapath Scheduling", in *Proceedings of the IEEE-CS Annual Symposium on VLSI (ISVLSI)*, pp. 121-126, 2003 (26 full papers accepted out of 115 submissions, acceptance rate - 22.6%).
162. **S. P. Mohanty**, N. Ranganathan, and R. K. Namballa, "VLSI Implementation of Invisible Digital Watermarking Algorithms Towards the Development of a Secure JPEG Encoder", in *Proceedings of the IEEE Workshop on Signal Processing Systems (SIPS)*, pp. 183-188, 2003 (67 papers accepted out of 118 submissions, acceptance rate - 56.7%).

Year 2002 and Before:

163. **S. P. Mohanty**, N. Ranganathan, and V. Krishna, "Datapath Scheduling using Dynamic Frequency Clocking", in *Proceedings of the IEEE-CS Annual Symposium on VLSI (ISVLSI)*, pp. 65-70, 2002.

164. **S. P. Mohanty**, K. R. Ramakrishnan, and M. S. Kanakanhalli, "A DCT Domain Visible Watermarking Technique for Images", in *Proceedings of the IEEE International Conference on Multimedia and Expo (ICME)*, Vol. 2, pp. 1029-1032, 2000 (400 accepted out of 650 submissions, acceptance rate - 61.5%).
165. **S. P. Mohanty**, K. R. Ramakrishnan, and M. S. Kanakanhalli, "An Adaptive DCT Domain Visible Watermarking Technique for Protection of Publicly Available Images", in *Proceedings of the International Conference on Multimedia Processing and Systems (ICMPS)*, pp. 195-198, 2000.
166. **S. P. Mohanty**, K. R. Ramakrishnan, and M. S. Kanakanhalli, "A Dual Watermarking Technique for Images", in *Proceedings of the 7th ACM International Multimedia Conference (ACMMM)*, Vol. 2, pp. 49-51, 1999.

VLSI CHIPS DESIGNED

1. A 180nm CMOS Phase-Locked Loop (PLL), 2012.
2. A 180nm CMOS LC-VCO, 2011.
3. A 45nm CMOS Sense Amplifier, 2011.
4. A 45nm CMOS Ring Oscillator, 2010.
5. A 90nm CMOS Analog to Digital Converter (ADC), 2008.
6. A 90nm CMOS Voltage Controlled Oscillator (VCO), 2008.
7. A Universal Voltage Level Converter to Step-Up, Step-Down, Pass, or Block Signals, 2007.
8. A Dual Voltage and Dual Frequency Low Power CMOS VLSI Chip for DCT Domain Image Watermarking, 2005.
9. A CMOS VLSI Chip for Visible Image Watermarking, 2004.
10. A CMOS VLSI Chip for Invisible Image Watermarking, 2003.

INVITED TALKS and CONFERENCE PRESENTATIONS

Invited Presentations:

1. Smart Cities - Demystified, Keynote, 2nd International Conference on Man and Machine Interfacing (MAMI), 2017, Bhubaneswar, India, 23rd December 2017.
2. Internet of Things (IoT) - Demystified, Keynote, 16th International Conference on Information Technology (ICIT), 2017, Bhubaneswar, India, 22nd December 2017.
3. iVAMS: A Paradigm Shift System Simulation Framework for the IoT Era, Keynote Presentation, 17th IEEE International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE), Montpellier, France, 19th April 2016.
4. DFX for Nanoelectronic Systems, Government College of Engineering and Technology, Bhubaneswar, India, Invited Talk, 18th December 2014.
5. DfX for Nanoelectronic Embedded Systems, Keynote Address, International Conference on Control, Automation, Robotics and Embedded System (CARE), Indian Institute of Information Technology, Design and Manufacturing Jabalpur, India, 18th December 2013.
6. DfX for Nanoelectronic Circuits and Systems, Invited Talk, Oriental Group of Institutes, Bhopal, India, 23rd December 2013.
7. Energy Efficient Nanoelectronic System Design, Invited Talk, Energy Efficient Buildings and Communities Workshop, Tartu, Estonia, 21st May 2013.
8. Ultra-Fast Design Exploration of Nanoscale Circuits through Metamodeling, Invited Talk, Semiconductor Research Corporation (SRC), Texas Analog Center for Excellence (TxACE), 27th April 2012.
9. Towards The Design of Robust Secure Digital Cameras (SDC), Seminar, Department of Electrical and Computer Engineering, University of Calgary, Canada, 25th May 2010.
10. Unified Challenges in Nano-CMOS High-Level Synthesis, Invited Talk, 22nd International Conference on VLSI Design (VLSID), New Delhi, India, 7th January 2009.
11. Research in VLSI Design and CAD Laboratory (VDCL), Seminar, Industry Council meeting, Department of

Computer Science and Engineering University of North Texas (UNT), Denton, TX, on 2nd May 2008.

12. Low-Power Image Watermarking Chip Design, Seminar, CV Raman College of Engineering (CVRCE), Bhubaneswar, India, 3rd January 2008.
13. Power Dissipation in Nano-CMOS Circuits, Guest Lecture, Department of Electrical Engineering, University of North Texas, Denton, TX, 24th March 2008.
14. Circuits and Systems for Real-Time DRM of Multimedia, Seminar, Department of Electrical and Computer Engineering, Utah State University (USU), Utah, 15th May 2007.
15. Circuits and Systems for Real-Time DRM of Multimedia, Seminar, Department of Computer Science and Electrical Computer Engineering, University of Missouri-Kansas City (UMKC), MO, 5th May 2007.
16. A Secure Digital Camera for Real-Time Security and Copyright Protection of Multimedia, Seminar, Department of Electrical and Computer Engineering, University of Texas, San Antonio (UTSA), TX, 20th March 2007.
17. A Secure Digital Camera for Real-Time Security and Copyright Protection of Multimedia, Seminar, Department of Computer Science and Electrical Engineering, University of Maryland, Baltimore County (UMBC), Baltimore, MD, 9th March 2007.
18. Secure Digital Camera, Seminar, Department of Electrical Engineering, Indian Institute of Science (IISc), Bangalore, India, 8th January 2007.
19. Secure Digital Camera, Seminar, Indian Institute of Technology (IIT), Kharagpur, India, 27th December 2006.
20. Design of a Image Watermarking Low-Power Chip, Seminar, Institute of Technical Education and Research (ITER), Bhubaneswar, India, 23rd December 2006.
21. Secure Digital Camera, Seminar, College of Engineering and Technology (CET), Biju Patnaik University of Technology (BPUT), Bhubaneswar, India, 18th December 2006.
22. VLSI Design and CAD Research at University of North Texas, Seminar, Current Research in CSCE course (CSCE-5020), Department of Computer Science and Engineering, University of North Texas (UNT), Denton, TX, 15th February 2006.
23. Gate Leakage Analysis and Reduction in Nanoscale CMOS circuits, Seminar, Department of Computer Science and Engineering, Southern Methodist University (SMU), Dallas, TX, 16th November 2005.
24. DKDT: A Performance Aware Dual Dielectric Assignment for Tunneling Current Reduction, Seminar, Department of Electrical Engineering, University of Texas, Dallas (UTD), TX, 28th March 2005.
25. DKDT: A Performance Aware Dual Dielectric Assignment for Tunneling Current Reduction, Seminar, Department of Electrical and Computer Engineering, Oklahoma State University (OSU), Stillwater, OK, 10th March 2005.
26. DKDT: A Performance Aware Dual Dielectric Assignment for Tunneling Current Reduction, Seminar, Department of Electrical and Computer Engineering, University of Utah, Salt Lake City, UT, 4th February 2005.
27. Research at VLSI Design and CAD Laboratory (VDCL), Seminar, Industry Council meeting, Department of Computer Science and Engineering University of North Texas (UNT), Denton, TX, on 3rd December 2004.
28. A Dual Voltage Dual Frequency Low Power VLSI Chip for Image Watermarking, Seminar, Current Research in CSCE course (CSCI-5170), Department of Computer Science and Engineering, University of North Texas (UNT), Denton, TX, November 2004.
29. Low Power Design and Synthesis using Voltage and Frequency Reduction, Seminar, Department of Computer Science and Engineering University of North Texas (UNT), Denton, TX, 16th January 2004.
30. Low Power Design and Synthesis using Multiple Supply Voltage, Variable Frequency and Multicycling, Seminar, Department of Computer Engineering, Rochester Institute of Technology (RIT), Rochester, NY, 11th December 2003.
31. Energy and Transient Power Minimization using Multiple Supply Voltages and Dynamic Frequency Clocking, Seminar, Department of Electrical and Computer Engineering, New Jersey Institute of Technology (NJIT), Newark, NJ, 29th October 2003.

Conference Presentations:

32. A Wireless Sensor Network Simulation Framework for Structural Health Monitoring in Smart Cities, Presentation, 6th IEEE International Conference on Consumer Electronics - Berlin (ICCE-Berlin), 5th September, 2016, Berlin, Germany.
33. Embedding Low Cost Optimal Watermark During High Level Synthesis for Reusable IP Core Protection, Talk, 48th IEEE International Symposium on Circuits and Systems (ISCAS), 24th May 2016, Montreal, Canada.
34. Bee Colony Inspired Metamodeling Based Fast Optimization of a Nano-CMOS PLL, Talk, 2nd International Symposium on Electronic System Design (ISED), 19th December 2011, Kochi, India.
35. Low Power Nanoscale Buffer Management for Network on Chip Routers, Talk, 20th ACM Great Lakes Symposium on VLSI (GLSVLSI), Providence, RI, 17th May 2010.
36. Layout-Aware Illinois Scan Design for High Fault Coverage, Talk, 11th International Symposium on Quality Electronic Design (ISQED), San Jose, CA, 24th March 2010.
37. On the Design of Different Concurrent EDC Schemes for S-Box and GF(p), Presentation, 11th International Symposium on Quality Electronic Design (ISQED), San Jose, CA, 23rd March 2010.
38. P4VT (Power-Performance-Process-Parasitic-Voltage-Temperature) Aware Dual-V_{Th} Nano-CMOS VCO, Talk, 23rd International Conference on VLSI Design (VLSID), 6th January, Bangalore, India.
39. A Combined DOE-ILP Based Power and Read Stability Optimization in Nano-CMOS SRAM, Talk, 23rd International Conference on VLSI Design (VLSID), 6th January, Bangalore, India.
40. Tabu Search Based Gate Leakage Optimization using DKCMOS Library in Architecture Synthesis, Talk, 12th International Conference on Information Technology (ICIT), 23rd December 2009, Bhubaneswar, India.
41. Simulink Based Architecture Prototyping of Compressed Domain MPEG-4 Watermarking, Talk, 12th International Conference on Information Technology (ICIT), 23rd December 2009, Bhubaneswar, India.
42. ILP Based Leakage Optimization During Nano-CMOS RTL Synthesis: A DOXCMOS Versus DTCMOS Perspective, Talk, Proceedings of the International Symposium on Biologically Inspired Computing And Applications (BICA), 22nd December 2009, Bhubaneswar, India.
43. Single Ended Static Random Access Memory for Low-Vdd, High-Speed Embedded Systems, Talk, 22nd International Conference on VLSI Design (VLSID), New Delhi, India, 6th January 2009.
44. A Process and Supply Variation Tolerant Nano-CMOS Low Voltage, High Speed, A/D Converter for System-on-Chip, Talk, 18th ACM Great Lakes Symposium on VLSI (GLSVLSI), Orlando, FL, 5th May 2008.
45. Parasitic Aware Process Variation Tolerant Voltage Controlled Oscillator (VCO) Design, Presentation, International Symposium on Quality Electronic Design (ISQED), San Jose, CA, 18th March 2008.
46. A Dual Oxide CMOS Universal Voltage Converter for Power Management in Multi-V_{DD} SoCs, Presentation, International Symposium on Quality Electronic Design (ISQED), San Jose, CA, 18th March 2008.
47. ILP based Gate Leakage Optimization using DKCMOS Library during RTL Synthesis, Talk, International Symposium on Quality Electronic Design (ISQED), San Jose, CA, 18th March 2008.
48. CryptMark: A Novel Secure Invisible Watermarking Technique for Color Images, Talk, International Symposium on Consumer Electronics (ISCE), Dallas, TX, 21st June 2007.
49. Interdependency Study of Process and Design Parameter Scaling for Power Optimization of Nano-CMOS Circuits under Process Variation, Presentation, ACM/IEEE International Workshop on Logic and Synthesis (IWLS), San Diego, CA, 01st June 2007.
50. A Comparative Analysis of Gate Leakage and Performance of High-K Nanoscale CMOS Logic Gates, Presentation, ACM/IEEE International Workshop on Logic and Synthesis (IWLS), San Diego, CA, 30th May 2007.
51. Simultaneous Power Fluctuation and Average Power Minimization during Nano-CMOS Behavioral Synthesis, Talk, International Conference of VLSI Design (VLSID), Bangalore, India, 9th January 2007.
52. Metrics to Quantify Steady and Transient Gate Leakage in Nanoscale Transistors: NMOS Vs PMOS Perspective, Talk, International Conference of VLSI Design (VLSID), Bangalore, India, 8th January 2007.
53. Steady and Transient State Analysis of Gate Leakage Current in Nanoscale CMOS Logic Gates, Talk, IEEE

International Conference of Computer Design (ICCD), San Jose, CA, 3rd October 2006.

54. Dual-K Versus Dual-T Technique for Gate Leakage Reduction : A Comparative Perspective, Talk, 7th International Symposium on Quality Electronic Design (ISQED), San Jose, CA, 29th March 2006.
55. A High-Performance VLSI Architecture for Advanced Encryption Standard (AES) Algorithm, Talk, International Conference of VLSI Design (VLSID), Hyderabad, India, 6th January 2006.
56. Modeling and Reduction of Gate Leakage during Behavioral Synthesis of NanoCMOS Circuits, Talk, International Conference of VLSI Design (VLSID), Hyderabad, India, 5th January 2006.
57. A Dual Dielectric Approach for Performance Aware Gate Tunneling Reduction in Combinational Circuits, Talk, IEEE International Conference of Computer Design (ICCD), San Jose, CA, 4th October 2005.
58. Analytical Modeling and Reduction of Direct Tunneling Current during Behavioral Synthesis of Nanometer CMOS Circuits, Presentation, ACM/IEEE International Workshop on Logic and Synthesis (IWLS), Presentation, Lake Arrowhead, CA, 9th June 2005.
59. Reduction of Direct Tunneling Power Dissipation during Behavioral Synthesis of Nanometer CMOS Circuits, Presentation, IEEE CS Annual Symposium on VLSI (ISVLSI), Tampa, FL, 12th May 2005.
60. Peak Power Minimization Through Datapath Scheduling, Talk, IEEE CS Annual Symposium on VLSI (ISVLSI), Tampa, FL, 21st February 2003.
61. A DCT Domain Visible Watermarking Technique for Images, Talk, IEEE International Conference on Multimedia and Expo (ICME), New York City, NY, 31st July 2000.

COURSES DEVELOPED

1. **CSCE 6731: Advanced Topics in VLSI Systems (University of North Texas)**:
   The objective of this course is to understand design, simulation, synthesis, and optimization of nanoscale digital and analog/mixed-signal circuits and systems. The prerequisites are the following: knowledge of computer logic design, semiconductor physics, architecture, or CMOS VLSI. The selected topics covered under this course include the following: (1) Current Conduction Mechanisms in Nano-CMOS Devices. (2) Power Dissipation in nano-CMOS Logic Gates. (3) Origin and Effect of Process Variations. (4) Nano-CMOS Power, Leakage, and Delay Modeling and Estimation. (5) Architecture-Level Power, Leakage, and Delay Estimation for Nano-CMOS. (6) Power and Leakage Reduction Fundamentals. (7) Nanodevice based Design Flow. (8) Inside of a Circuit Simulator. (9) High-Level Synthesis Fundamentals. (10) Power Estimation at Transistor and Logic Levels. (11) Energy or Average Power Reduction Techniques. (12) Peak Power Reduction Techniques. (13) Transient Power Reduction Techniques. (14) Leakage Power Reduction Techniques. (15) Design of Analog and Mixed-Signal Systems, including: VCO, PLL, and Voltage Converters. A selected of the above topics are covered based on a theme. Some examples of the themes include: "Nanoscale Mixed-Signal System Design", "Nanoscale Circuit Synthesis", and "Nanoelectronic Circuit Design". The 3 credit hours course cay be repeated for credit with the consent of the instructor.
2. **CSCE 6651: Advanced VLSI Systems (University of North Texas)**:
   The objective of this course is to study design issues, such as power consumption, performance, silicon area, process variations, device scaling in nanometer CMOS circuits. The course is introduced with understanding the properties of MOS devices and employing them to implement small to large complex systems. This course will make the student proficient in design, layout and simulation of digital VLSI circuits using various CAD tools. The course syllabus tentatively includes MOS transistor theory, CMOS processing technology, circuit characterization and simulation, physics of power dissipation in a nanometer CMOS circuits, design of low voltage CMOS circuits, low power SRAM architectures, power estimation/analysis techniques, power optimization techniques, adaptive power supply systems, and emerging technology.
3. **CSCE 5740: Topics in Modern Electronic System Design (University of North Texas)**:
   The objective of this course is to discuss design of hardware components such as phase-locked loops, electronic signal converters, sensor circuits, and memory for efficient realization of modern electronic systems. This course will introduce the students to concepts and means for nanoelectronic based energy efficient design, high performance design, reliable system design, secure system design targeted for Internet

of Things (IoT) and smart city components.

4. **CSCE 5730/4730: Digital CMOS VLSI Design (University of North Texas)**:
   The objective of this course is to understand MOSFET transistor theory and to learn design of digital systems using such transistors. The course involves design, layout and simulation of digital VLSI circuits using various Computer-Aided-Design (CAD) tools. The regular teaching activity involves one lecture and one laboratory session per week. In order to provide a comprehensive learning process, the lecture introduces theory and analysis of various issues, and the laboratory session emphasizes the design and simulation of CMOS circuits. A tentative syllabus of the course includes MOS transistor theory, CMOS processing technology, circuit characterization, power dissipation, clocking strategies, and design methods and tools.
5. **CSCI 5330/CSCI 4330: Digital System Design with VHDL (University of North Texas)**:
   This course is about the design of digital systems using a hardware description language, VHDL. Students are taught about the structure of the individual components of a computer such as ALU, register file, and RAM, and how to combine them together in constructing a computer. Students acquire practical working knowledge of creating digital circuits using commercial VLSI CAD tools. The course consists of one lecture and one laboratory session per week. While during the regular lecture the theory and issues involved in digital system are the focus of discussion, the laboratory session involves the design and simulation of practical digital circuits.

STUDENT/SCHOLAR MENTORING

Postdoctoral Scholars Mentored:

1. J. Singh, Visiting Scholar, PDPM-Indian Institute of Information Technology Design and Manufacturing, Jabalpur, India, Fall 2016.
2. P. Ghosal, UGC Raman Post Doctoral Fellow, Indian Institute of Engineering Science and Technology, Shibpur, India, Summer 2013 – Summer 2014.

Ph.D. Dissertations Supervised:

3. U. Albalawi, Ph.D.(Computer Science and Engineering), Dissertation: "New Frameworks for Secure Image Communication in the Internet of Things (IoT)", Department of Computer Science and Engineering, University of North Texas, Summer 2016, Major Professor. (First Employment: University of Tabuk, Saudi Arabia.)
4. S. Joshi, Ph.D.(Computer Science and Engineering), Dissertation: "Analysis and Optimization of Graphene FET Based Integrated Circuits", Department of Computer Science and Engineering, University of North Texas, Spring 2016, Major Professor.
5. O. Okobiah, Ph.D.(Computer Science and Engineering), Dissertation: "Geostatistical Inspired Metamodeling and Optimization of Nanoscale Analog Circuits", Department of Computer Science and Engineering, University of North Texas, Spring 2014, Major Professor. (**Received Outstanding Ph.D. student in Computer Science and Engineering Award for the year 2013-2014**.) (**Received scholarship for ACM A.M. Turing Centenary Celebration 2012**.) (**Received scholarship for ACM SIGDA Design Automation Summer School 2011**.) (First Employment: Samsung Semiconductor)
6. S. Nimgaonkar, Ph.D.(Computer Science and Engineering), Dissertation: "Secure and Energy Efficient Execution Frameworks Using Virtualization and Light-Weight Cryptographic Components", Department of Computer Science and Engineering, University of North Texas, Summer 2014, Co-Major Professor. (First Employment: Cisco Systems, Inc.)
7. G. Zheng, Ph.D.(Computer Science and Engineering), Dissertation: "Layout-Accurate Ultra-Fast System Level Design Exploration Through Verilog-AMS", Department of Computer Science and Engineering, University of North Texas, Spring 2013, Major Professor. (**Received Outstanding Ph.D. student in Computer Science and Engineering Award for the year 2012-2013**.) (**Received scholarship for ACM**

A.M. Turing Centenary Celebration 2012.) (**Received scholarship for ACM SIGDA Design Automation Summer School 2011**.) (First Employment: Analog Devices, Inc.)

8. O. Garitselov, Ph.D.(Computer Science and Engineering), Dissertation: "Metamodeling-Based Fast Optimization of Nanoscale AMS-SoCs", Department of Computer Science and Engineering, University of North Texas, Spring 2012, Major Professor. (**Received Outstanding Ph.D. student in Computer Science and Engineering Award for the year 2011-2012**.) (**Received scholarship for ACM SIGDA Design Automation Summer School 2011**.) (First Employment: Spectracom Corporation)
9. G. Thakral, Ph.D.(Computer Science and Engineering), Dissertation: "Process-Voltage-Temperature Aware Nanoscale Circuit Optimization", Department of Computer Science and Engineering, University of North Texas, Fall 2010, Major Professor. (**First UNT woman Computer Science and Engineering Ph.D. with VLSI specialization**.) (Current Position: Professor and Dean (Academics), Oriental University, Indore, India.)
10. D. V. Ghai, Ph.D.(Computer Science and Engineering), Dissertation: "Variability Aware Low-Power Techniques for Nanoscale Mixed-Signal Circuits", Department of Computer Science and Engineering, University of North Texas, Spring 2009, Major Professor. (**First UNT Computer Science and Engineering Ph.D. with VLSI specialization**.) (Current Position: Professor and Dean (Engineering and Technology), Oriental University, Indore, India.)

Masters Theses Supervised:

11. V. Dhayal, M.S.(Computer Science), Thesis: "Exploring Simscape™ Modeling for Piezoelectric Sensor Based Energy Harvester", Department of Computer Science and Engineering, University of North Texas, Spring 2017, Major Professor. (First Employment: North Carolina State University)
12. N. Mukka, M.S.(Computer Engineering), Thesis: "Simulink® Based Modeling of A Multi Global Navigation Satellite System", Department of Computer Science and Engineering, University of North Texas, Summer 2016, Major Professor. (**Received Outstanding Master's student in Computer Engineering Award for the year 2015-2016**.) (First Employment: Sirius XM Radio Inc.)
13. G. Aluru, M.S.(Computer Engineering), Thesis: "Exploring Analog and Digital Design using the Open-source Electric VLSI Design System", Department of Computer Science and Engineering, University of North Texas, Spring 2016, Major Professor.
14. M. K. Mukka, M.S.(Computer Engineering), Thesis: "Simulink based Design and Implementation of a Solar Power based Mobile Charger", Department of Computer Science and Engineering, University of North Texas, Fall 2015, Major Professor.
15. M. L. Rajaram, M.S.(Electrical Engineering Technology), Thesis: "Comparative Analysis and Implementation of High Data Rate Wireless Sensor Network Simulation Frameworks", Department of Engineering Technology, University of North Texas, Fall 2015, Co-Major Professor.
16. A. Hanson, M.S.(Computer Science), Thesis: "General Purpose Computing in GPU - A Watermarking Case Study", Department of Computer Science and Engineering, University of North Texas, Summer 2014, Major Professor. (First Employment: AGS Consultants, LLC)
17. M. Gautam, M.S.(Computer Engineering), Thesis: "Exploring Memristor Based Analog Design in Simscape", Department of Computer Science and Engineering, University of North Texas, Spring 2013, Major Professor.
18. J. Franco, M.S.(Computer Engineering), Thesis: "Rapid Prototyping and Design of a Fast Random Number Generator", Department of Computer Science and Engineering, University of North Texas, Spring 2012, Major Professor. (First Employment: Raytheon Company)
19. G. Coelho, M.S.(Engineering Systems), Thesis: "OTA-Quadrotor: An Object-Tracking Quadrotor for Real-Time Detection and Recognition", Department of Engineering Technology, University of North Texas, Spring 2012, Co-Major Professor. (First Employment: Peterbilt Motors Company)
20. O. Okobiah, M.S.(Computer Engineering), Thesis: "Exploring Process-Variation Tolerant Design of Nanoscale Sense Amplifier Circuits", Department of Computer Science and Engineering, University of North

Texas, Fall 2010, Major Professor. (**Received Outstanding Master's student in Computer Engineering Award for the year 2010-2011**.) (First Employment: Joined Ph.D. Program)

21. I. Zarate, M.S.(Engineering Systems), Thesis: "Software and Hardware in the Loop Modeling of an Audio Watermarking Algorithm", Department of Engineering Technology, University of North Texas, Fall 2010, Co-Major Professor. (First Employment: Weatherford Inc.)
22. R. Rastogi Bani, M.S.(Computer Engineering), Thesis: "A New N-Way Reconfigurable Data Cache Architecture for Embedded Systems", Department of Computer Science and Engineering, University of North Texas, Fall 2009, Major Professor. (**Received Outstanding Master's student in Computer Engineering Award for year 2009-2010**.) (**Received International Education Committee Scholarship Award for the year 2009-2010**.) (First Employment: Center for Development of Advanced Computing (CDAC), Pune, India.)
23. S. Rangoonwala, M.S.(Engineering Systems), Thesis: "A Verilog 8051 Softcore for FPGA Applications", Department of Engineering Technology, University of North Texas, Spring 2009, Co-Major Professor. (First Employment: Joined Ph.D. Program)
24. S. Naraharisetti, M.S.(Computer Engineering), Thesis: "Region Aware DCT Domain Invisible Robust Blind Watermarking for Color Images", Department of Computer Science and Engineering, University of North Texas, Fall 2008, Major Professor. (**Received Outstanding Master's student in Computer Engineering Award for the year 2008-2009**.)
25. A. Mendoza, M.S.(Engineering Systems), Thesis: "Hardware Software Co-Design of a JPEG2000 Watermarking Encoder", Department of Engineering Technology, University of North Texas, Fall 2008, Co-Major Professor. (First Employment: Olympus Controls)
26. S. Tarigopula, M.S.(Computer Engineering), Thesis: "A CAM based High-Performance Classifier-Scheduler for a Video Network Processor", Department of Computer Science and Engineering, University of North Texas, Spring 2008, Major Professor. (**Received Outstanding Master's student in Computer Engineering Award for the year 2007-2008**.) (First Employment: GE)
27. N. Pati, M.S.(Computer Engineering), Thesis: "Occlusion Tolerant Object Recognition Methods for Video Surveillance and Tracking of Moving Civilian Vehicles", Department of Computer Science and Engineering, University of North Texas, Fall 2007, Co-Major Professor. (First Employment: FedEx)
28. S. T. Vadlamudi, M.S.(Computer Engineering), Thesis: "A Nano-CMOS Based Universal Voltage Level Converter for Multi-V_{DD} SoCs", Department of Computer Science and Engineering, University of North Texas, Spring 2007, Major Professor.
29. A. Palakodety, M.S.(Computer Engineering), Thesis: "CMOS Active Pixel Sensors for Digital Cameras: Current State-of-the-Art", Department of Computer Science and Engineering, University of North Texas, Spring 2007, Major Professor. (First Employment: Vertex Pharmaceuticals)
30. W. Cai, M.S.(Electronics Engineering Technology), Thesis: "FPGA Prototyping of a Watermarking Algorithm for MPEG-4", Department of Engineering Technology, University of North Texas, Spring 2007, Co-Major Professor. (First Employment: Microsoft Corporation)
31. G. Sarivisetti, M.S.(Computer Engineering), Thesis: "Design and Optimization of Components in a 45nm CMOS Phase Locked Loop", Department of Computer Science and Engineering, University of North Texas, Fall 2006, Major Professor. (**First UNT woman Computer Engineering graduate with VLSI specialization**.)
32. A. K. Ale, M.S.(Computer Engineering), Thesis: "Comparison and Evaluation of Existing Analog Circuit Simulators Through a Sigma-Delta Modulator", Department of Computer Science and Engineering, University of North Texas, Fall 2006, Major Professor.
33. O. B. Adamo, M.S.(Computer Engineering), Thesis: "VLSI Architecture and FPGA Prototyping of a Secure Digital Camera for Biometric Application", Department of Computer Science and Engineering, University of North Texas, Summer 2006, Major Professor. (**Third UNT Computer Engineering graduate with VLSI specialization**.) (First Employment: Joined Ph.D. Program)
34. R. Velagapudi, M.S.(Computer Engineering), Thesis: "Modeling and Reduction of Gate Leakage during Behavioral Synthesis of NanoCMOS Datapath Circuits", Department of Computer Science and Engineering,

University of North Texas, Spring 2006, Major Professor. (**Second UNT Computer Engineering graduate with VLSI specialization**.)

35. V. Mukherjee, M.S.(Computer Engineering), Thesis: "A Dual Dielectric Approach for Performance Aware Reduction of Gate Leakage in Combinational Circuits", Department of Computer Science and Engineering, University of North Texas, Spring 2006, Major Professor. (**First UNT Computer Engineering graduate with VLSI specialization**.) (First Employment: Amdocs Inc.)
36. C. Renuka Kumara, Masters of Science in VLSI CAD, Thesis: "VLSI Implementation of Invisible Robust/Fragile Digital Watermarking Algorithms", Manipal Centre for Information Science, Manipal Academy of Higher Education, India, Spring 2004, Co-Major Professor. (I remotely guided the master's thesis.) (First Employment: Synopsys India)

Undergraduate Students Mentored:

37. I. Lee, Senior Student, Texas Academy of Math and Science (TAMS), Spring 2017.
38. M. Behnia, Senior Student, Texas Academy of Math and Science (TAMS), Spring 2014 – Summer 2014.
39. J. E. Barcenas, Senior Student, B.S.(Computer Engineering), University of North Texas, Fall 2013 – Spring 2014.
40. R. A. Cerrato, Senior Student, B.S.(Computer Engineering), University of North Texas, Spring 2014.
41. T. Ali, Senior Student, B.S.(Computer Engineering), University of North Texas, Spring 2013.
42. T. T. Jost, Junior Student, B.S.(Pre Engineering), University of North Texas, Fall 2012 – Spring 2013.
43. R. Patel, Senior Student, B.S.(Computer Engineering), University of North Texas, Spring 2011.
44. J. Judge, Senior Student, Texas Academy of Math and Science (TAMS), Fall 2010.

Dissertations or Theses Currently Supervising:

45. P. Sundaravadivel, Ph.D.(Computer Science and Engineering), Research: "Sensors for IoT Applications", Department of Computer Science and Engineering, University of North Texas, since Fall 2015, Major Professor.
46. P. V. Yanambaka, Ph.D.(Computer Science and Engineering), Research: "Methods for FinFET based Digital and Analog Circuit Design", Department of Computer Science and Engineering, University of North Texas, since Fall 2014, Major Professor.
47. O. Okpokwasili, Ph.D.(Computer Science and Engineering), Research: "Simulation of Intelligent Battery Design and Management", Department of Computer Science and Engineering, University of North Texas, since Fall 2014, Major Professor.
48. A. Sayeed, Ph.D.(Computer Science and Engineering), Research: "Energy Efficient IoT Component Design", Department of Computer Science and Engineering, University of North Texas, since Spring 2016, Major Professor.
49. L. Rachakonda, Ph.D.(Computer Science and Engineering), Research: "Sensors for Smart Health Care", Department of Computer Science and Engineering, University of North Texas, since Fall 2017, Major Professor.

Dissertation or Thesis Committees Served:

50. S. Bhadauria, Ph.D.(Computer Science and Engineering), Dissertation: "Low Cost Fault Reliability and Trojan Security Aware High Level Synthesis for Application Specific Datapath Processors", Department of Computer Science and Engineering, Indian Institute of Technology Indore, India, Spring 2016.
51. L. Garg, Ph.D.(Electronics and Communication Engineering), Dissertation: "On Efficient and Accurate Surrogate Models of Leakage in CMOS Gated Circuits", Malaviya National Institute of Technology, Jaipur, India, October 2015.
52. K. K. Jha, Ph.D.(VLSI Design), Dissertation: "Tunnel FET Based Topologies for Low Power Digital and Analog Circuits", ABV - Indian Institute of Information Technology and Management, Gwalior, India, June

2015.

53. Z. Zhang, Ph.D.(Computer Science and Engineering), Dissertation: "Adaptive Power Management for Autonomic Resource Configuration in Large-Scale Computer Systems", Department of Computer Science and Engineering, University of North Texas, Spring 2015.
54. V. K. Mishra, Ph.D.(Computer Science and Engineering), Dissertation: "Multi-Objective Design Space Exploration in High-Level Synthesis for Application Specific Computing", Department of Computer Science and Engineering, Indian Institute of Technology Indore, India, Spring 2015.
55. S. Shrivastava, Ph.D.(Computer Science and Engineering), Dissertation: "Soybean Disease Administration Using Image Processing Techniques", Department of Computer Science and Engineering, Jaypee University of Engineering and Technology, Guna, India, Fall 2014.
56. R. Peesapati, Ph.D.(Electronic Science), Dissertation: "Development of FPGA based Coprocessors for Signal Processing Applications", School of Physics, University of Hyderabad, India, 2013.
57. R. Dutta, Ph.D.(Engineering), Dissertation: "Offering New Web Services for Efficient Web-Page Prediction", Department of Computer Science and Engineering, Jadavpur University, India, 2010.
58. A. Kundu, Ph.D.(Engineering), Dissertation: "Proposing Efficient Techniques to Develop Web Services and Multi-Agent Based Systems", Department of Computer Science and Engineering, Jadavpur University, India, 2009.
59. D. Sinha Roy, Ph.D.(Electrical and Electronics Engineering), Dissertation: "Software Reliability Analysis of Wavelet-Neuro-Fuzzy Based Algorithms for Computer Relaying", Department of Electrical and Electronics Engineering, Birla Institute of Technology, Mesra, India, 2009.
60. S. S. Dan, Ph.D.(Electronics Design and Technology), Dissertation: "Impact of Energy Quantization on Single Electron Transistor Devices and Circuits", Center for Electronics Design and Technology, Indian Institute of Science, Bangalore, India, March 2009.
61. W. Li, Ph.D.(Computer Science), Dissertation: "High-Performance Architecture using Speculative Threads and Dynamic Memory Management Hardware", Department of Computer Science and Engineering, University of North Texas, Fall 2007.
62. P. B. Pati, Ph.D.(Electrical Engineering), Dissertation: "Analysis of Multi-Lingual Documents with Complex Layout and Content", Department of Electrical Engineering, Indian Institute of Science, Bangalore, India, November 2006.
63. K. A. Amin, Ph.D.(Computer Science), Dissertation: "An Integrated Architecture for Ad Hoc Grids", Department of Computer Science and Engineering, University of North Texas, Fall 2005.
64. Y. Yestekov, M.S.(Computer Science), Thesis: "Design and Analysis of Novel Verifiable Voting Schemes", Department of Computer Science and Engineering, University of North Texas, Summer 2013.
65. I. Nwachukwu, M.S.(Computer Engineering), Thesis: "Techniques for Improving Uniformity in Direct-Mapped Caches", Department of Computer Science and Engineering, University of North Texas, Spring 2011.
66. H. Liddar, M.S.(Electronics Engineering Technology), Thesis: "Development of Hybrid Molecular Ultraviolet Photodetector Based on Guanosine Derivatives", Department of Engineering Technology, University of North Texas, Summer 2005, Minor Professor.

Visiting Scholars Mentored:

67. Y. -T. Pai, Visiting Ph.D. student from Department of Electronic Engineering, National Taiwan University of Science and Technology, Taiwan, R.O.C, Fall 2008 – Spring 2009.
68. C. -H. Lee, Visiting M.S. student from Department of Electronic Engineering, National Taiwan University of Science and Technology, Taiwan, R.O.C, Spring 2009.
69. L. -T. Lee, Visiting M.S. student from Department of Electronic Engineering, National Taiwan University of Science and Technology, Taiwan, R.O.C, Fall 2008.
70. S. -S. Chen, Visiting M.S. student from Department of Electronic Engineering, National Taiwan University of Science and Technology, Taiwan, R.O.C, Fall 2008.

71. J. -C. Hsu, Visiting M.S. student from Department of Electronic Engineering, National Taiwan University of Science and Technology, Taiwan, R.O.C, Fall 2008.

Individual Research Advised:

72. **Fall 2016**: P. Sundaravadivel - Ph.D. (Computer Science and Engineering), V. P. Yanambaka - Ph.D. (Computer Science and Engineering), M. A. Sayeed - Ph.D. (Computer Science and Engineering), L. Rachakonda - M.S.(Computer Engineering).
73. **Summer 2016**: V. P. Yanambaka - Ph.D. (Computer Science and Engineering), M. A. Sayeed - Ph.D. (Computer Science and Engineering).
74. **Spring 2016**: V. P. Yanambaka - Ph.D. (Computer Science and Engineering), P. Sundaravadivel - Ph.D. (Computer Science and Engineering), A. Sayeed - Ph.D. (Computer Science and Engineering), O. C. Okpokwasili - Ph.D. (Computer Science and Engineering), E. Z. Agu - Ph.D. (Computer Science and Engineering), S. Joshi - Ph.D. (Computer Science and Engineering), R. R. Bommineni - M.S. (Computer Engineering), D. R. Kanthala - M.S. (Computer Engineering), M. Kothapalli - M.S. (Computer Engineering), S. S. Muttavarapu - M.S. (Computer Engineering), M. Ponnam - M.S. (Computer Engineering), K. D. Sapireddy - M.S. (Computer Engineering).
75. **Fall 2015**: P. Sundaravadivel - Ph.D. (Computer Science and Engineering), O. C. Okpokwasili - Ph.D. (Computer Science and Engineering), E. Z. Agu - Ph.D. (Computer Science and Engineering), V. P. Yanambaka - Ph.D. (Computer Science and Engineering), N. Mukka - M.S. (Computer Engineering), V. S. Dhayal - M.S. (Computer Engineering).
76. **Spring 2015**: V. P. Yanambaka - Ph.D. (Computer Science and Engineering), O. C. Okpokwasili - Ph.D. (Computer Science and Engineering), U. Albalawi - Ph.D. (Computer Science and Engineering), P. Ajjampudi - M.S. (Computer Engineering), G. Aluru - M.S. (Computer Engineering), B. Beavers - M.S. (Computer Engineering), B. Dulam - M.S. (Computer Engineering), S. Polemreddy - M.S. (Computer Engineering).
77. **Fall 2014**: S. Joshi - Ph.D. (Computer Science and Engineering), V. P. Yanambaka - Ph.D. (Computer Science and Engineering), O. C. Okpokwasili - Ph.D. (Computer Science and Engineering), T. R. Dhamera - M.S. (Computer Engineering), M. K. Mukka - M.S. (Computer Engineering), K. Vema - M.S. (Computer Engineering), K. James - B.S. (Computer Engineering), R. Koehler - B.S. (Computer Engineering).
78. **Spring 2014**: E. Z. Agu - Ph.D. (Computer Science and Engineering), A. Khan - Ph.D. (Computer Science and Engineering), J. E. Barcenas - B.S. (Computer Engineering), B. D. Bergman - B.S. (Computer Engineering), A. L. Dsilva - B.S. (Computer Engineering).
79. **Fall 2013**: Md A. Khan - Ph.D. (Computer Science and Engineering), E. Z. Agu - Ph.D. (Computer Science and Engineering), S. B. Chava - M. S. (Computer Engineering), S. S. Chepuri - M. S. (Computer Engineering), V. N. Jaladi - M. S. (Computer Engineering), S. Vadlamudi - M. S. (Computer Engineering).
80. **Summer 2013**: L. N. Avula - M. S. (Computer Engineering), M. Deva - M. S. (Computer Engineering), S. Karlaputi - M. S. (Computer Engineering), S. Majety - M. S. (Computer Engineering), S. Sabbineni - M. S. (Computer Engineering), A. Vesangi - M. S. (Computer Engineering).
81. **Spring 2013**: A. Khan - Ph.D. (Computer Science and Engineering), R. K. Eluri - M. S. (Computer Engineering).
82. **Fall 2012**: H. Erupaka - M.S. (Computer Engineering) and J. Linhart - B.S. (Computer Engineering).
83. **Summer 2012**: A. Hanson - M.S. (Computer Science).
84. **Spring 2012**: O. Okobiah - Ph.D. (Computer Science and Engineering), M. Gautam - M.S. (Computer Engineering), A. Hanson - M.S. (Computer Science).
85. **Fall 2011**: G. Zheng - Ph.D. (Computer Science and Engineering), E. Z. Agu - M.S. (Computer Engineering).
86. **Summer 2011**: G. Zheng - Ph.D. (Computer Science and Engineering), O. Okobiah - Ph.D. (Computer Science and Engineering), Z. Derrick - B.S. (Computer Science), A. Humphries - B.S. (Computer Engineering).
87. **Spring 2011**: M. A. L. Dubasi - Ph.D. (Computer Science and Engineering), O. Garitselov - Ph.D. (Computer

Science and Engineering), O. Okobiah - Ph.D. (Computer Science and Engineering), S. Kamishetty - M.S. (Computer Engineering), J. C. Franco - M.S. (Computer Engineering), N. Dhar - M.S. (Computer Engineering).

88. **Fall 2010**: G. Thakral - Ph.D. (Computer Science and Engineering), S. Kamishetty - M.S. (Computer Engineering), S. R. Adama - M.S. (Computer Engineering), R. R. Peesari - M.S. (Computer Engineering), A. C. Jones - B.S. (Computer Engineering).
89. **Summer 2010**: G. Thakral - Ph.D. (Computer Science and Engineering), R. Kochara - M.S. (Computer Engineering).
90. **Spring 2010**: O. Garitselov - Ph.D. (Computer Science and Engineering), M. A. L. Dubasi - Ph.D. (Computer Science and Engineering), O. Okobiah - M.S. (Computer Engineering).
91. **Fall 2009**: G. Thakral - Ph.D. (Computer Science and Engineering), M. A. L. Dubasi - M.S. (Computer Engineering), N. Dhar - M.S. (Computer Engineering), H. T. Patrawala - M.S. (Electrical Engineering).
92. **Summer 2009**: G. Thakral - Ph.D. (Computer Science and Engineering).
93. **Spring 2009**: D. V. Ghai - Ph.D. (Computer Science and Engineering) and G. Thakral - Ph.D. (Computer Science and Engineering).
94. **Fall 2008**: M. R. Ratnani - Ph.D.(Computer Science and Engineering), R. Rastogi - M.S. (Computer Engineering).
95. **Summer 2008**: D. V. Ghai - Ph.D. (Computer Science and Engineering), T. Jawad - M.S. (Computer Engineering), Y. T. Meenakshisundaram - M.S. (Computer Engineering).
96. **Spring 2008**: D. V. Ghai - Ph.D. (Computer Science and Engineering), M. R. Ratnani - M.S. (Computer Engineering).
97. **Fall 2007**: D. V. Ghai - Ph.D. (Computer Science and Engineering), S. Naraharisetti - M.S. (Computer Engineering), S. Pamidimukkala - M.S. (Computer Engineering), R. Chalasani - M.S. (Computer Engineering), M. R. Ratnani - M.S. (Computer Engineering), L. R. Kankanala - M.S. (Computer Engineering).
98. **Summer 2007**: T. Jawad - M.S. (Computer Engineering), R. K. Kolli - M.S. (Computer Engineering), V. S. Kontham - M.S. (Computer Engineering), S. Koppanur - M.S. (Computer Engineering), R. Tale - M.S. (Computer Engineering), S. Vasarla - M.S. (Computer Engineering).
99. **Spring 2007**: D. V. Ghai - Ph.D. (Computer Science), L. Z. Zounon - M.S. (Computer Engineering), Y. M. Tiruneli - M.S. (Computer Engineering), S. Adumulla - M.S. (Computer Engineering), S. G. Moneswamy - M.S. (Computer Engineering), S. D. P. Kommineni - M.S. (Computer Engineering).
100. **Fall 2006**: D. V. Ghai - Ph.D. (Computer Science), S. Adumulla - M.S. (Computer Engineering), T. V. John - M.S. (Computer Engineering).
101. **Summer 2006**: A. Palakodety - M.S. (Computer Engineering), O. B. Adamo - M.S. (Computer Engineering), N. Pati - M.S. (Computer Engineering), V. K. Pemmaraju - M.S. (Computer Engineering), S. Tarigopula - M.S. (Computer Engineering), S. Kancherla - M.S. (Computer Engineering).
102. **Spring 2006**: N. Pati - M.S. (Computer Engineering), S. K. Maraboina - M.S. (Computer Engineering), V. K. Pemmaraju - M.S. (Computer Engineering).
103. **Fall 2005**: O. B. Adamo - M.S. (Computer Engineering), T. V. John - M.S. (Computer Engineering), A. Palakodety - M.S. (Computer Engineering).
104. **Summer 2005**: A. K. Ale - M.S. (Computer Engineering).
105. **Spring 2005**: R. Allawadhi - M.S. (Computer Engineering), S. Nagalla - M.S. (Computer Engineering), R. Velagapudi - M.S. (Computer Engineering), J. Wells - B.S. (Computer Engineering).
106. **Fall 2004**: V. Mukherjee - Ph.D. (Computer Science).

PROFESSIONAL SERVICES

Professional Membership:

1. Senior Member, IEEE (IEEE Computer Society, IEEE Circuits and Systems Society, and IEEE Consumer Electronics Society)

2. Senior Member, ACM (ACM Special Interest Group in Design Automation)
3. Ex-Officio Member of Board of Governors IEEE Consumer Electronics Society, 2016–Present.
4. Life Member, Orissa Information Technology Society (OITS), Bhubaneswar, Odisha, India.
5. Overseas Secretary, Orissa Information Technology Society (OITS), Bhubaneswar, Odisha, India, 2006–2012.

Journal Editorship:

6. **Editor-in-Chief (EiC)**, IEEE Consumer Electronics Magazine, 2016–present.
7. **Founding Editor-in-Chief (EiC)**, VLSI Circuits and Systems Letter, IEEE-CS TCVLSI, 2015–present.
8. Steering Committee Member, IEEE Transactions on Big Data (TBD), 2018–present.
9. Associate Editor, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2016–present.
10. Associate Editor, ACM Journal on Emerging Technologies in Computing Systems (JETC), 2016–present.
11. Associate Editor, IEEE Transactions on Nanotechnology (TNANO), 2017–present.
12. Associate Editor, IET Circuits, Devices and Systems (CDS), 2014–present.
13. Associate Editor, Elsevier The VLSI Integration Journal, 2014–present.
14. Associate Editor, ASP Journal of Low Power Electronics (JOLPE), 2011–present.
15. Senior Editor, IEEE Consumer Electronics Magazine, 2015–2016.
16. Associate Editor, Elsevier International Journal on Computers and Electrical Engineering, 2010–2014.
17. Guest Editor, "Circuit and System Design Automation for Internet of Things", IEEE Transactions on Computer Aided Design (TCAD), Volume 37, Issue 1, January 2018.
18. Guest Editor, "Nanoelectronic Devices and Circuits for Next Generation Sensing and Information Processing", IEEE Transaction on Nanotechnology (TNANO), Volume 16, Issue 3, May 2017.
19. Guest Editor, "Hardware Assisted Techniques for IoT and Bigdata Applications", Elsevier The VLSI Integration Journal, 2017.
20. Guest Editor, "Nanoelectronic Circuit and System Design Methods for Mobile Computing Era", ACM Journal on Emerging Technologies in Computing Systems (JETC), Volume 13, Issue 2, March 2017.
21. Guest Editor, "Security and Reliability Aware System Design for Mobile Computing Systems", IEEE Access Journal (Access), Volume 4, 2016.
22. Guest Editor, "Circuit and System Design Methodologies for Emerging Technologies", IEEE Transactions on Emerging Topics in Computing (TETC), Vol. 3, No. 4, October-December 2015.
23. Guest Editor, "Advanced Techniques for Efficient Electronic System Design", Springer Circuits, Systems, and Signal Processing Journal (CSSP), Volume 32, Issue 6, December 2013.
24. Guest Editor, "Special Issue on Design Methodologies for Nanoelectronic Digital and Analog Circuits", IET Circuits, Devices, & Systems Journal (CDS), Volume 7, Issue 5, September 2013.
25. Guest Editor, "Special Section on New Circuit and Architecture Level Solutions for Multidiscipline Systems", ACM Journal on Emerging Technologies in Computing Systems (JETC), Volume 8, Issue 3, August 2012.
26. Guest Editor, "Special Issue on Power, Parasitics, and Process-Variation (P3) Awareness in Mixed-Signal Design", ASP Journal of Low Power Electronics (JOLPE), Volume 8, Issue 3, June 2012.
27. Guest Editor, "Special Issue on Circuits and Systems for Real-Time Security and Copyright Protection of Multimedia", Elsevier International Journal on Computers and Electrical Engineering, Volume 35, Issue 2, March 2009.

Conference Chairs:

28. **Founding Steering Committee Chair**, IEEE International Symposium on Nanoelectronic and Information Systems (iNIS), 2015–Present.
29. **Steering Committee Vice-Chair**, IEEE-CS Annual Symposium on VLSI (ISVLSI), 2016–Present.

30. **Steering Committee Vice-Chair**, OITS International Conference on Information Technology (ICIT), 2017–Present.
31. **General Chair**, 36th IEEE International Conference on Consumer Electronics (ICCE), January 12-14, 2018, Las Vegas, USA.
32. Media Outreach Chair, 3rd IEEE Canada International Humanitarian Technology Conference (IHTC), July 20–22, 2017, Toronto, Canada.
33. Special Session Chair, 16th IEEE-CS Annual Symposium on VLSI (ISVLSI), July 3-5, 2017, Bochum, Germany.
34. Track Chair, "Consumer Healthcare & Systems", 35th IEEE International Conference on Consumer Electronics (ICCE), January 8-11, 2017, Las Vegas, USA.
35. **General Chair**, 2nd IEEE International Symposium on Nanoelectronic and Information Systems (iNIS), December 19-21, 2016, Gwalior, India.
36. **General Chair**, 15th International Conference on Information Technology (ICIT), December 22-24, 2016, Bhubaneswar, India.
37. Session Chair, "Electromagnetic Compatibility", 6th IEEE International Conference on Consumer Electronics - Berlin (ICCE-Berlin), September 5-7, 2016, Berlin, Germany.
38. **Program Chair**, 15th IEEE-CS Annual Symposium on VLSI (ISVLSI), July 11-13, 2016, Pittsburgh, PA.
39. **Founding General Chair**, 1st IEEE International Symposium on Nanoelectronic and Information Systems (iNIS), December 21-23, 2015, Indore, India.
40. Publication Chair, 14th International Conference on Information Technology (ICIT), December 21-23, 2015, Bhubaneswar, India.
41. **Program Chair**, 14th IEEE-CS Annual Symposium on VLSI (ISVLSI), July 8-10, 2015, Montpellier, France.
42. Track Chair, "VLSI Design", 25th ACM Great Lakes Symposium on VLSI (GLSVLSI), May 20-22, 2015, Pittsburgh, PA.
43. **General Chair**, 13th International Conference on Information Technology (ICIT), December 22-24, 2014, Bhubaneswar, India.
44. **General Chair**, 13th IEEE-CS Annual Symposium on VLSI (ISVLSI), July 9-11, 2014, Tampa, FL.
45. Session Chair, "Analog Design", 24th ACM Great Lakes Symposium on VLSI (GLSVLSI), May 21-23, 2014, Houston, TX.
46. Track Chair, "VLSI Design", 24th ACM Great Lakes Symposium on VLSI (GLSVLSI), May 21-23, 2014, Houston, TX.
47. **General Chair**, 11th IEEE-CS Annual Symposium on VLSI (ISVLSI), May 19-21, 2012, Amherst, MA.
48. Track Co-Chair, "Design for Manufacturability/Yield & Quality (DFQ)", 13th International Symposium on Quality Electronic Design (ISQED), March 19-21, 2012, Santa Clara, CA.
49. Track Chair, "CAD for Analog and Mixed Signal Circuits", 25th International Conference on VLSI Design (VLSID), January 7-11, 2012, Hyderabad, India.
50. Publication Chair, 2nd International Symposium on Electronic System Design (ISED), December 19-21, 2011, Kochi, India.
51. Session Chair, "Design Methodologies for CMOS and Beyond", 12th International Symposium on Quality Electronic Design (ISQED), March 14-16, 2011, Santa Clara, CA.
52. Track Co-Chair, "Design for Manufacturability/Yield & Quality (DFQ)", 12th International Symposium on Quality Electronic Design (ISQED), March 14-16, 2011, Santa Clara, CA.
53. **Founding Steering Committee Chair**, International Symposium on Electronic System Design (ISED), 2010–2011.
54. **Founding Program Chair**, 1st International Symposium on Electronic System Design (ISED), December 20-22, 2010, Bhubaneswar, India.
55. Session Chair, "Poster Session II", 20th ACM Great Lakes Symposium on VLSI (GLSVLSI), 2010, 18th May, 2010, Providence, RI.
56. Session Chair, "SRAM Manufacturability", 11th International Symposium on Quality Electronic Design

(ISQED), March 22-24, 2010, San Jose, CA.
57. Session Chair, "Low-Power Architecture", 23rd International Conference on VLSI Design (VLSID), 6th January 2010, Bangalore, India.
58. Publication Chair, 12th International Conference on Information Technology (ICIT), December 21-24, 2009, Bhubaneswar, India.
59. Session Chair, 12th International Conference on Information Technology (ICIT), 24th December 2009, Bhubaneswar, India.
60. Session Chair, International Symposium on Biologically Inspired Computing And Applications (BICA), 22nd December 2009, Bhubaneswar, India.
61. Publication Chair, 8th IEEE-CS Annual Symposium on VLSI (ISVLSI), May 13-15, 2009, Tampa, FL.
62. Session Chair, "Process Variation", 10th International Symposium on Quality Electronic Design (ISQED), March 16-18, 2009, San Jose, CA.
63. Session Co-Chair, "Low Voltage Design", 10th International Symposium on Quality Electronic Design (ISQED), March 16-18, 2009, San Jose, CA.
64. Session Chair, "SoC Verification", 22nd International Conference on VLSI Design (VLSID), January 5-9, 2009, New Delhi, India.
65. Session Chair, "Networks - 1" and "Database and Web Technology", 11th International Conference on Information Technology (ICIT), December 17-20, 2008, Bhubaneswar, India.
66. Track Chair, "Architecture and Programming Systems", 11th International Conference on Information Technology (ICIT), December 17-20, 2008, Bhubaneswar, India.
67. Session Chair, "System-Level Testing, Verification and Design" and "Poster Session 2", 18th ACM Great Lake Symposium on VLSI (GLSVLSI), May 4-6, 2008, Orlando, FL.
68. Session Chair, "Low Power - I", 21st International Conference on VLSI Design (VLSID), January 4-8, 2008, Hyderabad, India.
69. Publicity Chair, 10th International Conference on Information Technology (ICIT), December 18-20, 2007, Bhubaneswar, India.
70. Publicity Chair, 2nd International Conference on Web Engineering and Application (ICWA), December 14-16, 2007, Bhubaneswar, India.
71. Publicity Chair, International Conference on IP Multimedia Subsystems Architecture and Applications (IMSAA-2007), December 6-8, 2007, Bangalore, India.
72. Session Chair, "Security and Digital Rights Management", IEEE International Symposium on Consumer Electronics (ISCE), 20-23 June 2007, Dallas, TX.
73. **Program Chair**, 9th International Conference on Information Technology (ICIT), December 18-26, 2006, Bhubaneswar, India.
74. Session Chair, "Internet, Network Protocol and Architecture", 8th International Conference on Information Technology (CIT), December 20-23, 2005, Bhubaneswar, India.

Proposal Panelist:

75. Panelist, National Science Foundation (NSF), Division of Electrical, Communications and Cyber Systems (ECCS).
76. Panelist, National Science Foundation (NSF), Division of Computer and Network Systems (CNS), Secure and Trustworthy Cyberspace (SaTC).
77. Panelist, National Science Foundation (NSF), Division of Computer and Network Systems (CNS), Cyber-Physical Systems (CPS).
78. Reviewer, National Science Foundation (NSF), Office of Cyberinfrastructure, Strategic Technologies for Cyberinfrastructure (STCI).
79. Invited Researcher, Workshop on NSF Nanoelectronics: Circuits, Systems, and CAD Tools, October 2007 to review the impacts of the Emerging Models and Technologies for Computation (EMT) Program of National Science Foundation (NSF) on various fronts.

80. Reviewer, National Center of Science and Technology Evaluation, Kazakhstan.
81. Reviewer, Division of Physics and applied Mathematics, Israeli Ministry of Science, Technology and Space.
82. Reviewer, The Austrian Science Fund (FWF), Natural and Technical Sciences.
83. Reviewer, U.S. Civilian Research & Development Foundation (CRDF, http://www.crdf.org/).

Conference Committees:

84. Executive Committee Member, IEEE International Conference on Consumer Electronics (ICCE), 2017–Present.
85. Steering Committee Member, IEEE-CS Annual Symposium on VLSI (ISVLSI), 2015–Present.
86. Steering Committee Member, OITS International Conference on Information Technology (ICIT), 2015–Present.
87. Program Committee Member, IEEE International Conference on Computer Design (ICCD) – 2016, 2015, 2014, 2013, 2012.
88. Program Committee Member, International Conference on VLSI Design (VLSID) – 2015, 2013, 2011, 2010, 2009, 2008.
89. Program Committee Member, ACM Great Lake Symposium on VLSI (GLSVLSI) – 2016, 2013, 2012, 2011, 2010, 2009, 2008.
90. Program Committee Member, International Symposium on Quality Electronic Design (ISQED) – 2015, 2014, 2013, 2010, 2009.
91. Program Committee Member, Asia Symposium on Quality Electronic Design (ASQED) – 2015, 2014, 2013, 2012, 2011, 2010, 2009.
92. Program Committee Member, IEEE-CS Annual Symposium on VLSI (ISVLSI) – 2015, 2014, 2011, 2010, 2009.
93. Student Design Contest Judge, Design Automation Conference – 2010, 2009, 2008, 2007, 2006, 2005.
94. Program Committee Member, IEEE/IFIP International Conference on VLSI and System-on-Chip (VLSI-SoC) – 2010.
95. Program Committee Member, International Conference on Intelligent Information Hiding and Multimedia Signal Processing (IIH-MSP) – 2013, 2012, 2011, 2010, 2009, 2008, 2007.
96. Program Committee Member, IEEE Dallas Circuits and Systems Workshop (DCAS) – 2008, 2007.
97. Program Committee Member, VLSI Design and Test Symposium (VDAT) - 2014, 2012.
98. The first Annual National Aspire Science Competition Judge, The Texas Academy of Mathematics and Science, 2011, http://www.aspiresciencecompetition.com/.
99. Program Committee Member, The 6th International Workshop on Unique Chips and Systems (UCAS-6), December 4, 2010, Atlanta, GA, USA.
100. Program Committee Member, International Conference on Computer Technology (ICCT-2010), December 3-5, 2010, Bhubaneswar, India.
101. Program Committee Member, International Conference on VLSI Design and Communication Systems (ICVLSICOM-10), January 8-10, 2010, Chennai, India.
102. Program Committee Member, International Conference on IP Multimedia Subsystems Architecture and Applications (IMSAA) – 2009, 2008, 2007.
103. Program Committee Member, 10th International Conference on Information Technology (ICIT), December 18-26, 2007, Bhubaneswar, India.
104. Technical Review Committee, Global Signal Processing Expo & Conference (GSPx) 2005.

Journal or Conference Reviewer:

105. ACM Journal on Emerging Technologies in Computing Systems (JETC)
106. ACM Transactions on Design Automation of Electronic Systems (TODAES)
107. ACM Transactions on Information Systems (TIS)

108. ASP Journal of Low Power Electronics (JOLPE)
109. Electronics and Telecommunications Research Institute (ETRI) Journal, Korea
110. Elsevier Applied Mathematical Modelling (APM)
111. Elsevier International Journal of Computers and Electrical Engineering
112. Elsevier Integration - The VLSI Journal
113. Elsevier Journal on Signal Processing
114. Elsevier Journal on Signal Processing: Image Communication
115. Elsevier Journal of Systems and Software (JSS)
116. Elsevier Microprocessors and Microsystems Journal
117. EURASIP Journal on Advances in Signal Processing
118. EURASIP Journal on Applied Signal Processing
119. IEEE Security & Privacy
120. IEEE Transactions on CAD of Integrated Circuits and Systems (TCAD)
121. IEEE Transactions on Circuits and Systems for Video Technology (TCSVT)
122. IEEE Transactions on Circuits and Systems Part II (TCAS II)
123. IEEE Transactions on Computers (TC)
124. IEEE Transactions on Industrial Electronics (TIE)
125. IEEE Transactions on Information Forensics and Security (TIFS)
126. IEEE Transactions on Multimedia (TMM)
127. IEEE Transactions on Nanotechnology (TNANO)
128. IEEE Transactions on Semiconductor Manufacturing (TSM)
129. IEEE Transactions on VLSI Systems (TVLSI)
130. IET Circuits, Devices & Systems (CDS)
131. IET Computers & Digital Techniques (CDT)
132. Springer Circuits, Systems & Signal Processing Journal (CSSP)
133. Springer Journal of Multimedia Tools and Applications
134. Oxford University Press The Computer Journal
135. Taylor & Francis International Journal of Electronics (IJE)
136. International Conference on Advanced Computing and Communications (ADCOM) - 2009
137. International Symposium on Biologically Inspired Computing And Applications (BICA) - 2009
138. 12th International CSI Computer Conference (CSICC'07)
139. ACM/IEEE Design Automation Conference (DAC) - 2003, 2004, 2005, 2006, 2007, 2011, 2013, 2014, 2015
140. IEEE International Conference on Computer Design (ICCD) - 2005, 2010
141. IEEE International Conference on VLSI Design - 2003, 2004, 2005, 2006, 2008, 2009
142. IEEE International Midwest Symposium on Circuits and Systems (MWSCAS) - 2008, 2011, 2013
143. IEEE International Symposium on Circuits and Systems (ISCAS) - 2006, 2010, 2011, 2014
144. Memory Performance: Dealing with Applications, Systems, and Architecture Workshop - 2004
145. PCEA- IFToMM International Conference: Recent Trends in Automation & its Adaptation to Industries (PICA) - 2006
146. VLSI Design and Test Workshops, India - 2003, 2004

UNIVERSITY or DEPARTMENTAL SERVICES

Academic Year: Fall 2016 - Spring 2017

1. Served in the Faculty Senate of the University of North Texas.
2. Served in the Faculty Development Leave Committee of the University of North Texas.
3. Participated in the commencement ceremonies of University of North Texas.
4. Served in the Faculty Council of the College of Engineering, University of North Texas.
5. Participated in license purchase and maintenance of Electronic Design Automation (EDA) softwares,

including Cadence and Mentor Graphics which are used by various departments in the College of Engineering at the University of North Texas.
6. Served in the Personnel Affairs Committee of the Department of Computer Science and Engineering, University of North Texas.
7. Served as the course coordinator for the VLSI related courses of computer engineering program of the Department of Computer Science and Engineering, University of North Texas.

Academic Year: Fall 2015 - Spring 2016

8. Represented the Department of Computer Science and Engineering at the Electrical and Computer Engineering Department Head Association (ECEDHA) Conference 2016, San Diego, CA.
9. Served in the Faculty Senate of the University of North Texas.
10. Served in the Faculty Development Leave Committee of the University of North Texas.
11. Participated in the commencement ceremonies of University of North Texas.
12. Served in the Faculty Council of the College of Engineering, University of North Texas.
13. Served in the Personnel Affairs Committee of the Department of Engineering Technology, University of North Texas.
14. Served in the Personnel Affairs Committee of the Department of Computer Science and Engineering, University of North Texas.
15. Served in the undergraduate studies committee of the Department of Computer Science and Engineering, University of North Texas.
16. Participated in license purchase and maintenance of Electronic Design Automation (EDA) softwares, including Cadence and Mentor Graphics which are used by various departments in the College of Engineering at the University of North Texas.
17. Served as the course coordinator for the VLSI related courses of computer engineering program of the Department of Computer Science and Engineering, University of North Texas.

Academic Year: Fall 2014 - Spring 2015

18. Served in the Personnel Affairs Committee of the Department of Computer Science and Engineering, University of North Texas.
19. Served in the undergraduate studies committee of the Department of Computer Science and Engineering, University of North Texas.
20. Chaired the ad-hoc committee on undergraduate Computer Engineering curriculum of the Department of Computer Science and Engineering, University of North Texas.
21. Served as the course coordinator for the VLSI related courses of computer engineering program of the Department of Computer Science and Engineering, University of North Texas.
22. Participated in license purchase and maintenance of Electronic Design Automation (EDA) softwares, including Cadence and Mentor Graphics which are used by various departments in the College of Engineering at the University of North Texas.
23. Participated in the commencement ceremonies of University of North Texas.

Academic Year: Fall 2013 - Spring 2014

24. Served in the Personnel Affairs Committee of the Department of Computer Science and Engineering, University of North Texas.
25. Served in the graduate studies committee of the Department of Computer Science and Engineering, University of North Texas.
26. Served as the course coordinator for the VLSI related courses of computer engineering program of the Department of Computer Science and Engineering, University of North Texas.

27. Participated in license purchase and maintenance of Electronic Design Automation (EDA) softwares, including Cadence and Mentor Graphics which are used by various departments in the College of Engineering at the University of North Texas.
28. Participated in the commencement ceremonies of University of North Texas.

Academic Year: Fall 2012 - Spring 2013

29. Served on the Oversight Committee on the Core Curriculum of University of North Texas.
30. Participated in the commencement ceremonies of University of North Texas.
31. Served in the Personnel Affairs Committee of the Department of Computer Science and Engineering, University of North Texas.
32. Served in the graduate studies committee of the Department of Computer Science and Engineering, University of North Texas.
33. Participated in license purchase and maintenance of Electronic Design Automation (EDA) softwares, including Cadence and Mentor Graphics which are used by various departments in the College of Engineering at the University of North Texas.
34. Served as the course coordinator for the VLSI related courses of computer engineering program of the Department of Computer Science and Engineering, University of North Texas.

Academic Year: Fall 2011 - Spring 2012

35. Represented the delegation of University of North Texas who signed a memorandum of understanding with Indian Institute of Technology Bhubaneswar (IITBBS) and International Institute of Information Technology Bhubaneswar (IIITBBS) for collaboration in research and education.
36. Served on the Oversight Committee on the Core Curriculum of University of North Texas.
37. Participated in the commencement ceremonies of University of North Texas.
38. Served as the Elected Chair of the Personnel Affairs Committee of the Department of Computer Science and Engineering, University of North Texas.
39. Served as an elected member of the executive committee of the Department of Computer Science and Engineering, University of North Texas.
40. Participated in license purchase and maintenance of Electronic Design Automation (EDA) softwares, including Cadence and Mentor Graphics which are used by various departments in the College of Engineering at the University of North Texas.
41. Served as the course coordinator for the VLSI related courses of computer engineering program of the Department of Computer Science and Engineering, University of North Texas.

Academic Year: Fall 2010 - Spring 2011

42. Represented the delegation of University of North Texas who signed a memorandum of understanding with Indian Institute of Science, Bangalore, India, for collaboration in research and education.
43. Participated in the commencement ceremonies of University of North Texas.
44. Served as the Elected Chair of the Personnel Affairs Committee of the Department of Computer Science and Engineering, University of North Texas.
45. Served as an elected member of the graduate studies committee of the Department of Computer Science and Engineering, University of North Texas.
46. Participated in license purchase and maintenance of Electronic Design Automation (EDA) softwares, including Cadence, Synposys, and Mentor Graphics which are used by various departments in the College of Engineering at the University of North Texas.
47. Served as the course coordinator for the VLSI related courses of computer engineering program of the Department of Computer Science and Engineering, University of North Texas.

Academic Year: Fall 2009 - Spring 2010

48. Served as an elected member of executive committee of the Department of Computer Science and Engineering, University of North Texas.
49. Served in the graduate studies committee of the Department of Computer Science and Engineering, University of North Texas.
50. Served as the course coordinator for the VLSI related courses of computer engineering program of the Department of Computer Science and Engineering, University of North Texas.
51. Participated in the commencement ceremonies of University of North Texas.

Academic Year: Fall 2008 - Spring 2009

52. Served as an elected member of executive committee of the Department of Computer Science and Engineering, University of North Texas.
53. Served in the graduate studies committee of the Department of Computer Science and Engineering, University of North Texas.
54. Served as the course coordinator for the VLSI related courses of computer engineering program of the Department of Computer Science and Engineering, University of North Texas.
55. Participated in SACS (Southern Association of Colleges and Schools) accreditation of the Department of Computer Science and Engineering, University of North Texas.
56. Participated in the commencement ceremonies of University of North Texas.

Academic Year: Fall 2007 - Spring 2008

57. Served in the graduate studies committee of the Department of Computer Science and Engineering, University of North Texas.
58. Served in the faculty search committee of the Department of Computer Science and Engineering, University of North Texas.
59. Served as the course coordinator for the VLSI related courses of computer engineering program of the Department of Computer Science and Engineering, University of North Texas.
60. Participated in ABET (Accreditation Board for Engineering and Technology) accreditation of Computer Engineering program of the Department of Computer Science and Engineering, University of North Texas.
61. Participated in the commencement ceremonies of University of North Texas.

Academic Year: Fall 2006 - Spring 2007

62. Served in the graduate studies committee of the Department of Computer Science and Engineering, University of North Texas.
63. Served as an elected member of executive committee of the Department of Computer Science and Engineering, University of North Texas.
64. Served as the course coordinator for the VLSI related courses of computer engineering program of the Department of Computer Science and Engineering, University of North Texas.
65. Participated in the commencement ceremonies of University of North Texas.

Academic Year: Fall 2005 - Spring 2006

66. Served as an elected member of executive committee of the Department of Computer Science and Engineering, University of North Texas.
67. Served in the graduate studies committee of the Department of Computer Science and Engineering, University of North Texas.

68. Served in the graduate studies subcommittee on Southern Association of Colleges and Schools (SACS) of the Department of Computer Science and Engineering, University of North Texas, to correct and modify learning outcome and assessment tools for computer engineering and computer science graduate programs.
69. Participated in building CAD, VLSI, and Digital Systems Laboratory, Department of Electrical Engineering, University of North Texas, which is major thrust for computer engineering program. The laboratory has modern state-of-the-art hardware facilities to meet the computational demands of VLSI design related research and education through the College of Engineering. The facilities include a Sunfire v440 server, an HP Dual Xeon Server, Sun Opteron workstations, and Sunblade workstations, all are connected to a 3-TB RAID storage array with open and licensed CAD software to enable the design, simulation, and testing of a variety of electronic chip designs.
70. Participated in establishing FPGA teaching laboratory in the Department of Computer Science and Engineering, University of North Texas, for teaching of courses like logic design, system design and reconfigurable logic etc. Besides sharing the technical know-how in bringing the laboratory to serviceable shape, I contributed five Xilinx boards that I received from Xilinx as a gift.
71. Participated in the development of an interdisciplinary research group, "Nanoscale Design and Test Research and Education Group (NREG)", in the College of Engineering, University of North Texas, engaged in cutting edge research and education in nanoscale VLSI design and testing.
72. Served as the course coordinator for the VLSI related courses of computer engineering program of the Department of Computer Science and Engineering, University of North Texas.
73. Participated in the commencement ceremonies of University of North Texas.

Academic Year: Fall 2004 - Spring 2005

74. Served in the graduate studies committee of the Department of Computer Science and Engineering, University of North Texas.
75. Served in the faculty search committee of the Department of Computer Science and Engineering, University of North Texas.
76. Established a new research laboratory, "NanoSystem Design Laboratory (NSDL)", homepage: `http://nsdl.cse.unt.edu`, at the Department of Computer Science and Engineering, University of North Texas.
77. Participated in the development of Computer Engineering curriculum as a founding Computer Engineering faculty of the Department of Computer Science and Engineering, University of North Texas.
78. Participated in the commencement ceremonies of University of North Texas.

NEWS ARTICLES ON MY RESEARCH/EDUCATION/OUTREACH ACTIVITIES

Please refer: http://www.smohanty.org/News.html

RESEARCH STATEMENT

My research is on Smart Electronic Systems. The key aspects of the smart electronics are Energy-Smart, Security-Smart, and Response-Smart. Energy-Smart ensures that energy consumption of consumer electronics is minimal for longer battery life. Security-Smart deals with the security/protection of electronics systems as well as that of the information/media that these systems capture, process, or store. Response-Smart refers to accurate sensing, intelligent processing, and fast actuation/response. The research can be classified into the following inter-related categories:

(1) Consumer Electronics for Smart Cities
(2) Application-Specific Things for Efficient Edge Computing
(3) Methodologies for Digital and Mixed-Signal Hardware

Breadth and depth are essential in order to establish a sustainable, active, and high impact research program with strong scholastic output. Depth in research is necessary to explore the underlying fundamental principles and breadth is needed to broaden knowledge and skills so as to remain vigilant and versatile for the ever changing science and technology trends. While individual identity is crucial, interdepartmental, interuniversity, and university-industrial collaborations are essential for high-impact cutting-edge low-power high-performance secure electronic systems research that essentially deals with the fastest growing technologies humankind has known. External funding is very much essential for a high quality, sustainable and productive research program. Funding is used to attract high-quality students and hiring researchers, which is vital for research productivity and output. Various Federal agencies and departments such as the National Science Foundation (NSF), Air Force Research, Department of Energy, and Defense Advanced Research Projects Agency (DARPA) provide funding for research. Moreover, it is of importance to approach various industries for their support and collaboration directly as well as through consortiums, such as the Semiconductor Research Corporation (SRC).

A. Description of Current Research Interests

(1) Consumer Electronic Systems for Smart Cities

The objective of this research is to explore application specific hardware and software based consumer electronic systems which can be deployed in smart cities. In order to cope up with constrained resources with increased population growth, smart cities with smart technology, smart healthcare, smart grids, smart transportation, smart buildings, and smart communications, are envisioned. The Internet of Things (IoT) which refers to the interconnection of "things" including buildings, energy-grids, transport-systems, and health-care system, which need not be inherently smart, to make them smart through the use of sensors, and information and communication technology (ICT) is the key for building smart cities. IoT frameworks may consist of various diverse components including sensors, electronics, communication networks, middleware, firmware, and software which enable the interactions of many diverse types of things for providing increasingly smart, reliable and secure services. Thus, the realization of IoT systems for smart cities needs the combination of several factors such as energy efficiency, high performance, reliability, security, privacy, and flexibility, which can be drivers of rigorous academic and industrial research. These factors impose significant circuit and system design challenges while keeping the design cost as minimal as possible and meeting the time to market demand. For example, a video processing unit needs to be energy efficient due to the battery source while at the same time needs to have high performance to process high definition video. With the increasing complexity of IoT design, the full-custom, semi-custom, and automatic design methodologies can be explored based on the complexity, time-to-market, and design budgets. At the same time, there is an immediate need for suitable and effective, electronic design automation techniques for the design and implementation of the next generation IoT systems. The research for efficient IoT, may involve circuit and system level challenges targeting specific application domains, e.g. healthcare and, transportation. The IoT system will use various sensors, computing platforms (e.g. smart phones, tablets, personal computers, and servers), middleware, firmware, and software.

(2) Methodologies for Nanoelectronic Digital and Mixed-Signal Systems

The objective of this research is to explore models, metamodels, optimization techniques, and design flows for ultra-fast and yet accurate design of digital and analog/mixed-signal (AMS) integrated circuits and systems. A typical consumer electronic system is essentially built as an Analog/Mixed-Signal System-on-a-Chip (AMS-SoC) in which analog and digital portions containing thousands-to-billion nanoelectronic devices are integrated on the same die for cost and performance tradeoffs. Nanoelectronic devices including memristors, graphene transistors, and tunnel transistors have shown significant promise for ultra-low power and very-high speed circuits and systems. To make the situation worse for designers of such high complexity systems the time-to-market has been reduced significantly. In such a situation, design methodology frameworks are more important in order to produce error free AMS-SoCs on time. In this research, new modeling techniques are investigated such that ultra-fast AMS-SoC design exploration can be performed using these models. In particular, techniques for metamodel (model of netlists) generation are investigated. Different types of metamodels are explored for various figures-of-merits (FoMs) of diverse AMS-SoC components. It may be noted that metamodels are not macromodels; the terms "metamodels" and "macromodel" are very distinct even though the two terms are often used in the literature interchangeably. A macromodel is simply a reduced complexity (order) representation of the circuit but is still a netlist, necessitating the use of an analog (SPICE) simulator. The proposed metamodel (which is a mathematical algorithm) is a language and simulator independent model of the original model/netlist (hence the term meta). The simulation time for locking of a phase-locked loop (PLL) over the actual circuit (i.e. full-blown parasitic-aware netlist) is of the order of days to weeks; while the simulation of the PLL over metamodels reduces to minutes! The FoMs of AMS-SoC components for which individual metamodels are generated include power, leakage, frequency, phase-noise, and locking time. In this research, new (metamodeling-based) design methodologies are investigated for AMS-SoC component design optimization. Research also includes integrating the metamodels in the Verilog-AMS and Simscape languages such that AMS-SoC design exploration with layout-level accuracy can be performed. Digital integrated circuits continue to remain the main work horse of AMS-SoC. Hence research also focuses on process-variation aware, power-aware, and security-aware high-level synthesis (HLS) for the realization of efficient register-transfer-level (RTL) description of these digital components. For optimization purposes, various biology and culture inspired algorithms, including bee-colony optimization and memetic algorithms, are investigated as they can handle a large number of parameters and converge rapidly.

(3) VLSI Architectures for Multimedia Signal Processing

The objective of this research is to develop hardware-amenable algorithms and architectures for multimedia data security and copyright protection and to build systems with built-in low-cost, low-power, and real-time digital right management (DRM) facilities following the algorithm-to-board-to-silicon (ABS) developmental approach. For secure, efficient and copyright protected data transmission, there is a need for the following: (1) watermarking techniques for copyright protection of digital video, (2) scrambling techniques for access control, (3) encryption to ensure secured transmission of data, and to also ensure the secure transmission of the scrambling and watermarking keys (if any), and (4) compression techniques to reduce the data transmission rate. Hardware assisted DRM systems that include encryption, watermarking, or scrambling, can be cost effective, real-time, high performance, and power efficient, providing transmission of data with high security and copyright protection. The objective of this research is to introduce hardware amenable algorithms, build secure architectures, and develop complete systems, such as digital cameras, network processors, and graphics processing units, with built-in DRM capabilities. The complete system development will involve FPGA-custom-IC hybrid circuit design, CPU-GPU multi-core, and digital-analog/mixed-signal circuit/system design for low-cost and real-time objectives. Design of low-power high-performance circuits and systems for various applications, like image compression, video compression, biometrics, character recognition, and language translation, are also being considered.

B. Research Accomplishments and Significance

The significance of my research is evident from the funded projects, peer-reviewed journal papers, peer-reviewed conference papers, patents, and citations from worldwide peers. The significant features of my research so far are the following:

1. New systems for *secure contactless payment* with or without mobile phones (CEM-2017-Apr, CEM-2017-Jan).
2. An earliest *Trojan-secured architecture synthesis* method for trusted consumer electronics hardware (TCAD-2017-Apr).
3. Low-cost architecture synthesis methods for *intellectual property (IP) protection* consumer electronics digital hardware (TCAD-2017, CDT-2017-Mar, ISCAS-2016).
4. First ever energy-efficient, secure *Better Portable Graphics (BPG)* compression architecture for trusted, high-quality, high-speed image and video communications in Internet-of-Things (IoT) (IEEE-Access-2016, ISVLSI-2016, iNIS-2015).
5. Kriging metamodel based *fast and accurate methods for process variation aware* AMS design optimization (ISQED-2015, TVLSI-2014-Apr, ISVLSI-2014, ISQED-2014).
6. iVAMS or *intelligent metamodel-integrated Verilog-AMS* for circuit-accurate system-level simulation (ASAP-2013).
7. *Layout-aware metamodel assisted ultrafast design flows* for AMS-SoC component layout optimization that iterates over the metamodels instead of netlists to achieve 10,000× speedup and needs exactly two layout steps (TSM-2014-Feb, TSM-2012-Feb, JOLPE-2012-Jun, VLSID-2012, ISQED-2011).
8. A *fast single-manual iteration design flow* for AMS-SoC component layout optimization that needs exactly two layout steps (VLSID-2010, TVLSI-2009-Sep).
9. An *Universal Voltage-Level Shifter (ULS)* or Universal Voltage-Level Converter (ULC) design that performs signal up-conversion, down-conversion, passing, and blocking for reconfiguration and energy efficiency of AMS-SoC (Springer-ALOG-2012-Aug, JETC-2010-Jun, ISQED-2009, ISQED-2008).
10. First ever *simultaneous consideration of power, parasitics, process-variations, and performance (P4)* in voltage controlled oscillator (VCO) design (TVLSI-2009-Sep, GLSVLSI-2009, and ISQED-2008).
11. First ever study to correlate the *impact of gate-oxide leakage on center frequency* of a voltage controlled oscillator (VCO) (MEJ-2009-Jan).
12. First ever *process variation aware optimization* during high-level synthesis (HLS) (VLSID-2007).
13. First ever high-level synthesis *(HLS) addressing gate leakage optimization* (CDT-2008-March, VLSID-2006 and IWLS-2005).
14. Introduction of *secure digital camera (SDC)* with built-in watermarking and encryption capabilities (SOCC-2006, TVLSI-2005-July/August, VLSID-2004).
15. Introduction of a novel memory allocator called *hybrid memory allocator* that uses software and hardware co-design to improve the speed of the software allocator for faster and low cost system implementation (IEEE-CAL-2006 July/December and ISCA-PDCS-2006).
16. Introduction of a novel metric called *effective tunneling capacitance* to quantify the transient gate leakage current in nano-CMOS (ICCD-2006 and ISCAS-2006).
17. Introduction of a new approach called *dual dielectric of dual thickness (DKDT)* for the reduction of gate tunneling current in sub-65nm CMOS technology circuits. This research brought the non-classical nano-CMOS technology (transistors made of non-SiO_2 dielectric) into automatic circuit synthesis flow (ICCD-2005 and ISQED-2006).
18. Introduction of a methodology for *peak power* optimization during behavioral synthesis (TCAS-I-2005-June, GLSVLSI-2003, and ISVLSI-2003).
19. Introduction of *fast analytical models for gate leakage* calculation of behavioral datapath components (VLSID-2006, IWLS-2005, and ISVLSI-2005).
20. Exploration of a new design approach called *dynamic frequency clocking* (frequency scaling) along with

multiple supply voltages during behavioral synthesis (TODAES-2005-April and VLSID-2003).

21. Design of the *lowest power consuming watermarking chip* available at present which consisted of $1.3M$ transistors and consumes only $0.3mW$ of power. This is also the first ever watermarking chip with both visible and invisible watermarking functionalities in the DCT domain (TCAS-II-2006-May and VLSID-2005).
22. A novel approach for simultaneous minimization of various forms of dynamic power datapath circuit, through the minimization of a measure, *cycle power function (CPF)* (TODAES-2006-January, TVLSI-2004-June, VLSID-2004, and VLSID-2003).
23. Design of the first ever *visible watermarking chip* for copyright protection of publicly available images (TVLSI-2005-July/August and VLSID-2004).
24. A novel approach for power fluctuation minimization of datapath circuits using a new metric called *mean power gradient (MPG)* (ICCD-2003).
25. Introduction of a *secure JPEG codec* with built-in watermarking capability (SIPS-2003).
26. Introduction of one of the earliest *visible watermarking algorithms*, an DCT domain image adaptive visible-transparent watermarking (ICME-2000).
27. Introduction of first ever multiple watermarking scheme, called *dual watermarking* that uses an invisible watermark with visible watermark (ACMMM-1999).

C. Research Citations

My research is well-received by the world-wide peers with continuous citations. A tentative list of citations from Google Scholar can be obtained from the following URL: http://scholar.google.com/citations?user=G0uvNwsAAAAJ&hl=en.

TEACHING STATEMENT

Training other individuals is an integral part of research. I enjoy teaching at the graduate and undergraduate levels and carry it out well. Moreover, I believe that to teach is to learn twice. In my opinion learning should be a uniform and continuous process with more student-teacher interaction. My goal as an instructor is to present relevant material as clearly as possible. I place a lot of emphasis on fundamentals and basic concepts and cover them in depth. I do not rush through my syllabus simply to cover all the topics. I focus on learning outcomes; I ask and expect for questions to be asked in order to resolve learning difficulties of students.

I recommend that students exercise their own powers of critical problem solving, creativity, analysis, and synthesis or data evaluation in even the most structured lectures. I insist that the students should keep abreast with present day technology. Developing skills with tools, concepts and designing are emphasized in my lectures. I motivate students to innovate on their own and contribute to the future technology. Hence I make working on a term-paper and mini-project a necessary part of my courses. I insist on hands-on approach. Consequently, much of my efforts in the courses I teach are directed towards developing a hands-on laboratory component that is tightly integrated with the lectures. As part of my teaching, I offer alternative methods to facilitate student learning: (1) open office hours, (2) using power-point presentations, (3) conducting examinations uniformly distributed over the semester, (4) conducting regular quizzes and homework, (5) maintaining a course home page, (6) maintaining a class mailing list, (7) assigning students to write a term paper and to do a term-project, and, (8) in-class problem solving. Before testing the students, I expose them to concepts three times: once in the lecture via examples, a second time via homework assignments and a third time via a laboratory or programming project.

I have successfully used this paradigm in both graduate and undergraduate courses. All the courses I have developed are an integral part of the computer engineering curriculum and have served the need of a large diversity of students. In multiple years, I received Honors Day recognition as an inspirational faculty at the UNT. I have also received UNT Provost's Thank a Teacher recognition for multiple years. I received the University of South Florida Provost's certificate of recognition for outstanding performance as a graduate teaching assistant for two consecutive years, 2002 and 2003. I have advised dozens of graduate students on their Ph.D. dissertations and M.S. theses. I advised the first Ph.D. dissertation and the first 3 M.S. theses in VLSI at UNT. I have also been a research mentor for dozens of undergraduate and Texas Academy of Mathematics and Science (TAMS) students. My Amazon best-seller book titled "Nanoelectronic Mixed-Signal System Design", published by McGraw-Hill in 2015, is a textbook for senior undergraduate to graduate students. My students regularly receive outstanding student awards at UNT. In addition, it is a pleasure to note that at 2014 UNT Honors day, 3 of my students were selected as outstanding students for each of the CSE doctoral, computer engineering Masters, and computer engineering Bachelors categories, respectively. My course enrollment is always very strong. My teaching evaluation is always excellent. A detailed list of courses that I have taught is given in the following Table, which also includes a few courses that I have assisted in delivering.

Semester	Course No.	Course Title	Size	Course Level	Institute
Spring 2018	CSCE 6731	Advanced Topics in VLSI Systems	08	Graduate	UNT
	CSCE 5740	Topics in Modern Electronic System Design	15	Graduate	
Fall 2017	CSCE 5730	Digital CMOS VLSI Design	15	Graduate	UNT
Spring 2017	CSCE 6731	Advanced Topics in VLSI Systems	07	Graduate	UNT
	CSCE 5730	Digital CMOS VLSI Design	30	Graduate	
	CSCE 4730	VLSI Design	05	Undergraduate	
Spring 2016	CSCE 5730	Digital CMOS VLSI Design	35	Graduate	UNT
	CSCE 4730	VLSI Design	05	Undergraduate	
Fall 2015	CSCE 6731	Advanced Topics in VLSI Systems	15	Graduate	UNT
	CSCE 5730	Digital CMOS VLSI Design	25	Graduate	
	CSCE 4730	VLSI Design	05	Undergraduate	
Spring 2015	CSCE 5730	Digital CMOS VLSI Design	35	Graduate	UNT

Semester	Course No.	Course Title	Size	Course Level	Institute
Fall 2014	CSCE 6731	Advanced Topics in VLSI Systems	12	Graduate	UNT
	CSCE 5730	Digital CMOS VLSI Design	38	Graduate	
	CSCE 4730	VLSI Design	03	Undergraduate	
Spring 2014	CSCE 5730	Digital CMOS VLSI Design	15	Graduate	UNT
	CSCE 4730	VLSI Design	15	Undergraduate	
Fall 2013	CSCE 6933	Advanced Topics in VLSI Systems	12	Graduate	UNT
	CSCE 5730	Digital CMOS VLSI Design	15	Graduate	
	CSCE 4730	VLSI Design	15	Undergraduate	
Spring 2013	CSCE 5730	Digital CMOS VLSI Design	15	Graduate	UNT
	CSCE 4730	VLSI Design	15	Undergraduate	
Fall 2012	CSCE 6933	Advanced Topics in VLSI Systems	15	Graduate	UNT
	CSCE 5933	Topics in VLSI Systems	15	Graduate	
	CSCE 5730	Digital CMOS VLSI Design	15	Graduate	
	CSCE 4730	VLSI Design	15	Undergraduate	
Spring 2012	CSCE 5730	Digital CMOS VLSI Design	15	Graduate	UNT
	CSCE 4730	VLSI Design	15	Undergraduate	
Fall 2011	CSCE 6933	Advanced Topics in VLSI Systems	15	Graduate	UNT
	CSCE 5730	Digital CMOS VLSI Design	20	Graduate	
	CSCE 4730	VLSI Design	10	Undergraduate	
Spring 2011	CSCE 5730	Digital CMOS VLSI Design	15	Graduate	UNT
	CSCE 4730	VLSI Design	15	Undergraduate	
Fall 2010	CSCE 6730	Advanced VLSI Systems	15	Graduate	UNT
	CSCE 5730	Digital CMOS VLSI Design	15	Graduate	
	CSCE 4730	VLSI Design	15	Undergraduate	
Spring 2010	CSCE 5730	Digital CMOS VLSI Design	15	Graduate	UNT
	CSCE 4730	VLSI Design	15	Undergraduate	
Fall 2009	CSCE 6730	Advanced VLSI Systems	15	Graduate	UNT
	CSCE 5730	Digital CMOS VLSI Design	15	Graduate	
	CSCE 4730	VLSI Design	15	Undergraduate	
Spring 2009	CSCE 5730	Digital CMOS VLSI Design	15	Graduate	UNT
	CSCE 4730	VLSI Design	15	Undergraduate	
	CSCE 2610	Computer Organization	15	Undergraduate	
Fall 2008	CSCE 5730	Digital CMOS VLSI Design	15	Graduate	UNT
	EENG 4710	VLSI Design	15	Undergraduate	
Spring 2008	CSCE 5730	Digital CMOS VLSI Design	15	Graduate	UNT
	CSCE 4730	VLSI Design	15	Undergraduate	
	CSCE 2610	Computer Organization	15	Undergraduate	
Fall 2007	CSCE 5730	Digital CMOS VLSI Design	15	Graduate	UNT
	CSCE 4730	VLSI Design	15	Undergraduate	
	EENG 4710	VLSI Design	15	Undergraduate	
Spring 2007	CSCE 5730	Digital CMOS VLSI Design	30	Graduate	UNT
	CSCE 5610	Computer System Architecture	15	Graduate	
	CSCE 4610	Computer Architecture	15	Undergraduate	
Fall 2006	CSCE 6651	Advanced VLSI Systems	30	Graduate	UNT
	CSCE 5730	Digital CMOS VLSI Design	15	Undergraduate	

Semester	Course No.	Course Title	Size	Course Level	Institute
	CSCE 4730	VLSI Design	15	Undergraduate	
	EENG 4710	VLSI Design	15	Undergraduate	
Spring 2006	CSCE 5730	Digital CMOS VLSI Design	30	Graduate	UNT
Fall 2005	CSCE 6651	Advanced VLSI Systems	30	Graduate	UNT
Spring 2005	CSCI 5330	Digital CMOS VLSI Design	30	Graduate	UNT
Fall 2004	CSCI 5330	Digital System Design with VHDL	15	Graduate	UNT
	CSCI 4330	Digital System Design with VHDL	15	Undergraduate	
Fall 2003	CDA 4203	Computer System Design	45	Undergraduate	USF
Summer 2003	COT 4400	Analysis of Algorithms	30	Undergraduate	USF
Spring 2003	COT 4400	Analysis of Algorithms	30	Undergraduate	USF
Fall 2002	COT 4400	Analysis of Algorithms	45	Undergraduate	USF
Summer 2002	COT 4400	Analysis of Algorithms	35	Undergraduate	USF
Spring 2002	CIS 4930	FPGA Design	30	Undergraduate	USF
(TA)	CDA 4205	Computer Architecture	50	Undergraduate	
Fall 2001	CDA 4205	Computer Architecture	50	Undergraduate	USF
Summer 2001	COT 4400	Analysis of Algorithms	45	Undergraduate	USF
Spring 2001 (TA)	CEN 4020	Software Engineering	45	Undergraduate	USF
Fall 2000	CDA 4205	Computer Architecture	50	Undergraduate	USF
Summer 2000	EEL 4851	Data Structures	45	Undergraduate	USF
(TA)	CIS 4930	Application Development	30	Undergraduate	
Spring 2000	CEN 4020	Software Engineering	45	Undergraduate	USF
(TA)	COT 4400	Analysis of Algorithms	45	Undergraduate	
Spring 1996	NA	Power System Design	35	Undergraduate	OUAT
	NA	Electrical Engineering Laboratory	35	Undergraduate	
Fall 1995	NA	Utilization of Electrical Energy	35	Undergraduate	OUAT
	NA	Power System Operation and Control	35	Undergraduate	