Variability-Aware Optimization of Nano-CMOS Active Pixel Sensors using Design and Analysis of Monte-Carlo Experiments

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Summary and Conclusions

- A novel design flow for mismatch and process variation aware optimization of nanoscale CMOS Active Pixel Sensor (APS) arrays is proposed. For case study, 32 nm 8 × 8 APS array is considered.
- The baseline APS array is subjected to 5% "intra-pixel" mismatch and 10% "inter-pixel" process variation and the effect on power and output voltage swing has been observed.
- The basekine array is optimized using a design and analysis of Monte Carlo experiments based optimization. We achieve 21% reduction in power (including leakage).
- In the future, we plan to investigate variability-aware design of APS for post-nano-CMOS, such as high-κ/metal gate, Carbon Nanotube, and Dual-Gate FETs.

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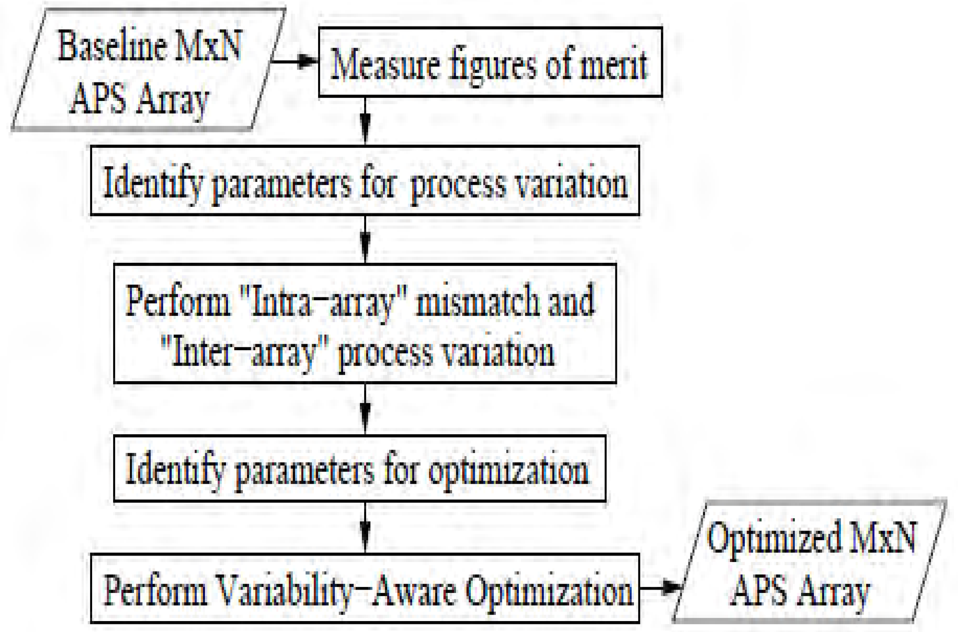
Abstract

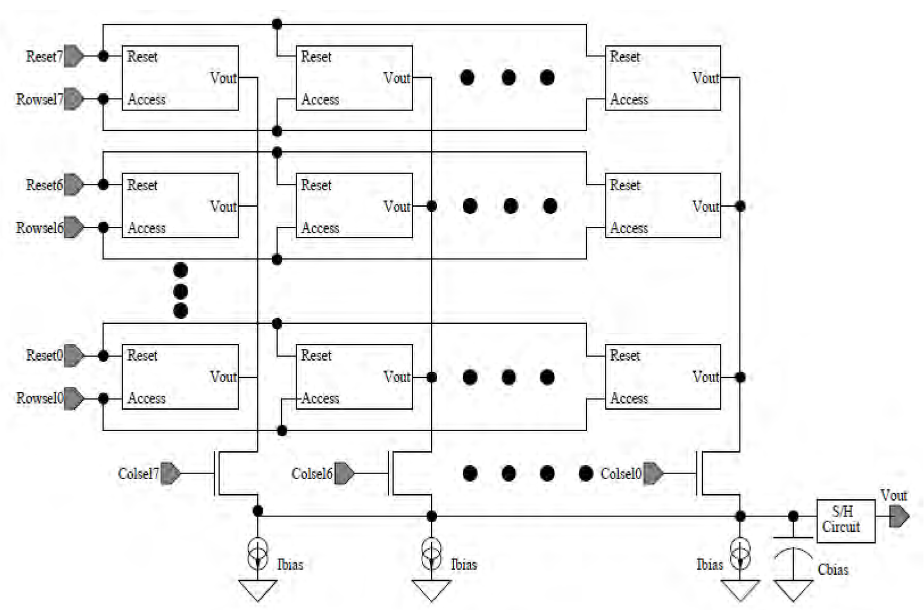
• *A novel design flow for mismatch and process variation aware optimization of nanoscale CMOS Active Pixel Sensor (APS) arrays is proposed. For case study, 32nm 8×8 APS array is considered.*
• *The baseline APS array is subjected to 5% "intra-pixel" mismatch and 10% "inter-pixel" process variation and the effect on power and output voltage swing has been observed.*
• *The basekine array is optimized using a design and analysis of Monte Carlo experiments based optimization.*
• *We achieve 21% reduction in power (including leakage). To the best of our knowledge, this is the first ever nano-CMOS implementation of an APS array optimized to be mismatch and process variation tolerant.*

Proposed Design Flow

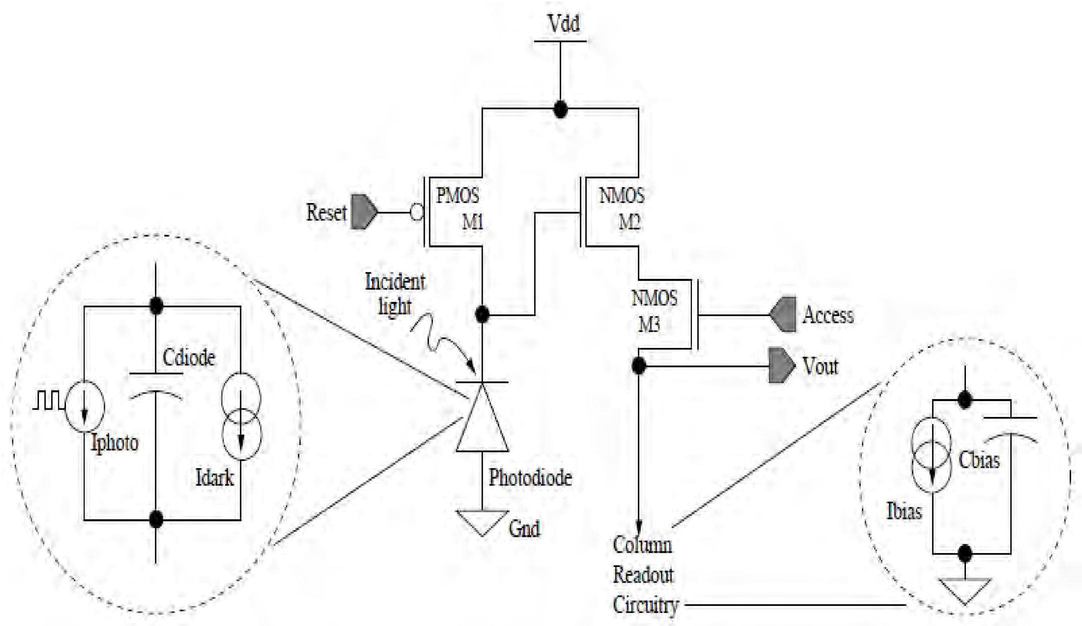


• Input to the design flow is a baseline array.
• The baseline array is simulated for the nominal values of the target figures of merit: power (P_{APS}) and voltage swing (V_{swing}).
• The array is then subjected to simultaneous intra-array mismatch and inter-array process variation.
• Once the process variation results are recorded, the design flow proceeds to the optimization.
• The end product is an $M \times N$ APS array optimized for nanoscale process variations.

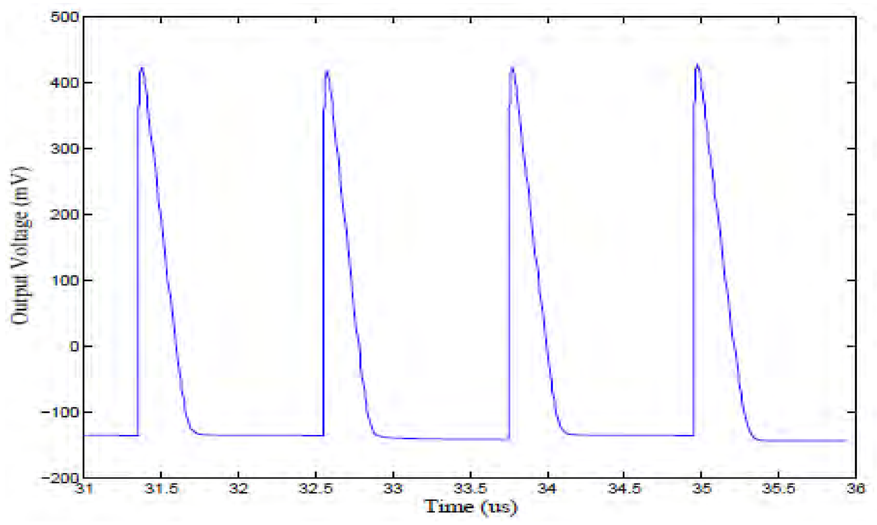
32nm Active Pixel Sensor



• Active-pixel sensor (APS) is an image sensor consisting of an integrated circuit containing an array of pixel sensors.



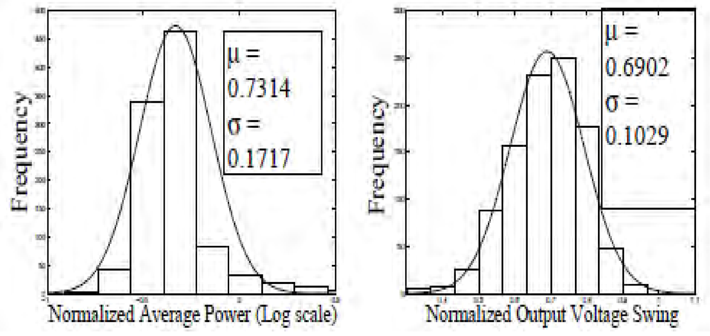
• Each pixel contains a photodetector and an active amplifier. The three transistors of the circuit: (i) M1: reset transistor, (ii) M2: source follower transistor, and (iii) M3: access transistor.
• Transistor sizes are chosen carefully for enough current, source follower gain, and isolation of source follower output from the pixel output.



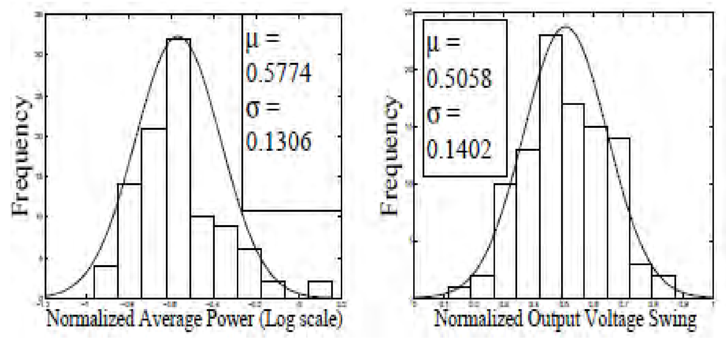
• Functional simulation of 8x8 APS Array.

Process Variation

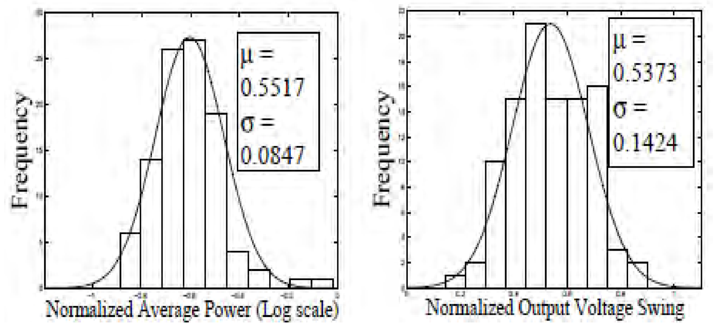
• Array subjected to Monte Carlo simulations.
• The process parameters identified are: (i) supply voltage V_{dd}, (ii) NMOS threshold voltage V_{Tnmos}, (iii) PMOS threshold voltage VT_{pmos}, (iv) Gate-oxide thickness T_{ox} .
•Parameters for optimization are: V_{dd}, T_{ox}.
• Mean (μ) and Standard deviation (σ) of P_{APS} and V_{swing} are recorded.



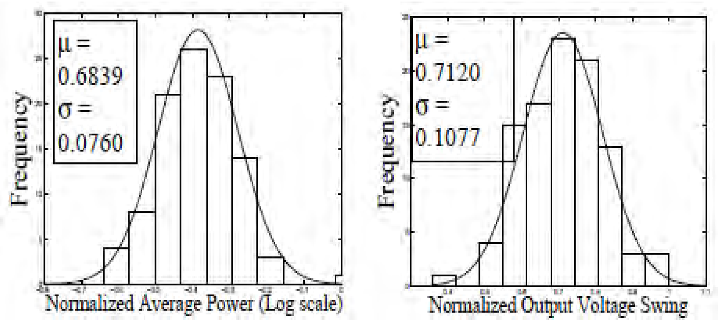
• Distribution of P_{APS} and V_{swing} for V_{dd-H} and T_{ox-L} (baseline case.)



• Distribution of P_{APS} and V_{swing} for V_{dd-L} and T_{ox-L}.



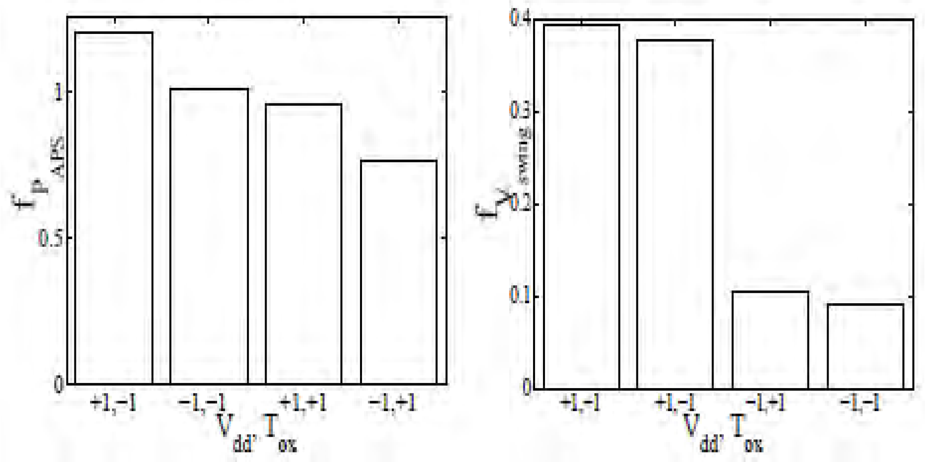
• Distribution of P_{APS} and V_{swing} for V_{dd-L} and T_{ox-H}.



• Distribution of P_{APS} and V_{swing} for V_{dd-H} and T_{ox-H}.

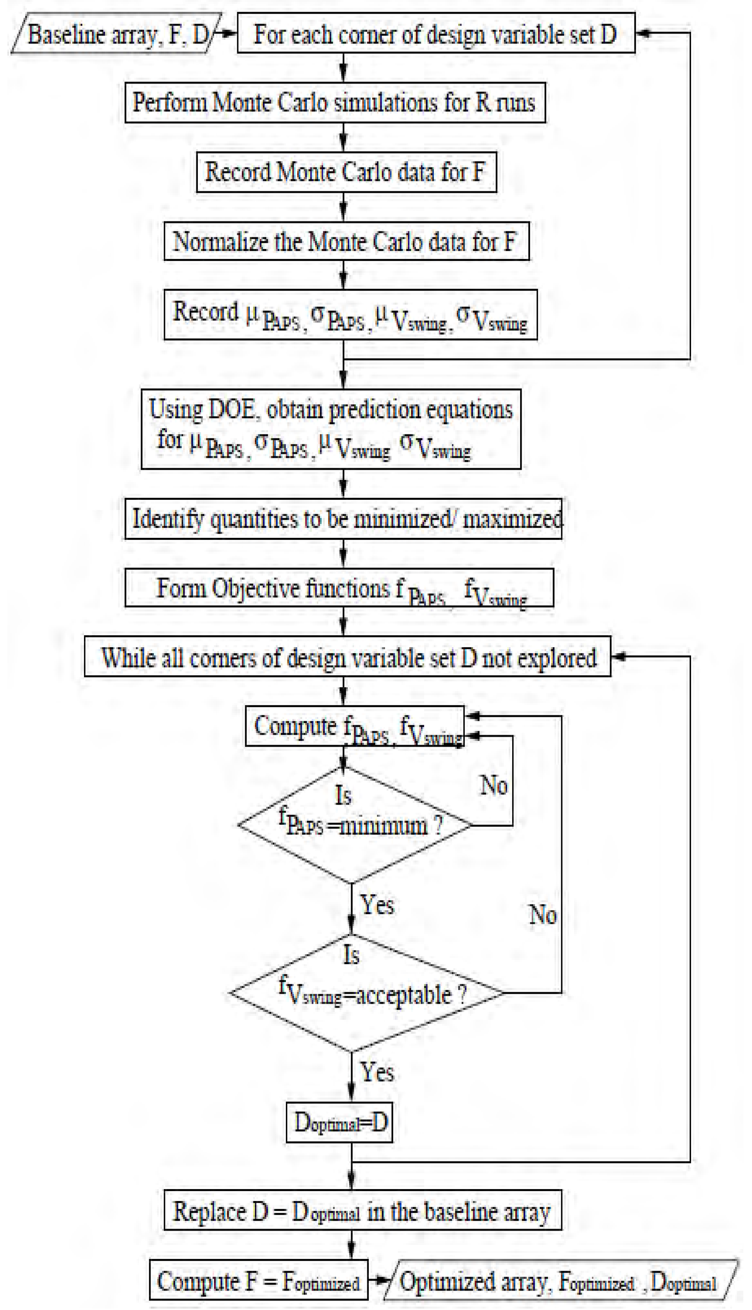
V_{dd} (V)	T_{ox} (nm)	μP_{APS} (μW)	σP_{APS} (μW)	μV_{swing} (mV)	σV_{swing} (mV)
V_{dd-L}	T_{ox-L}	0.5774	0.1306	0.5058	0.1402
V_{dd-L}	T_{ox-H}	0.5517	0.0847	0.5373	0.1424
V_{dd-H}	T_{ox-L}	0.7314	0.1717	0.6902	0.1029
V_{dd-H}	T_{ox-H}	0.6839	0.0760	0.7120	0.1077

• Monte Carlo simulation results



• Pareto Plot for f_{PAPS} and f_{Vswing}.

Proposed Optimization



• Using Design of Experiments, we obtain:

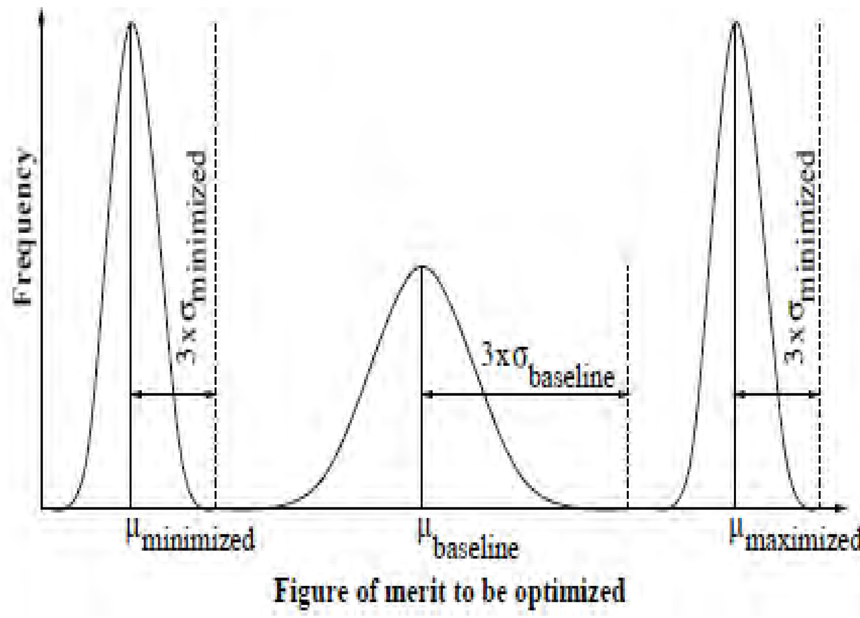
$\mu_{PAPS} = 0.6361 + 0.0716 \times Vdd - 0.0183 \times Tox$..(1)
$\sigma_{PAPS} = 0.1157 + 0.0081 \times Vdd - 0.0354 \times Tox$..(2)
$\mu_{Vswing} = 0.6113 + 0.0898 \times Vdd + 0.0133 \times Tox$..(3)
$\sigma_{Vswing} = 0.1233 - 0.0180 \times Vdd + 0.0018 \times Tox$..(4)

• Forming objective functions:

$f_{PAPS} = \mu_{PAPS} + 3 \times \sigma_{PAPS}$,
$= 0.9832 + 0.0959 \times Vdd - 0.1245 \times Tox$..(5)
$f_{Vswing} = \mu_{Vswing} - 3 \times \sigma_{Vswing}$,
$= 0.2414 + 0.1438 \times Vdd + 0.0079 \times Tox$..(6)

Value	P_{APS} (μW)	V_{swing} (mV)
baseline	16.32	428
Optimal	12.91	325

• Baseline and Optimal values of figures of merit.



• Objective of the Variability-Aware Optimization

Conclusion and Future Research

• We pesent a novel design flow and optimization algorithm suitable for variation-tolerant (robust) design of nano-CMOS APS..
• Design and analysis of Monte Carlo experiments on the baseline array has been carried out leading to 21% power reduction at the cost of 24% output voltage swing reduction.
• In the future, we plan to investigate variability-area design of APS for post-nano-CMOS, such as high-/ metal gate, Carbon Nanotube, and Dual-Gate FETs.

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