

Towards Robust Nano-CMOS Sense Amplifier Design: A Dual-Threshold versus Dual-Oxide Perspective

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Overview



- **Motivation**
- **Novel Contributions**
- **Functional Design of Sense Amplifier Circuit**
- **Statistical Analysis of Design**
- **Proposed Design Flow– Dual Threshold Technique vs Dual Oxide Technique**
- **Conclusion & Future Work**

Motivation

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- Impact of Process variations in nanoscale design is increasing
- Issues in Nanoscale circuit design
 - Variability
 - Leakage
 - Power consumption
- Memory systems are important component of Computing
 - Sense amplifiers are vital for DRAMs

Contributions of this Paper

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- Efficient process variation aware design methodology.
- Analysis of effects of device parameters on different sense amplifier FoMs.
- Analysis of effect of process variation on the performance of full latch sense amplifier.
- Exploring dual- V_{th} and dual- T_{ox} for more sense amplifier performance characteristics.

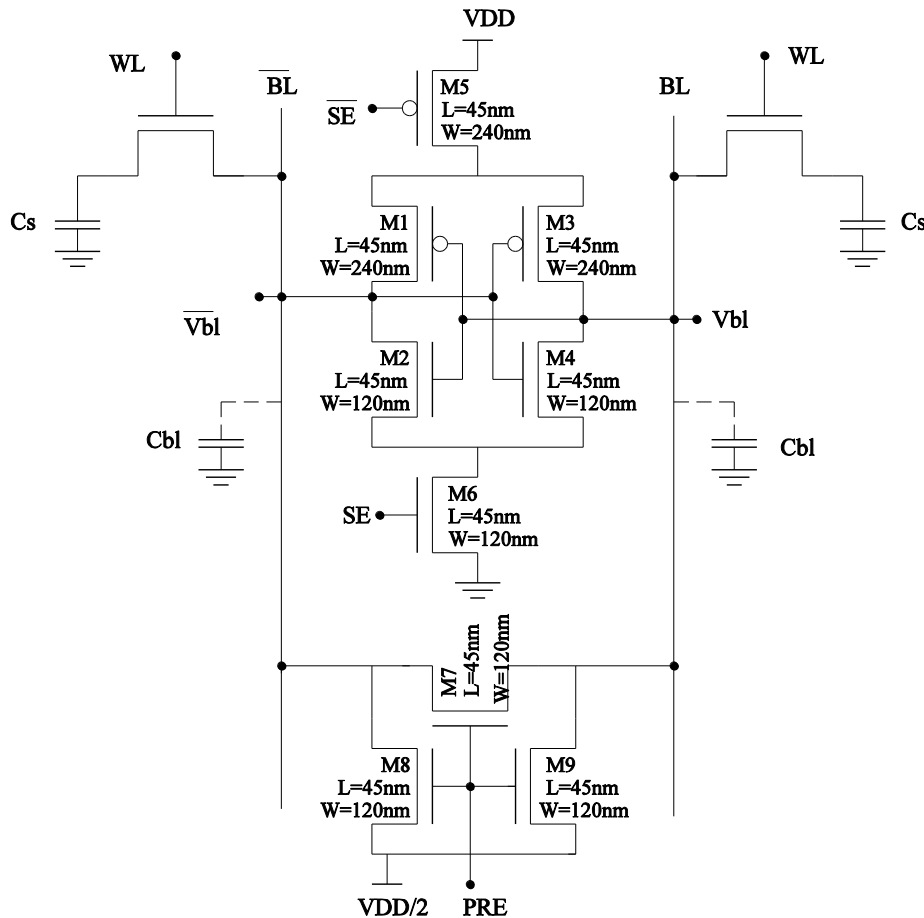
Prior Related Research

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Research	Parameter	Feature	Approach	Result Improvement
Sherwin[2]	V_{DD}	Voltage gain	Physical measurements	-
Chow[2]	C_{BL}	Sense Speed	Spice simulations	Sense speed – 40%
Laurent[8]	C_{BL}, V_{th}, β	Signal Margin	Spice Simulations	-
Choudhary[3]	V_{th}, L, W	Yield	Monte Carlo analysis	Improved Yield
Singh[13]		SE rise time	Spice simulations	Eliminated offset voltage
This paper	Dual- V_{th}, T_{ox}	Process variability	Optimization	Sense delay – 54% Sense margin – 40%

Functional Design of Sense Amplifier

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Equations for Charge Sharing

$$\Delta V = \frac{C_S}{C_S + C_{BL}} \left(V_{CS} - \frac{V_{DD}}{2} \right)$$

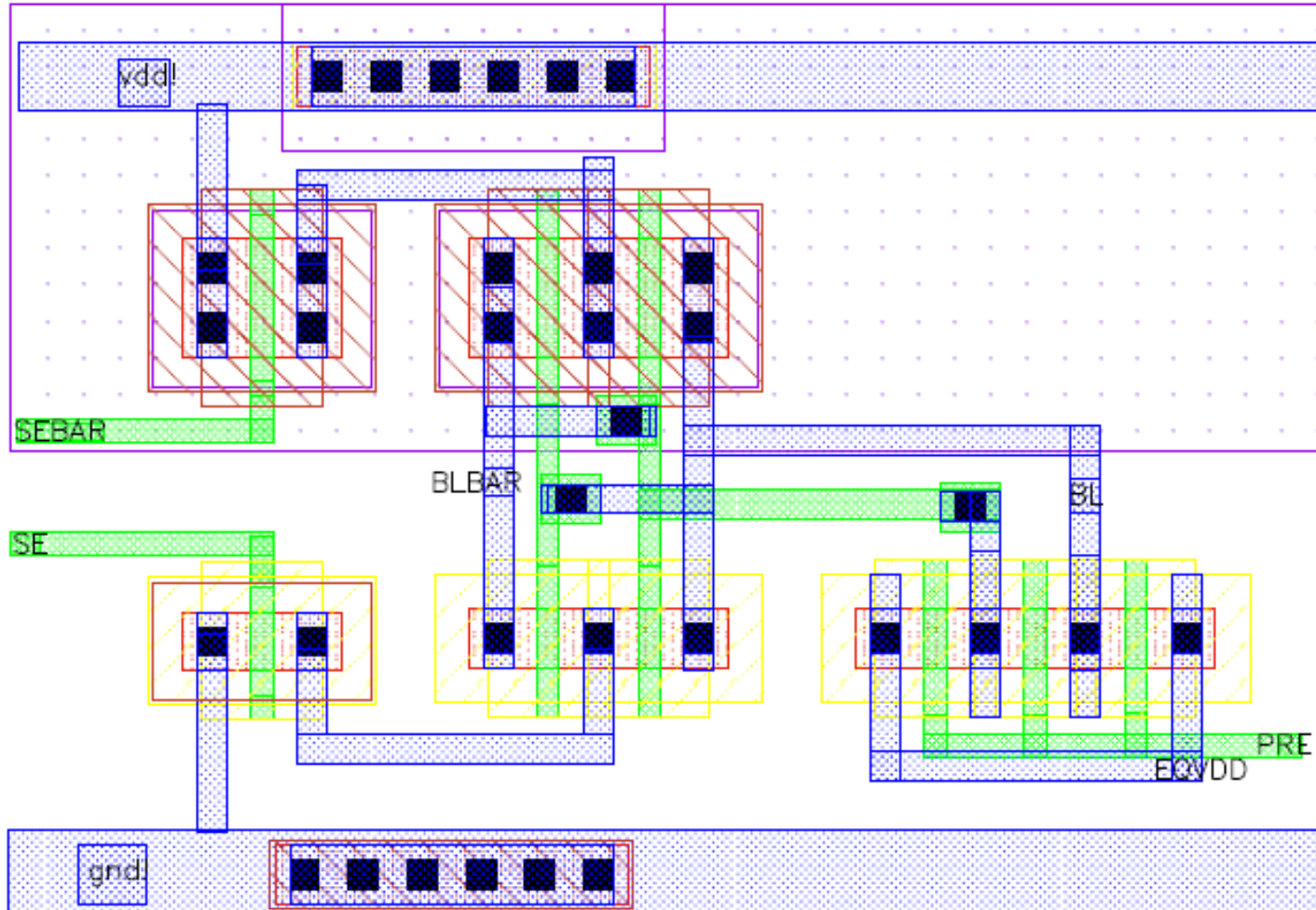
when bit cell value is 1, $V_{CS} = V_{DD} - V_{th}$

$$\Delta V \approx \frac{C_S}{C_{BL}} \left(\frac{V_{DD}}{2} - V_t \right)$$

when bit cell value is 0, $V_{CS} = 0$

$$\Delta V \approx -\frac{C_S}{C_{BL}} \left(\frac{V_{DD}}{2} \right)$$

Physical Layout for 45nm Sense Amplifier



Figures of Merit

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- Precharge and Equalization Time
- Average Power Consumption
- Sense Delay
- Sense Margin

Table for Figures of Merit
Characterization

Circuit	Precharge	Power	Sense Delay	Sense Margin
Schematic	18.024 ns	1.166 μ W	7.46 ns	29.331 mV
Layout	18.20 ns	1.175 μ W	7.45 ns	29.256 mV

Parametric Analysis

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The following parameters analyzed

- Gate Lengths and Widths (L_n , L_p , W_n , W_p)
- Voltage Supply (V_{DD})
- Cell Capacitance (C_S)
- Bitline Capacitance (C_{BL})
- Oxide Thickness (T_{oxn} , T_{oxp})
- Threshold Voltage (V_{thn} , V_{thp})

Parametric Analysis: Results and Comparison

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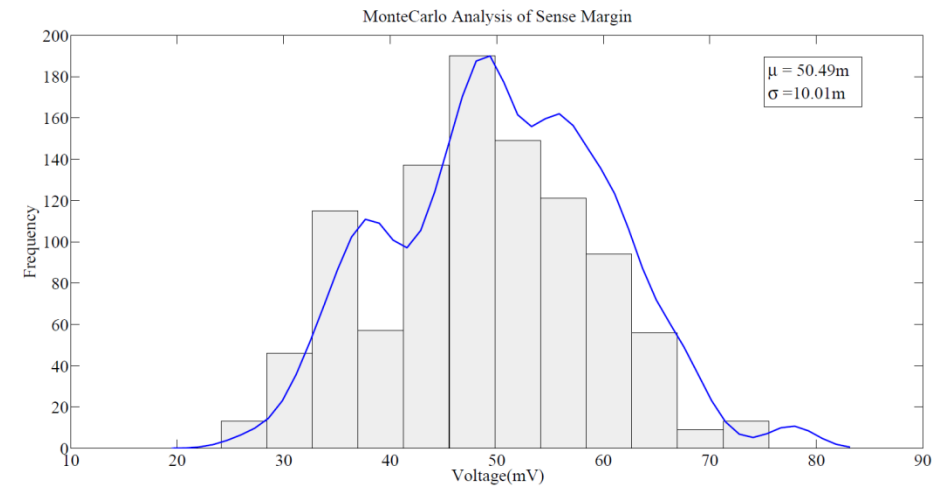
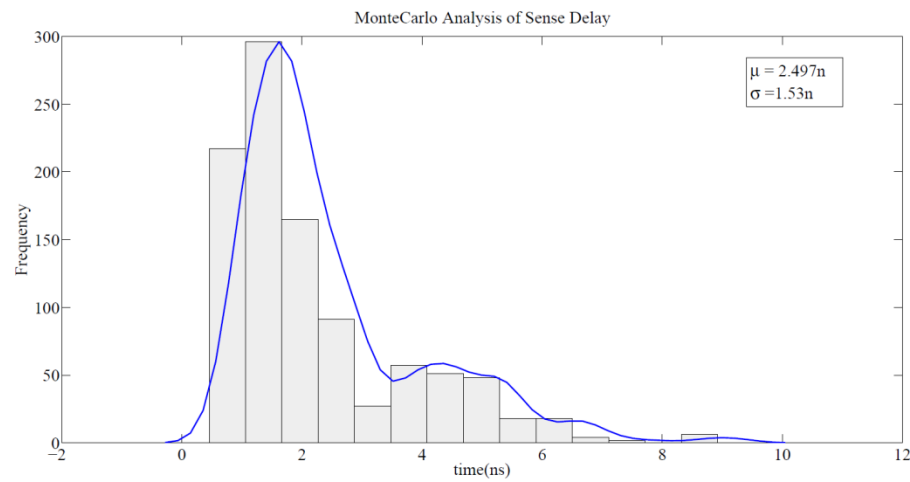
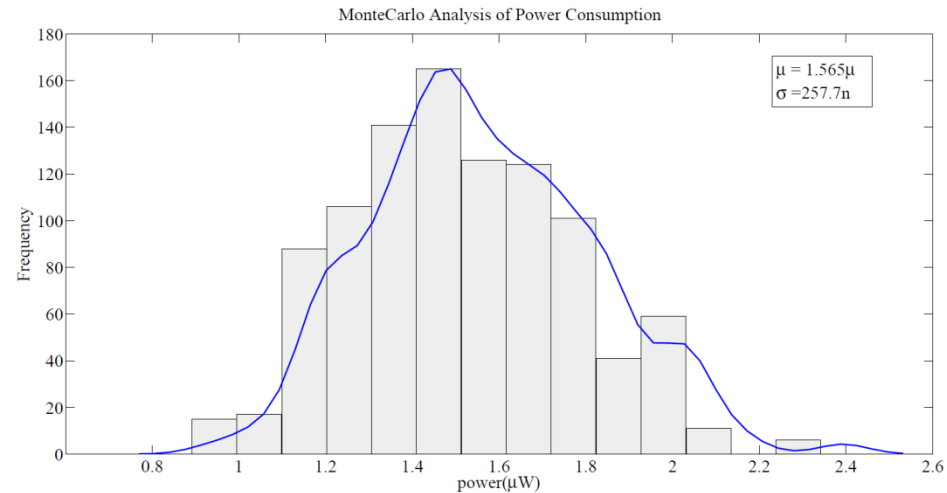
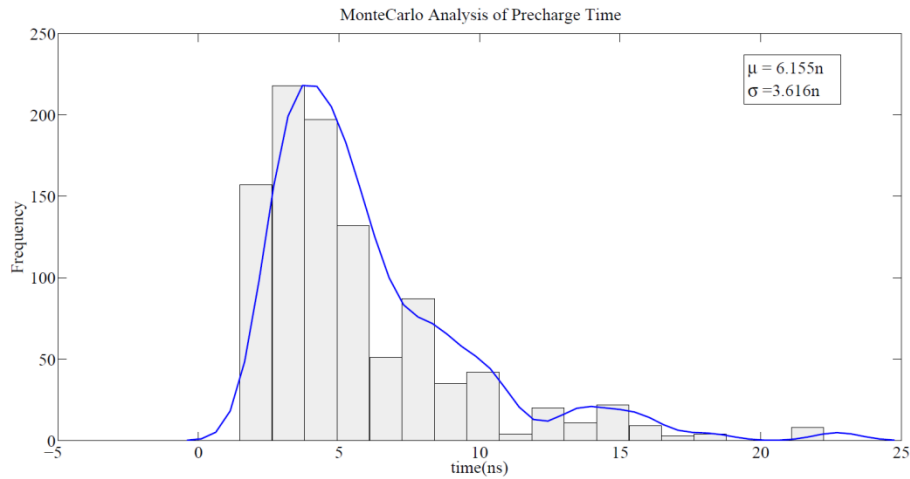
Parameter	Precharge Time	Power Dissipation	Sense Delay	Sense Margin
L_n	decrease	increase	decrease	increase
L_p	increase	decrease	mild increase	mild decrease
W_n	decrease	increase	decrease	decrease
W_p	increase	increase	mild decrease	mild decrease
V_{DD}	decrease	increase	decrease	increase
C_S	increase	increase	increase	increase
C_{BL}	increase	increase	mild increase	mild decrease
V_{thn}	decrease	decrease	decrease	increase
V_{thp}	decrease	decrease	mild increase	mild increase
t_{oxn}	decrease	increase	decrease	increase
t_{oxp}	decrease	decrease	mild decrease	mild increase

Probability Density Function of Different FoMs of the Sense Amplifier

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Parameters	Precharge PDF		Power PDF		Sense Delay PDF		Sense Margin PDF	
	μ (ns)	σ (ps)	μ (μ W)	σ (nW)	μ (ns)	σ (ps)	μ (mV)	σ (mV)
L_n	5.474	4.22	94.93	3.13	770.10	80.85	7.89	907.49
L_p	5.546	674.26	1.54	44.33	2.165	272.9	49.4	2.06
W_n	5.398	664.4	1.53	44.04	2.118	255.6	49.51	1.97
W_p	5.546	671.63	1.54	44.26	2.166	274.03	49.39	2.06
V_{DD}	6.308	3256.8	1.55	215.8	2.58	1534.3	49.49	8.64
C_S	5.546	671.65	1.54	44.91	2.171	294.2	49.38	2.66
C_{BL}	5.55	725.64	1.54	89.5	2.167	275.1	49.44	2.88
V_{thn}	5.557	775.5	1.54	47.6	2.172	306.8	49.4	2.27
V_{thp}	5.545	671.7	1.55	45.77	2.166	274	49.39	2.07
t_{oxn}	5.566	741.25	1.54	45.57	2.173	293.4	49.39	2.34
t_{oxp}	5.546	671.64	1.54	43.6	2.166	274	49.39	2.06

Probability Density Function of FoMs



Proposed Design Flow:

Algorithm 1 Design Flow for the Optimal Sense Amplifier Design.

- 1: Perform the baseline sense amplifier circuit design.
 - 2: Simulate baseline sense amplifier for functional verification.
 - 3: Characterize the sense amplifier for the target figures of merit.
 - 4: Perform the physical design of the sense amplifier.
 - 5: Perform DRC and LVS of the physical design.
 - 6: Perform RLCK extraction to obtain parasitic-aware netlist.
 - 7: Parameterize parasitic-aware netlist of the sense amplifier.
 - 8: Perform parametric analysis to identify impact on FoMs.
 - 9: Perform statistical yield analysis for process variation effects.
 - 10: Select the device parameters for optimization.
 - 11: Perform sense amplifier optimization using Algorithm 2.
 - 12: Obtain the optimal physical design of the sense amplifier.
 - 13: Characterize the optimal design of the sense amplifier.
 - 14: Perform quality analysis of the optimization.
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Dual V_{th} , T_{ox} , Technology

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- A Monte Carlo analysis of the effects of process variation of design parameters on FoMs
 - Parameters were varied at +/- 5% of selected values from parametric analysis
- A Monte Carlo analysis of the FoMs reaction to variation of individual parameters
- Transistors are assigned different threshold voltages for optimizing design
 - $V_{th,high} = 0.40V$ $T_{ox,high} = 1.7nm$
 - $V_{th,low} = 0.22V$ $T_{ox,low} = 3.0nm$
- FoM's are analyzed with different threshold voltages

Heuristic Optimization Algorithm: Dual V_{th} , T_{ox}

Algorithm 2 Heuristic for Sense Amplifier Circuit Optimization.

- 1: Start with a parameterized parasitic netlist of sense amplifier.
 - 2: Assign all the transistors to nominal V_{th} (or t_{ox}).
 - 3: Number each of the transistors in the netlist from 1 to N.
 - 4: **for** {Each of the transistors $i = 1$ to N} **do**
 - 5: Analyze the impact of each transistor on a specific figure of merit (e.g. precharge time) of the sense amplifier circuit.
 - 6: Rank the transistors according to their contribution to a figure of merit.
 - 7: Mark the significant transistors from ranks (e.g. top 30%).
 - 8: **end for**
 - 9: Start with the highest ranked transistor as $i = 0$.
 - 10: **while** {Design constraint of sense amplifier is met and transistor M_i is a significant transistor that contributes to the FoM} **do**
 - 11: Increase threshold voltage (or thickness oxide) of M_i .
 - 12: Move to the next ranked transistor.
 - 13: **end while**
 - 14: **return** { V_{th} (or t_{ox}) assignment of each transistor M_i .}
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Characterization of Optimized Design

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- The FoM's are improved on the final design

Circuit	Precharge Time	Power Dissipation	Sense Delay	Sense Margin
Schematic	18.024 ns	1.166 μ W	7.460 ns	29.331 mV
Layout	18.20 ns	1.175 μ W	7.45 ns	29.256 mV
Dual- V_{th}	6.61 ns	0.941 μ W	3.476 ns	40.851 mV
Dual- T_{ox}	6.596 ns	0.895 μ W	3.464 ns	40.77 mV

Conclusions

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- The effects of process variation were analyzed through parametric and Monte Carlo analysis
- A method of producing more tolerant and optimal designs was presented.
- FoM's were improved
 - Precharge by 63.3% using dual- V_{th} techniques
 - Precharge by 63.4% using dual- V_{th} techniques
- Methodology will be extended to different sense amplifier topologies

Thank you...

you can find copy of presentation at:

<http://www.cse.unt.edu/~smohanty/>

Questions?

