Comparative Analysis of Double Gate FinFET Configurations for Analog Circuit Design

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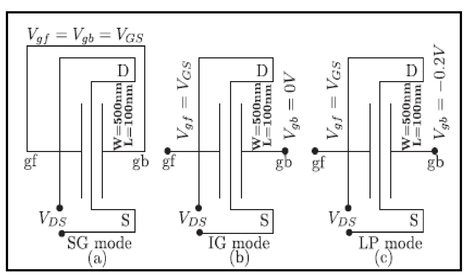
Abstract

• *The double gate (DG) FinFET gives rise to a rich design space using various configurations of the gates.*
• *We compare the DG FinFET parameters including transconductance (gm), output resistance (r0), open-circuit gain (gm × r0), transition frequency (fT) including the most important issue, "nanoscale variability" which are important for analog design.*
• *These configurations for a fully depleted SOI DG FinFET are analyzed: shorted-gate, independent-gate, and low-power, for both strong inversion and subthreshold operations.*
•*Using the results obtained, we present guidelines for DG FinFET based analog design.*

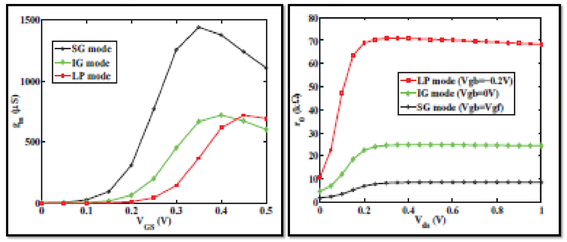
Introduction

Three configurations are identified: shorted-gate (SG) mode, low-power (LP) mode and independent gate (IG) mode.
In the SG mode, the front and back gates are tied together.
In the IG mode, the top part of the gate is etched out for two independent gates and back gate is grounded.
The LP-mode applies a reverse bias voltage to the back-gate.
The question is how good is each of the DG FinFET configurations for analog designs.

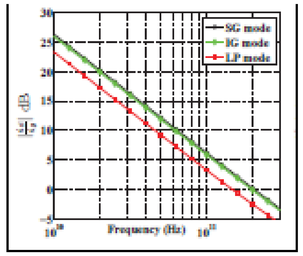


DG FinFET Parameters

Strong Inversion Region:



Configuration	g_m	r_0	$g_m \times r_0$
SG mode	1.4391 mS	8.49 kΩ	12.22
IG mode	666.07 μS	24.83 kΩ	16.54
LP mode	366.5 μS	70.88 kΩ	25.98

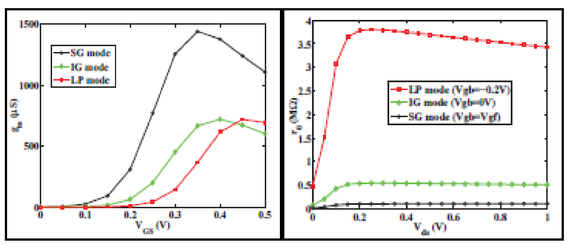


Configuration	f_T
SG mode	208.1 GHz
IG mode	200.6 GHz
LP mode	149.9 GHz

$$g_m \propto \sqrt{I_D}, r_0 \propto \frac{1}{I_D}, (g_m \times r_0) \propto \frac{1}{\sqrt{I_D}},$$

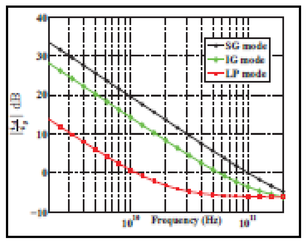
$$f_T = \frac{g_m}{2 \times \pi \times C_{gs}}$$

Subthreshold Region:



Configuration	g_m			r_0			f_T		
	μ	σ	$c_0=\frac{\sigma}{\mu}\%$	μ	σ	$c_0=\frac{\sigma}{\mu}\%$	μ	σ	$c_0=\frac{\sigma}{\mu}\%$
SG mode	1.436 mS	18.71 μS	1.30	8.51 kΩ	177.79Ω	2.08	207.23 GHz	11.06 GHz	5.33
IG mode	666.66 μS	21.14 μS	3.17	24.91 kΩ	1.17kΩ	4.69	198.46 GHz	7.58 GHz	3.82
LP mode	371.96 μS	53.24 μS	14.31	72.08 kΩ	13.54kΩ	18.78	148.68 GHz	5.03 GHz	3.38

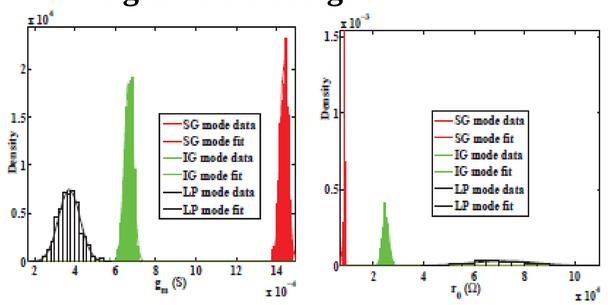
Configuration	g_m	r_0	$g_m \times r_0$
SG mode	309 μS	101.66 kΩ	31.41
IG mode	63.9 μS	538.78 kΩ	34.43
LP mode	12.4 μS	3.7466 MΩ	46.45

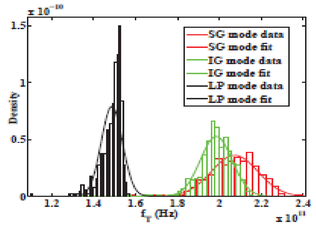


Configuration	f_T
SG mode	100.78 GHz
IG mode	57.65 GHz
LP mode	11.34 GHz

Process Variation Analysis

Strong Inversion Region:

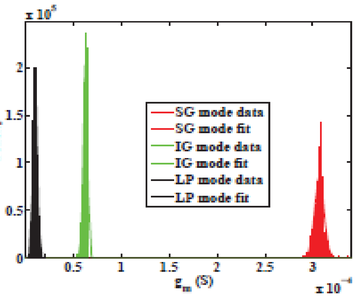


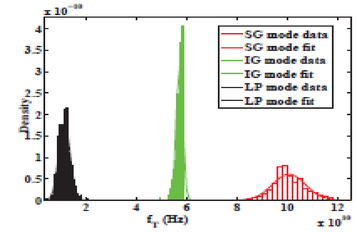


Back-gate Effect:

$$\frac{\partial V_{Thn}}{\partial V_{gb}} = -\left(\frac{\varepsilon_{Si} \times T_{ox}}{\varepsilon_{Si} \times T_{ox} + \varepsilon_{ox} \times T_{Si}}\right),$$

Subthreshold Region:





Configuration	g_m			r_0			f_T		
	μ	σ	$c_0=\frac{\sigma}{\mu}\%$	μ	σ	$c_0=\frac{\sigma}{\mu}\%$	μ	σ	$c_0=\frac{\sigma}{\mu}\%$
SG mode	306.65μS	4.72μS	1.53	105.68 kΩ	1.99 kΩ	1.88	100.68 GHz	6.53 GHz	6.49
IG mode	62.91μS	1.91μS	3.04	541.07 kΩ	11.64 kΩ	2.15	57.21 GHz	1.22 GHz	2.13
LP mode	11.52μS	2.06μS	17.88	3.79 MΩ	736.47 kΩ	19.43	11.51 GHz	2.16 GHz	18.77

$$\Delta V_{Thn} = \left(\frac{\varepsilon_{Si} \times T_{ox}}{\varepsilon_{Si} \times T_{ox} + \varepsilon_{ox} \times T_{Si}}\right) \times \Delta V_{fb},$$

Design Guidelines

Region	Gain	Speed	Variability	Configuration
Subthreshold	High	Low	High	LP
Subthreshold	Medium	Medium	Medium	IG
Subthreshold	Low	High	Low	SG
Strong inversion	High	Low	High	LP
Strong inversion	Medium	Medium	Medium	IG
Strong inversion	Low	High	Low	SG