

# iVAMS: A Paradigm Shift System Simulation Framework for the IoT Era

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04/19/2016

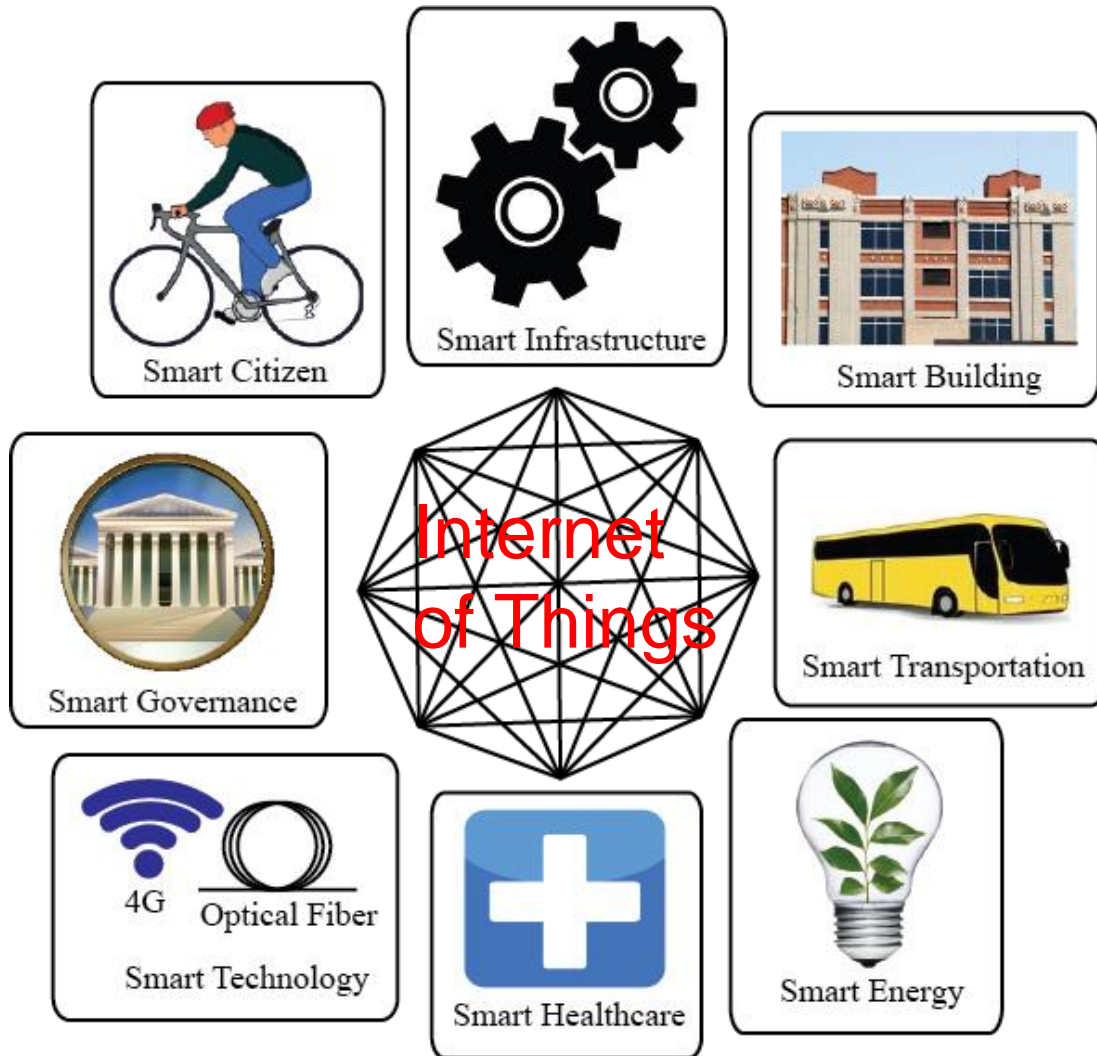


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# Smart Cities

70% of the world population will live in urban areas by 2050.

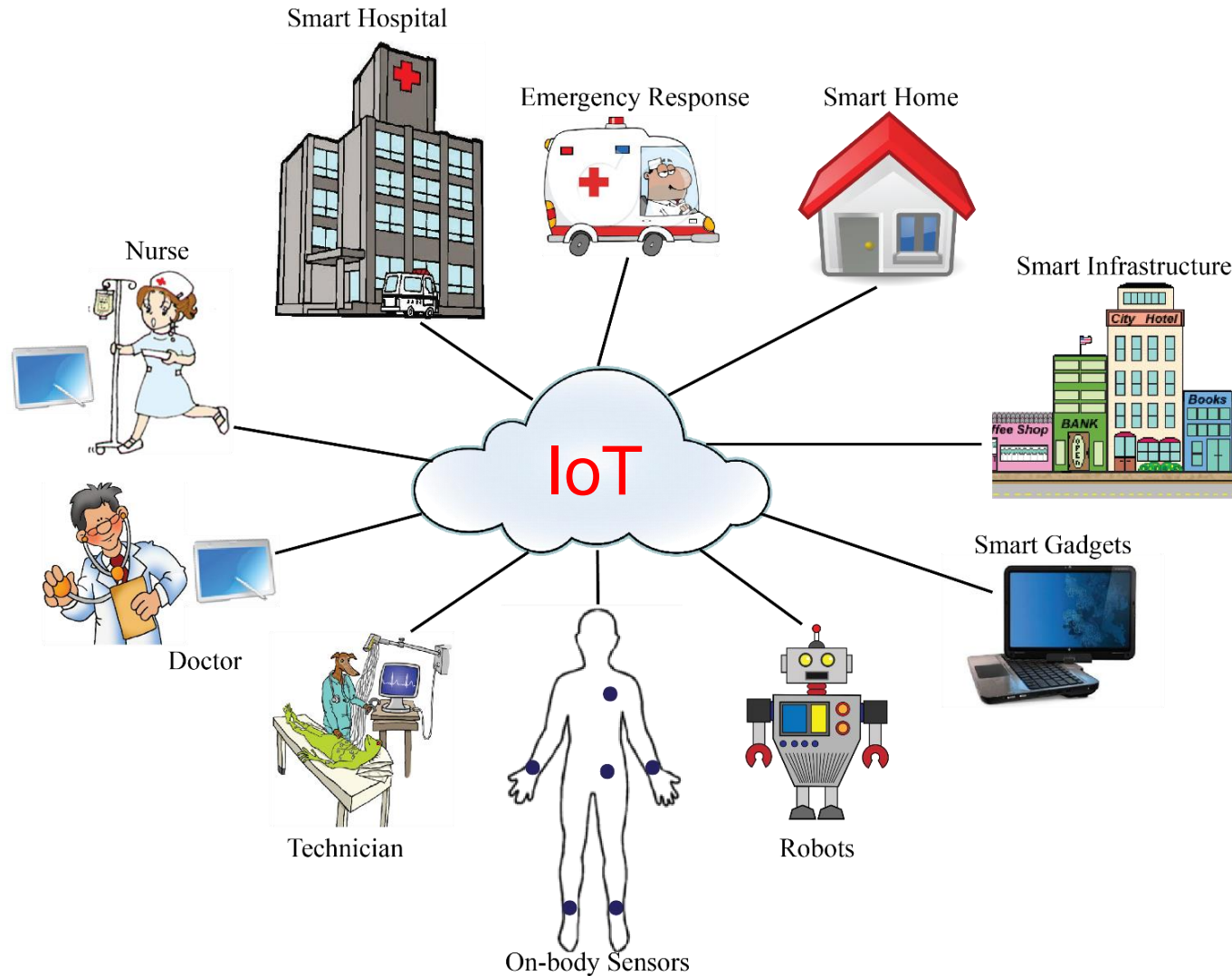
Smart Cities  
← Cities  
+ ICT  
+ Smart  
Components



Refer: <http://smartcities.ieee.org>

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# Smart Health Care

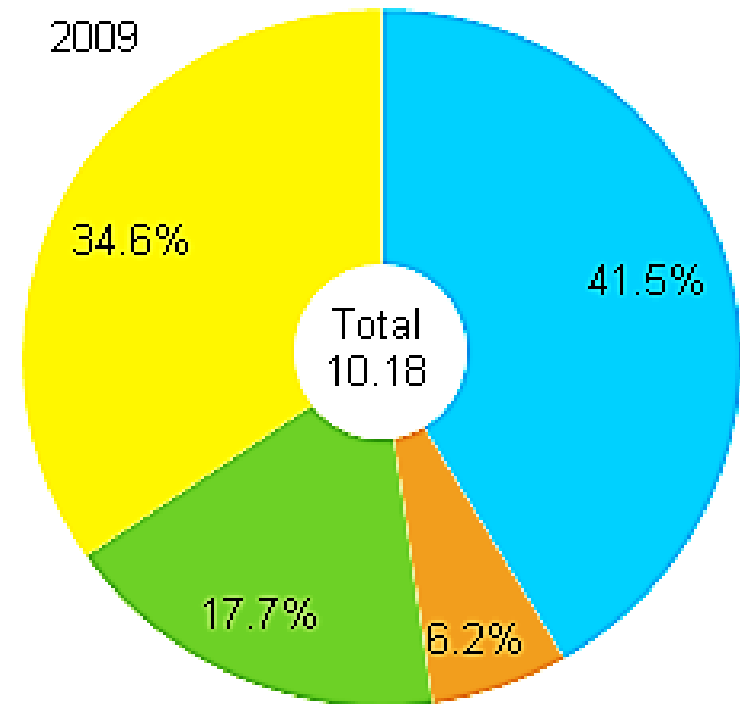
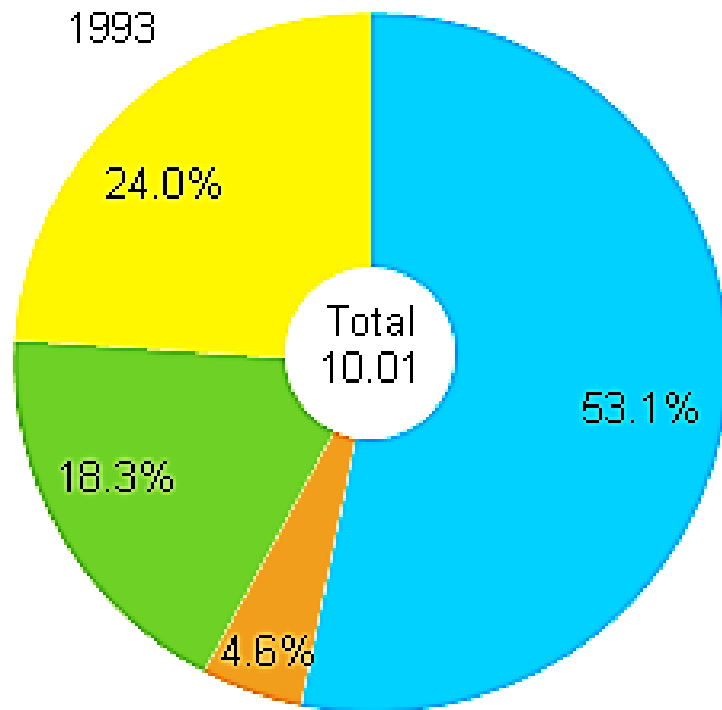


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# Consumer Electronics Demand More and More Energy

Energy consumption in homes by end uses  
quadrillion Btu and percent



■ space heating ■ air conditioning ■ water heating ■ appliances, electronics, and lighting

Quadrillion BTU (or quad): 1 quad =  $10^{15}$  BTU = 1.055 Exa Joule (EJ).

Source: U.S. Energy Information Administration.

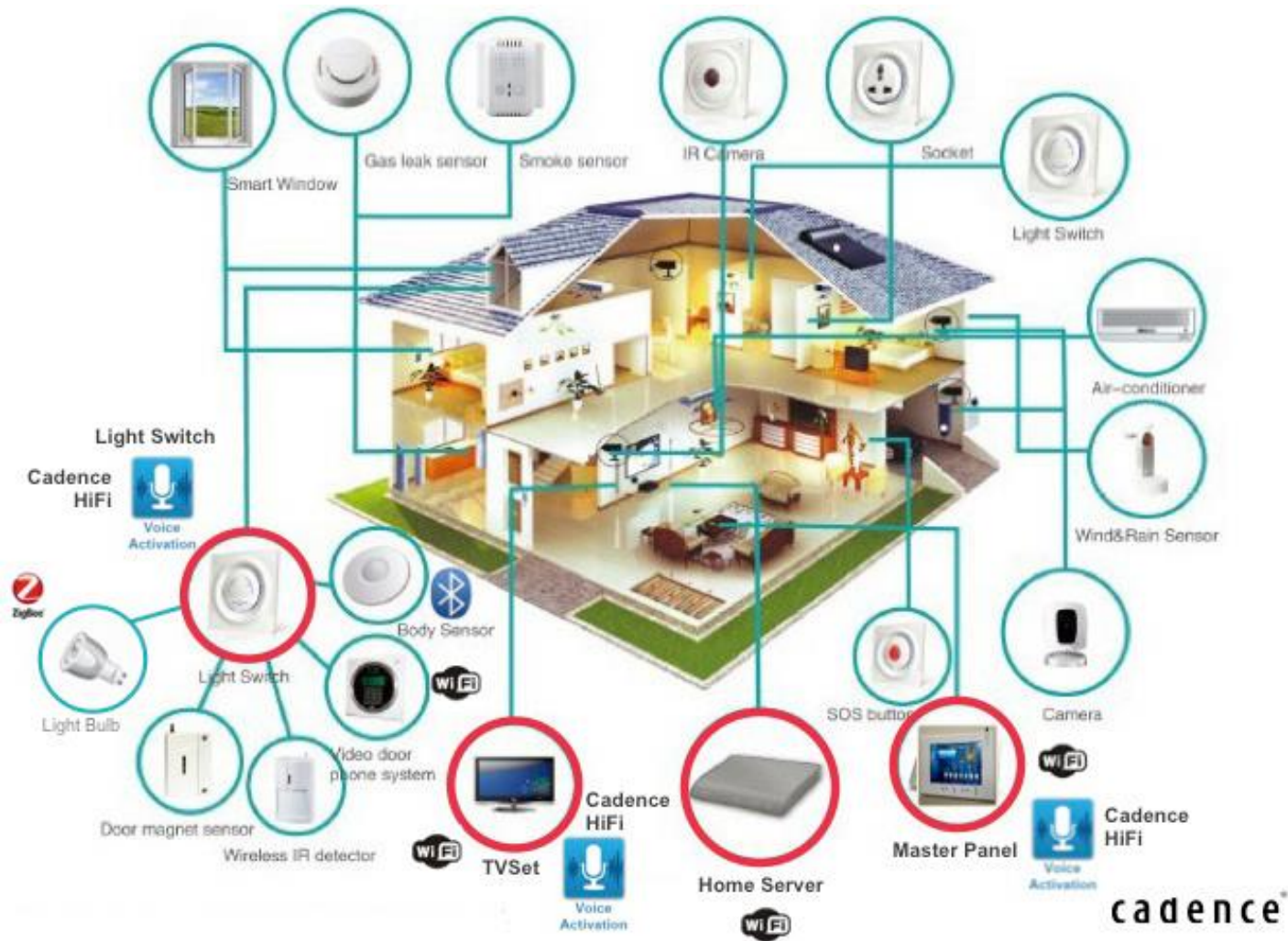
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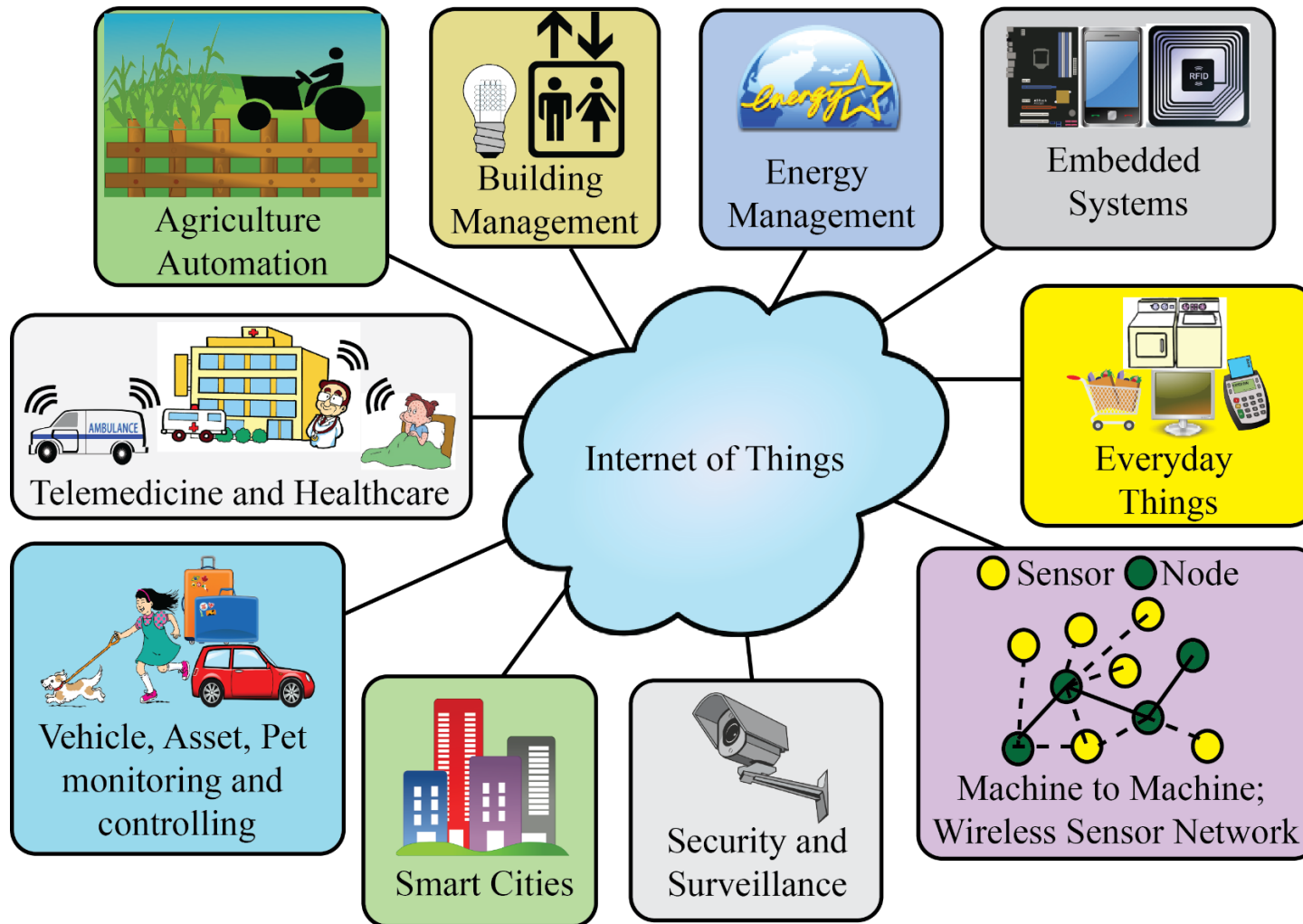


# Smart Home



- Source: Cadence

# What Makes Smart Cities Feasible?



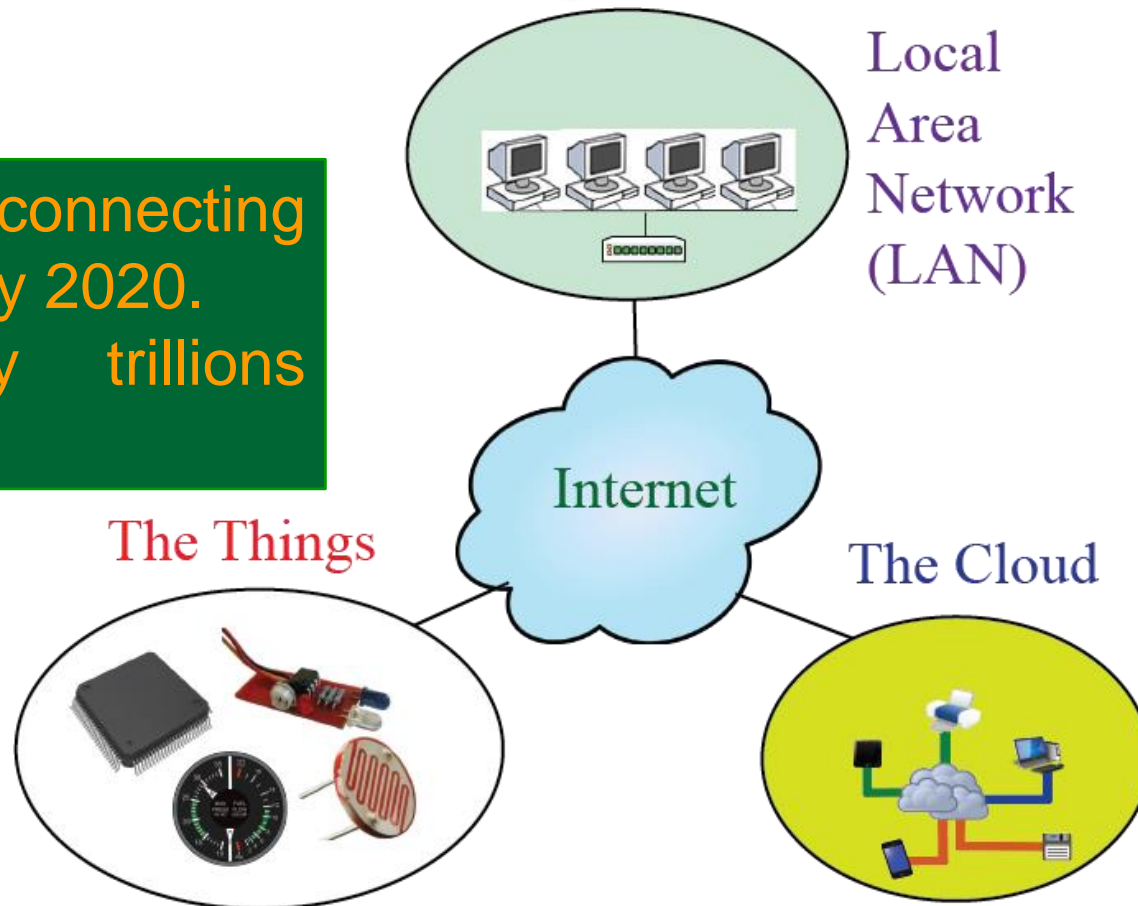
3 key features of Smart Cities come from IoT:

- Intelligence
- Interconnection
- Instrumentation

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# Internet of Things: Architecture

- ❖ 75 billion connecting devices by 2020.
- ❖ Eventually trillions of things.



## ❖ Overall architecture:

- ❖ A configurable dynamic global network of networks
- ❖ Systems-of-Systems

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# Internet of Things: Challenges ...

- Massive Scaling
- Architecture and Dependencies
- Creating Knowledge and Big Data
- Robustness
- Security and Privacy
- Energy Consumption
- Design and Operation Cost

❖ 75 billion connecting devices by 2020.  
❖ Eventually trillions of things.

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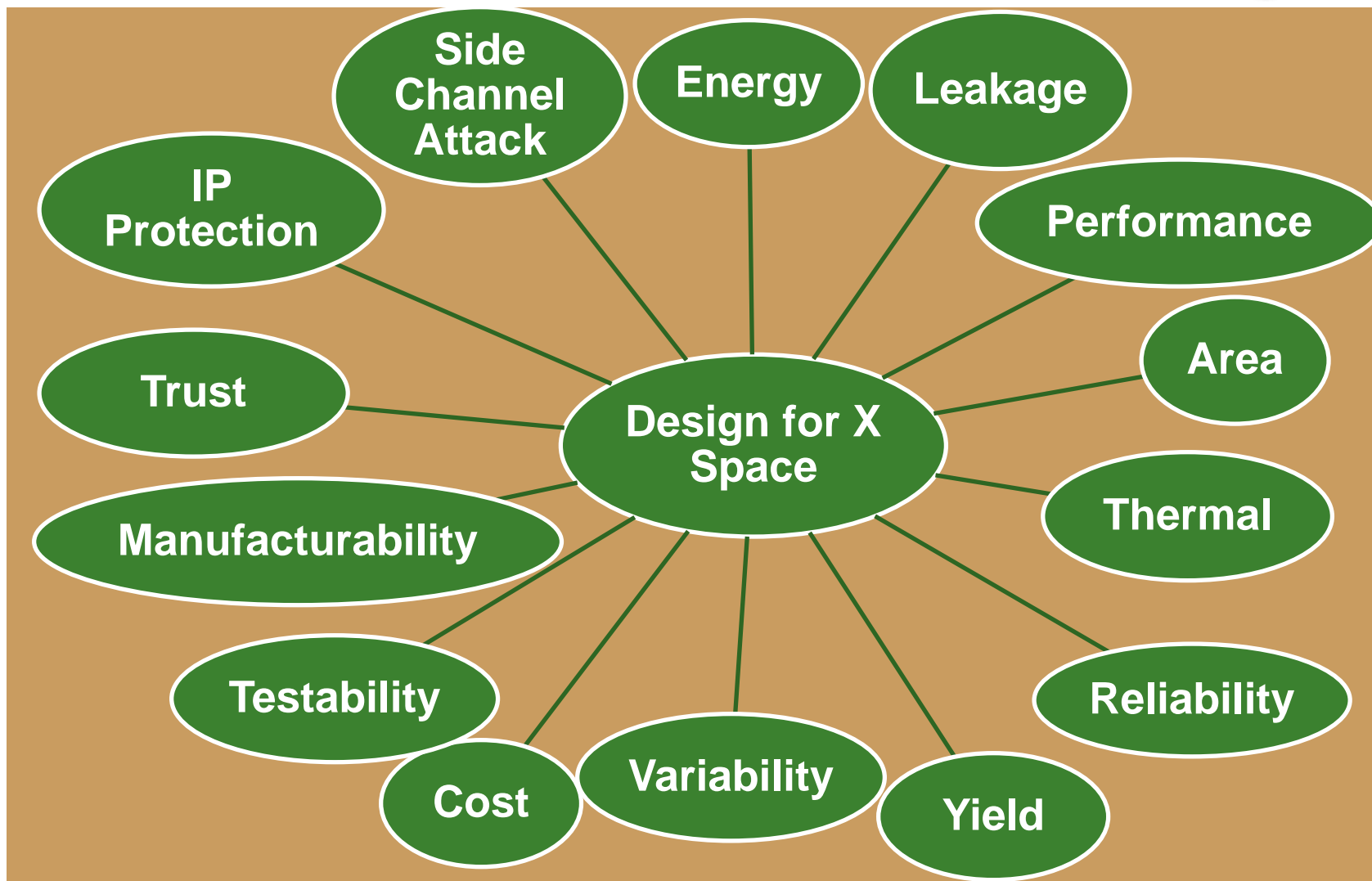


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# Internet of Things: Challenges

- Traditional controllers and processors do not meet IoT requirements, such as multiple sensor, communication protocol, energy consumption, and security requirements.
- Existing tools are not enough to meet challenges like time-to-market, complexity, design cost of IoT.
- Can a framework be developed for simulation, verification, and optimization:
  - ❑ of individual (multidiscipline) “Things”
  - ❑ of IoT Components
  - ❑ of IoT Architecture

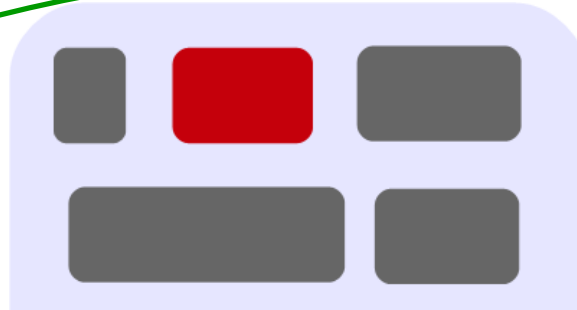
# How to Handle DfX in IoT Design?



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# A Solution - iVAMS

iVAMS




Verilog-AMS Description  
at a Specific Higher  
Abstraction

System-Level Speed Meets Design-Level Accuracy


Metamodels

Behavioral Model

- Model complexity  $\neq$  circuit complexity
- Layout-accurate simulation
- Suitable for design exploration



$y = f(x_1, x_2, x_3, \dots)$



Model of a Specific Lower Abstraction



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# iVAMS code : OP-AMP Example

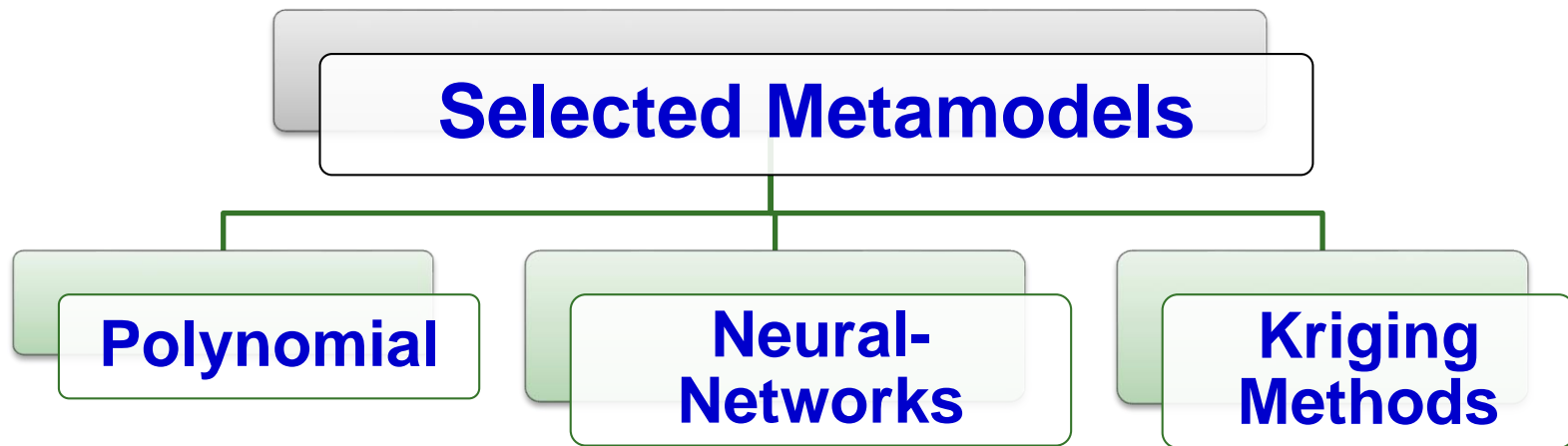
```
function real NN_metamodel; ... ..
integer  $\alpha_1$ ,  $\beta_2$ , b1, b2, i, j, readfile, ... ...; real w, b, v, u;
// Read metamodel weights and bias from text files.
//  $\alpha_1$ ,  $\beta_2$ , b1, and b2.
... .. v = 0.0;
for (j = 0; j < nl; j = j + 1)
begin
    u = 0.0;
    for (i = 0; i < size_x; i = i + 1)
        begin
            readfile = $fscanf(w1, "%e", w);    u = u + w * x[i];
        end
            readfile = $fscanf(w2, "%e", w); readfile = $fscanf(b1, "%e", b);
            v = v + w * tanh(u + b);
        end
            readfile = $fscanf(b2, "%e", b);
    NN_metamodel = v + b; ... ..
end function
```



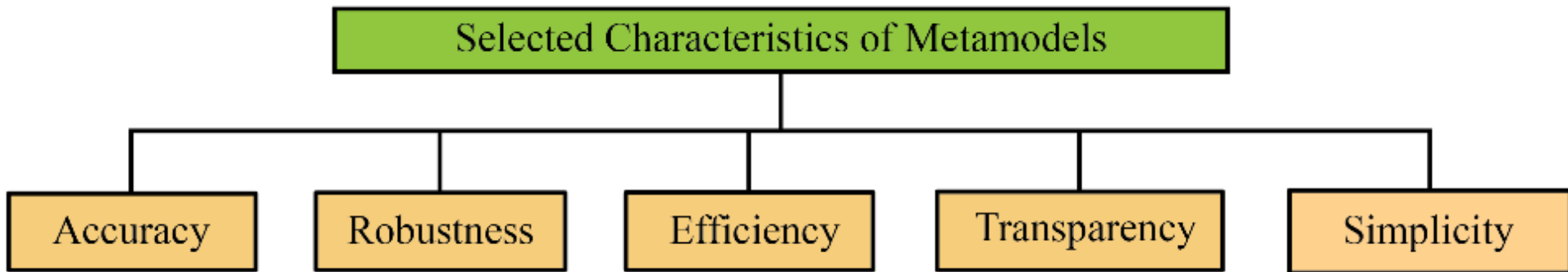
# What are Metamodels?

- “Model of a model” -- Metamodels are mathematical function(s) used to represent the computer simulation models – e.g. polynomial functions, DOE predictive functions, neural networks, and Kriging interpolation:

$$\hat{F}(x_n) = F(x_n) + \varepsilon \approx F(x_n)$$



# iVAMS : Key Characteristics



# iVAMS: Polynomial Metamodel (POM)

- ❖ The OP-AMP characteristics are estimated using POlynomial Metamodel (POM).

Gain

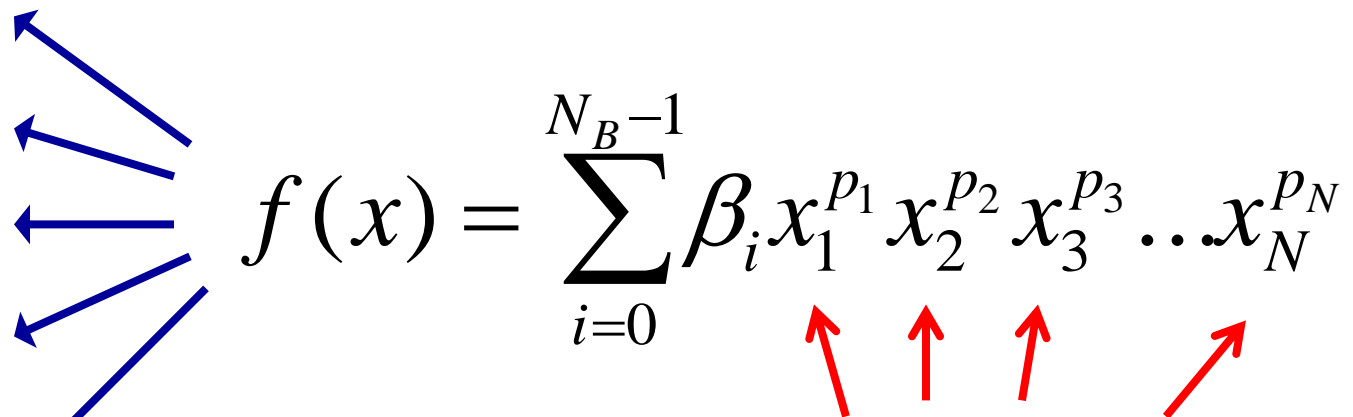
Bandwidth

Phase Margin

Slew Rate

Power

·  
·  
·



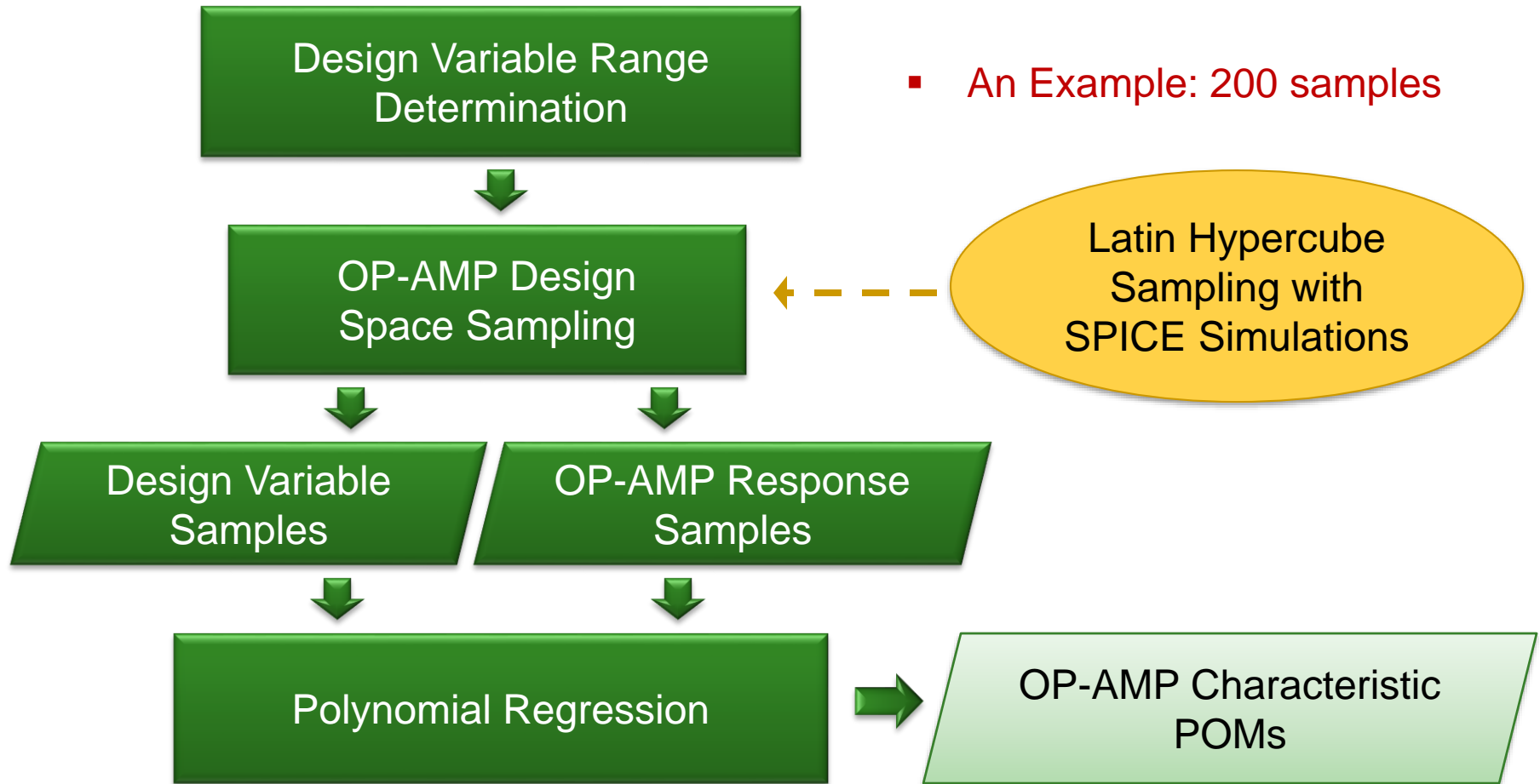
The diagram illustrates the Polynomial Metamodel (POM) equation,  $f(x) = \sum_{i=0}^{N_B-1} \beta_i x_1^{p_1} x_2^{p_2} x_3^{p_3} \dots x_N^{p_N}$ . On the left, a list of OP-AMP characteristics (Gain, Bandwidth, Phase Margin, Slew Rate, Power, and three dots) has blue arrows pointing towards the equation. Below the equation, a green oval contains the text "Transistor widths, lengths, bias current, ..." with four red arrows pointing upwards to the variables  $x_1, x_2, x_3,$  and  $x_N$  in the equation.

$$f(x) = \sum_{i=0}^{N_B-1} \beta_i x_1^{p_1} x_2^{p_2} x_3^{p_3} \dots x_N^{p_N}$$

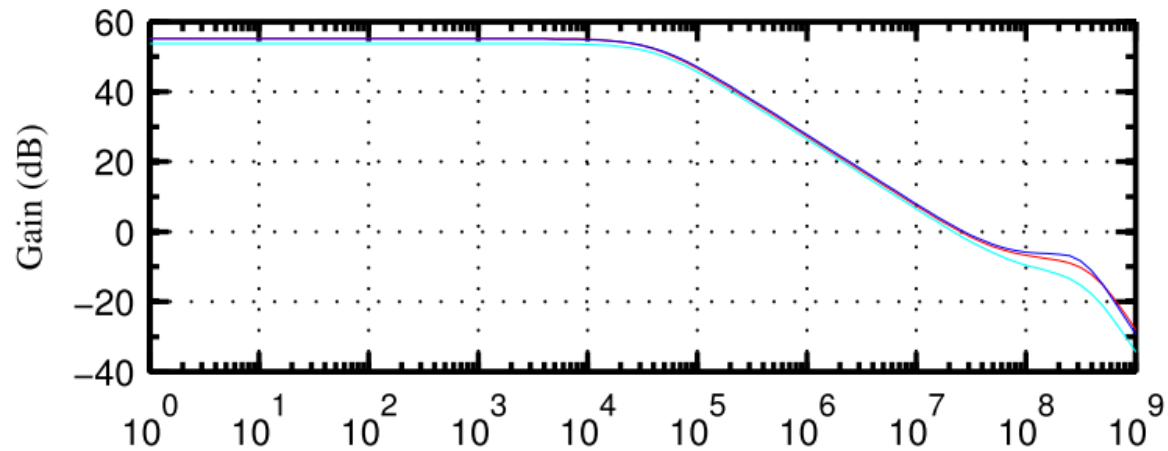
Transistor widths,  
lengths, bias current,  
...

# OP-AMP POM Generation

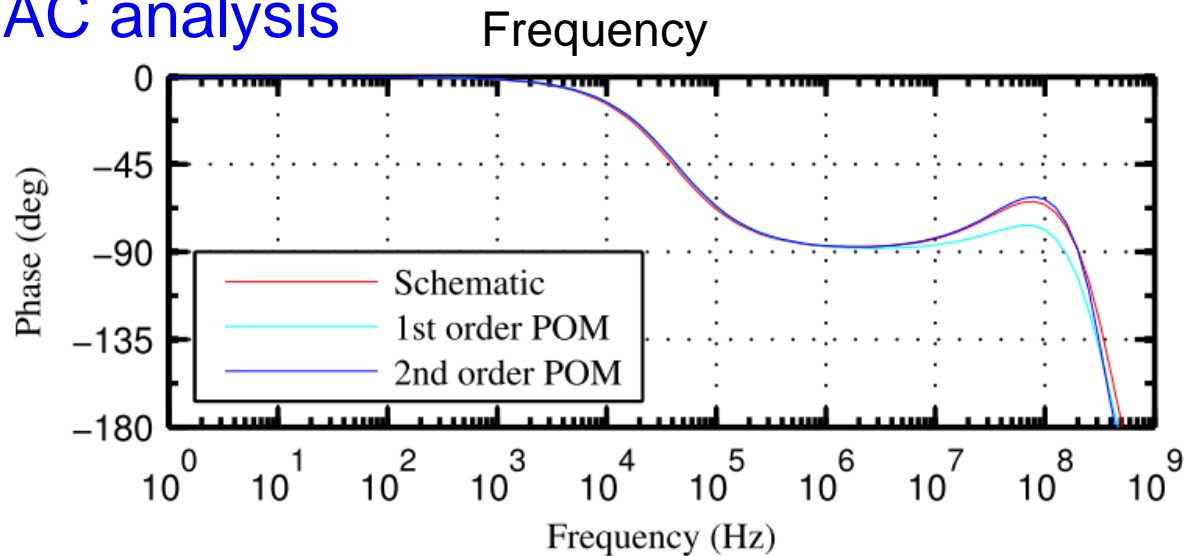
- ❖ The goal is to find the coefficients for the polynomials.



# iVAMS: Accuracy Analysis for OP-AMP

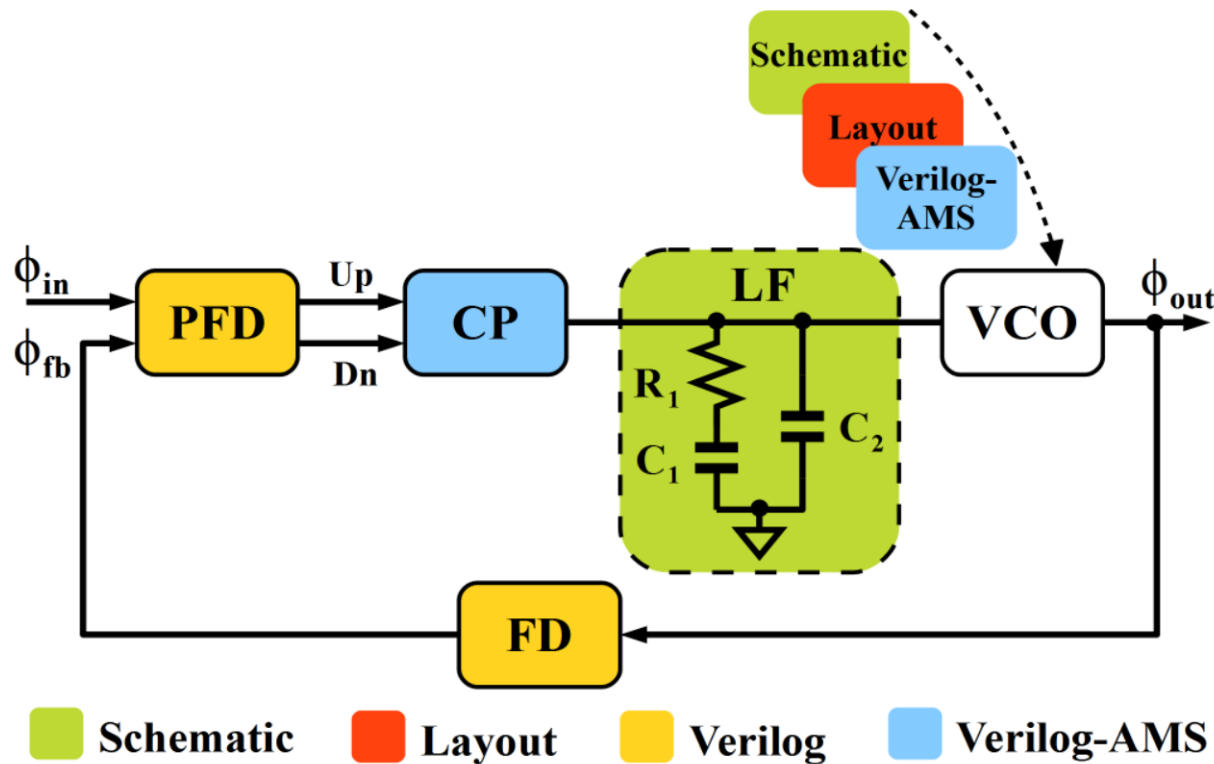


## ❖ Example: AC analysis





# Case Study Electronic Design: PLL



Polynomial Metamodel

$$f(X) = \sum_{i=0}^{K-1} \beta_i x_1^{P_{1i}} x_2^{P_{2i}} x_3^{P_{3i}}$$

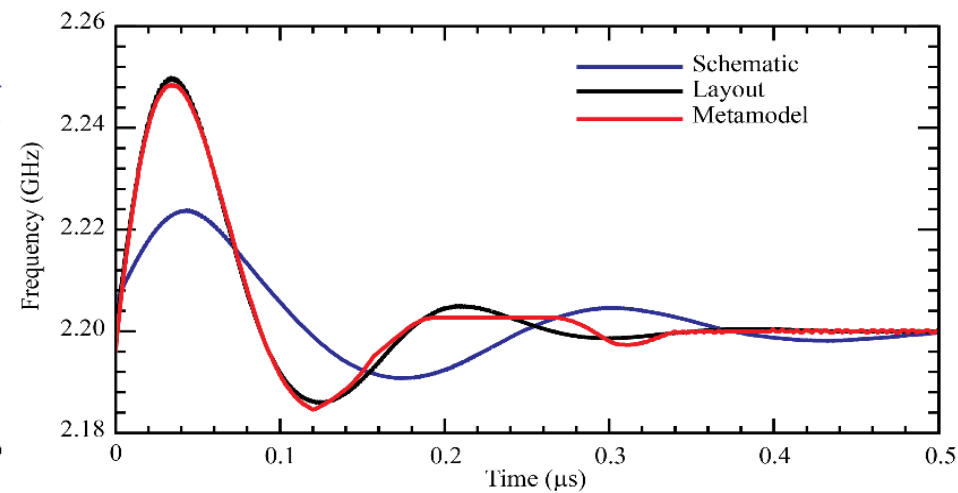
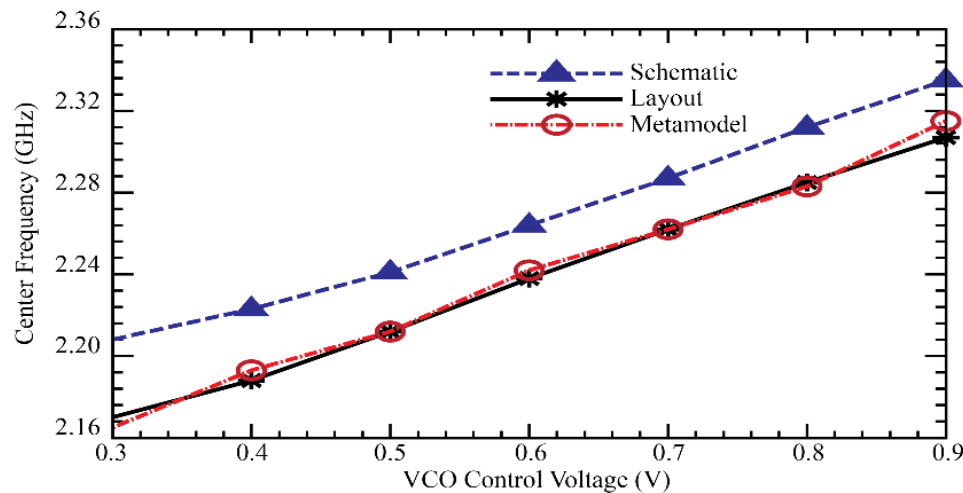
$$x_1 \rightarrow W_P$$

$$x_2 \rightarrow W_N$$

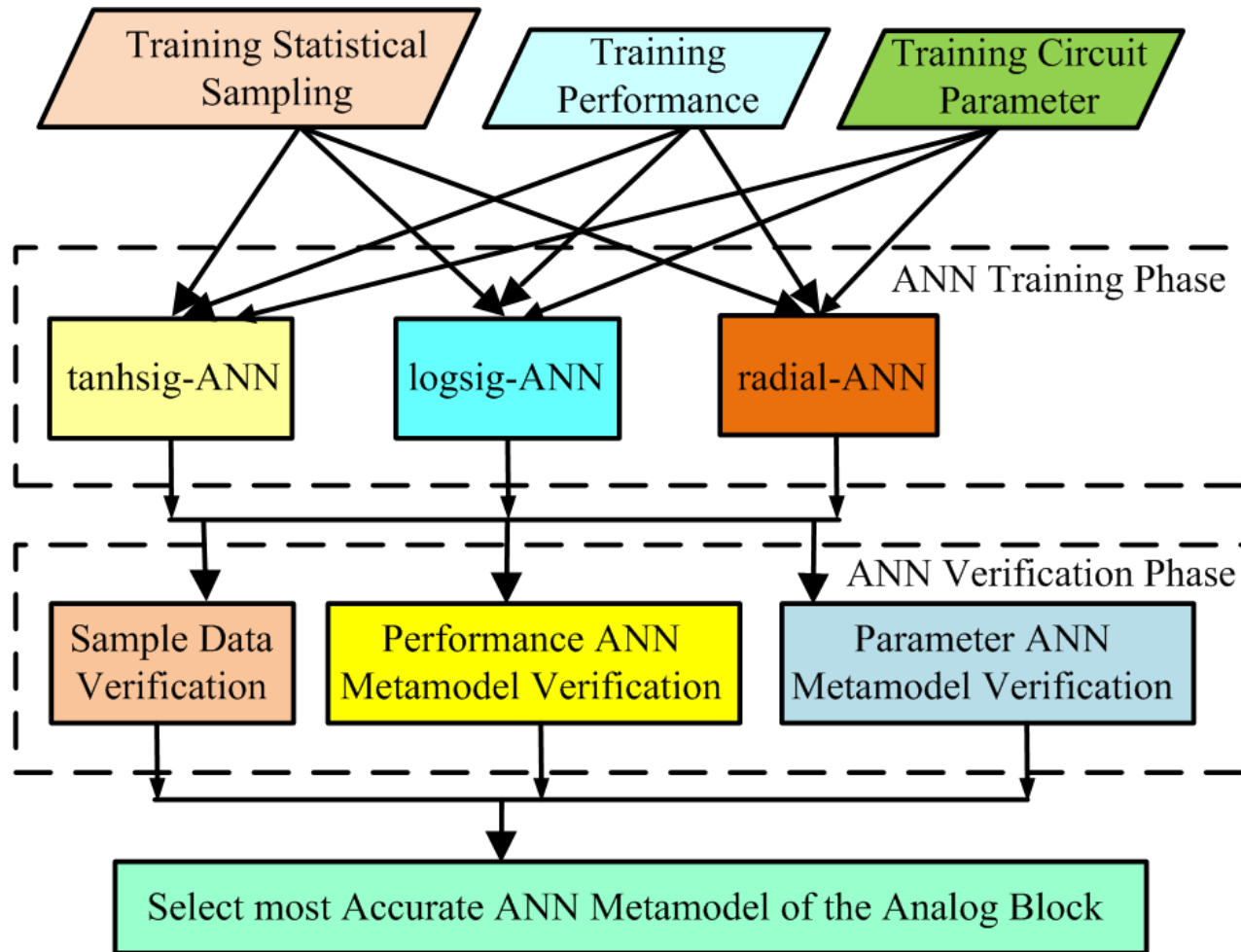
$$x_3 \rightarrow V_{in}$$

# iVAMS: Accuracy Analysis for PLL

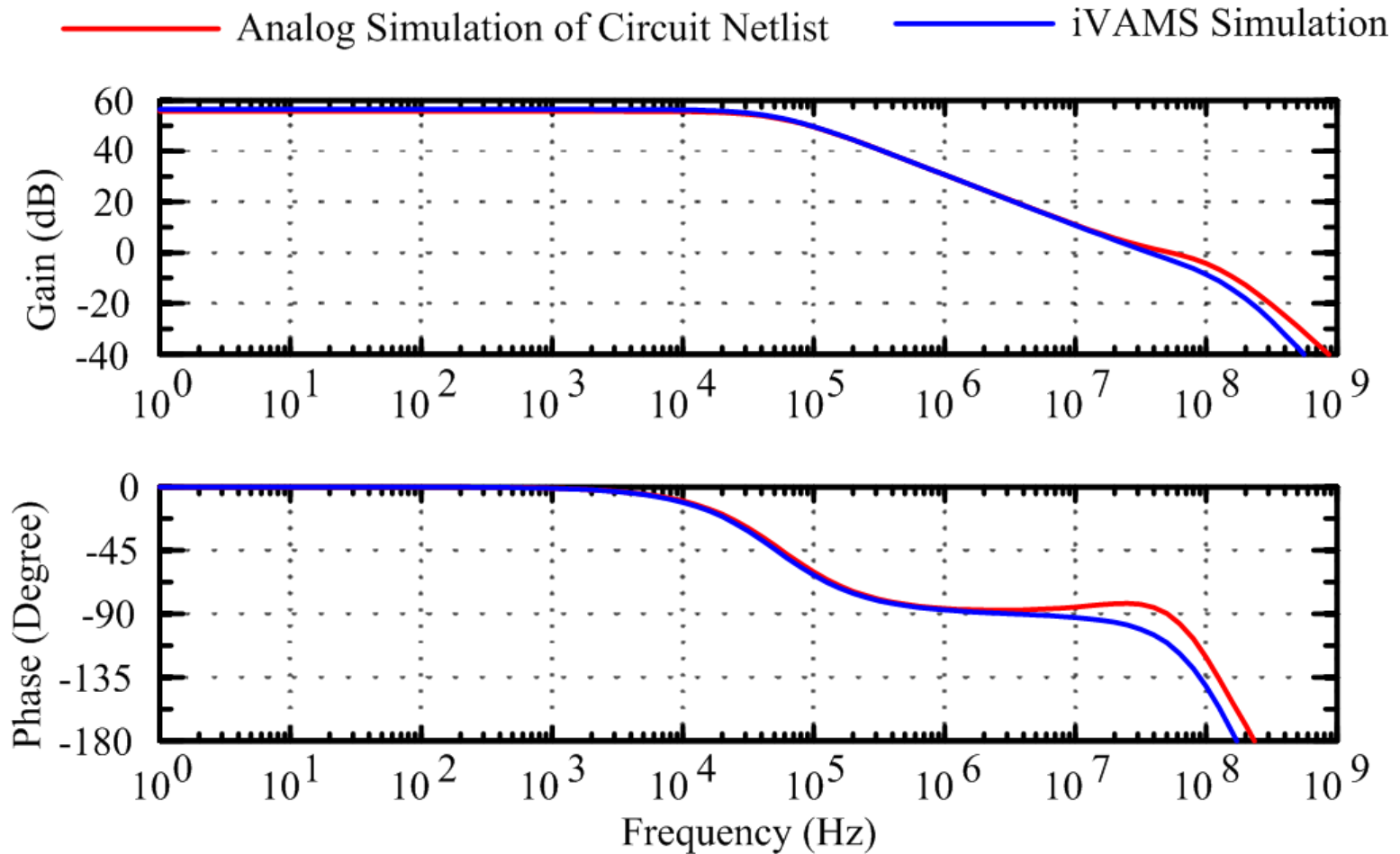
- iVAMS is capable of layout-accurate PLL design characteristics such as, center frequency, power dissipation, and jitter.



# iVAMS : NN Metamodel Architecture Selection

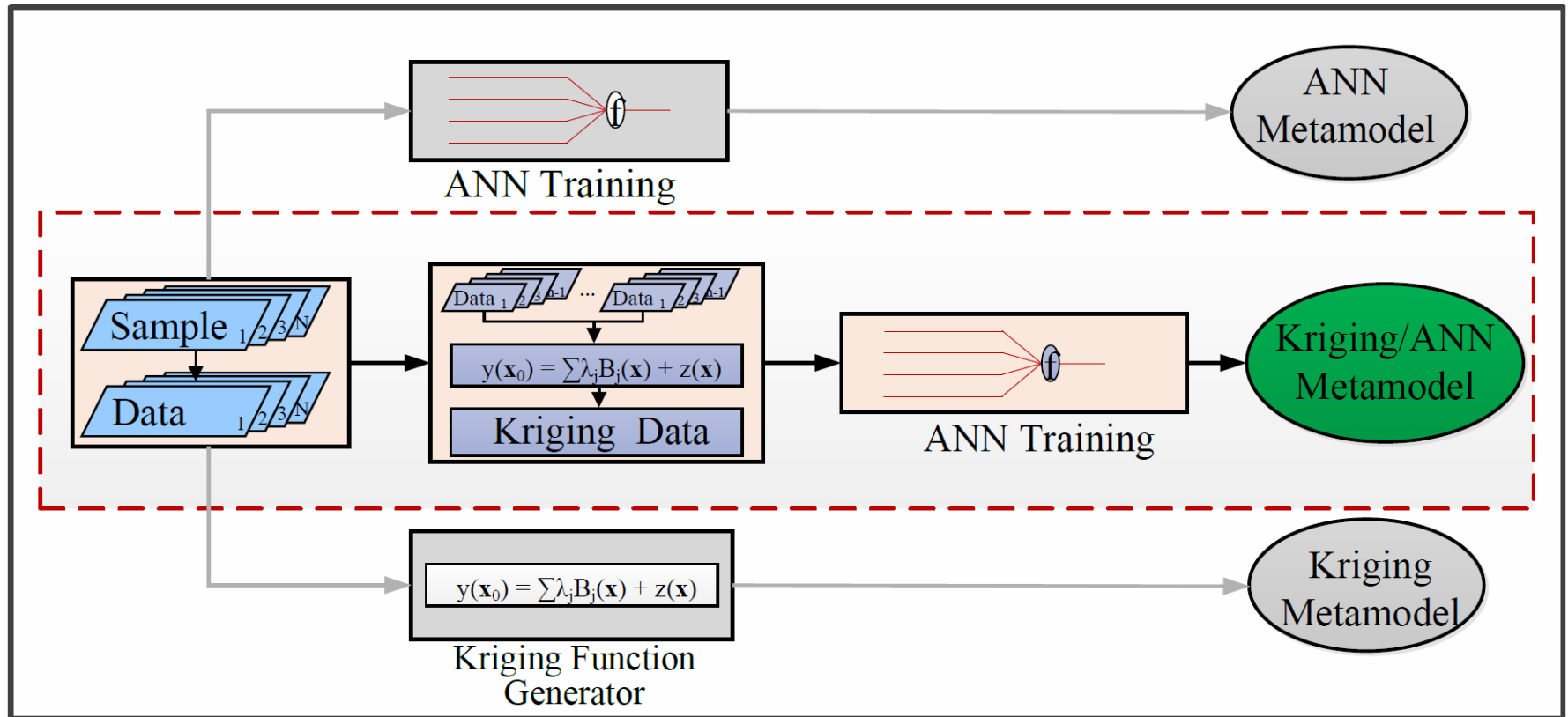


# iVAMS : AC Analysis for Comparison



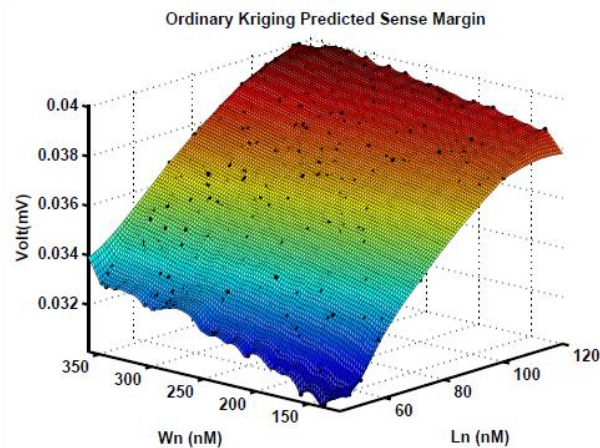
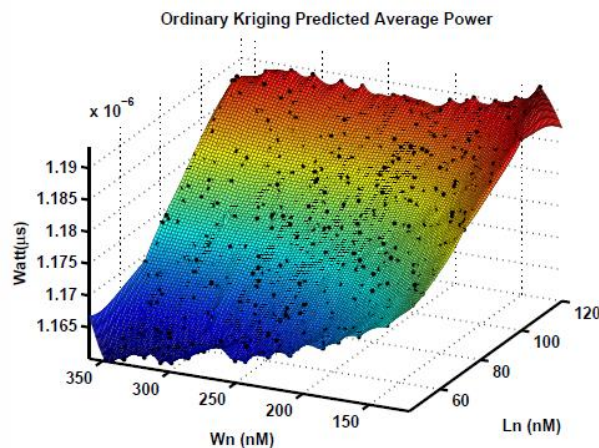
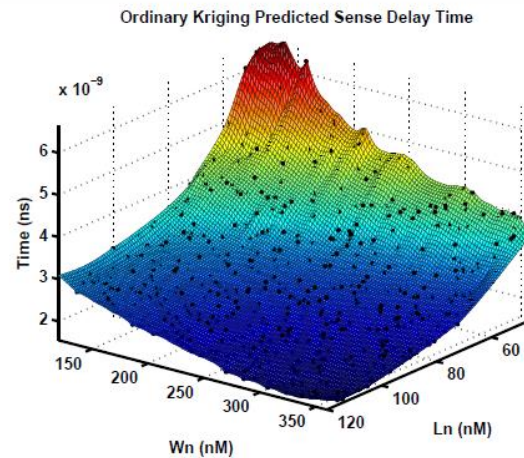
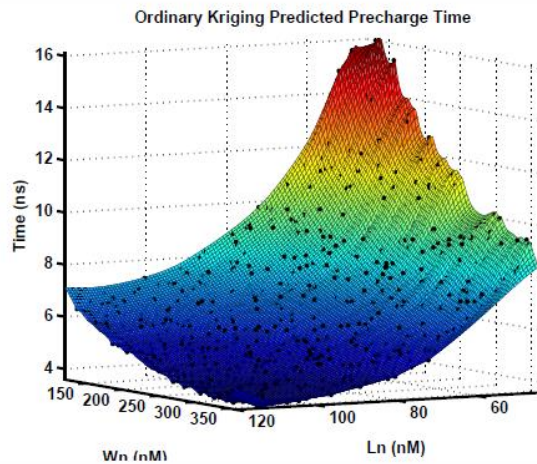
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# Kriging Bootstrapping NN Metamodel





# Ordinary Kriging Metamodels



For a Sense Amplifier Design

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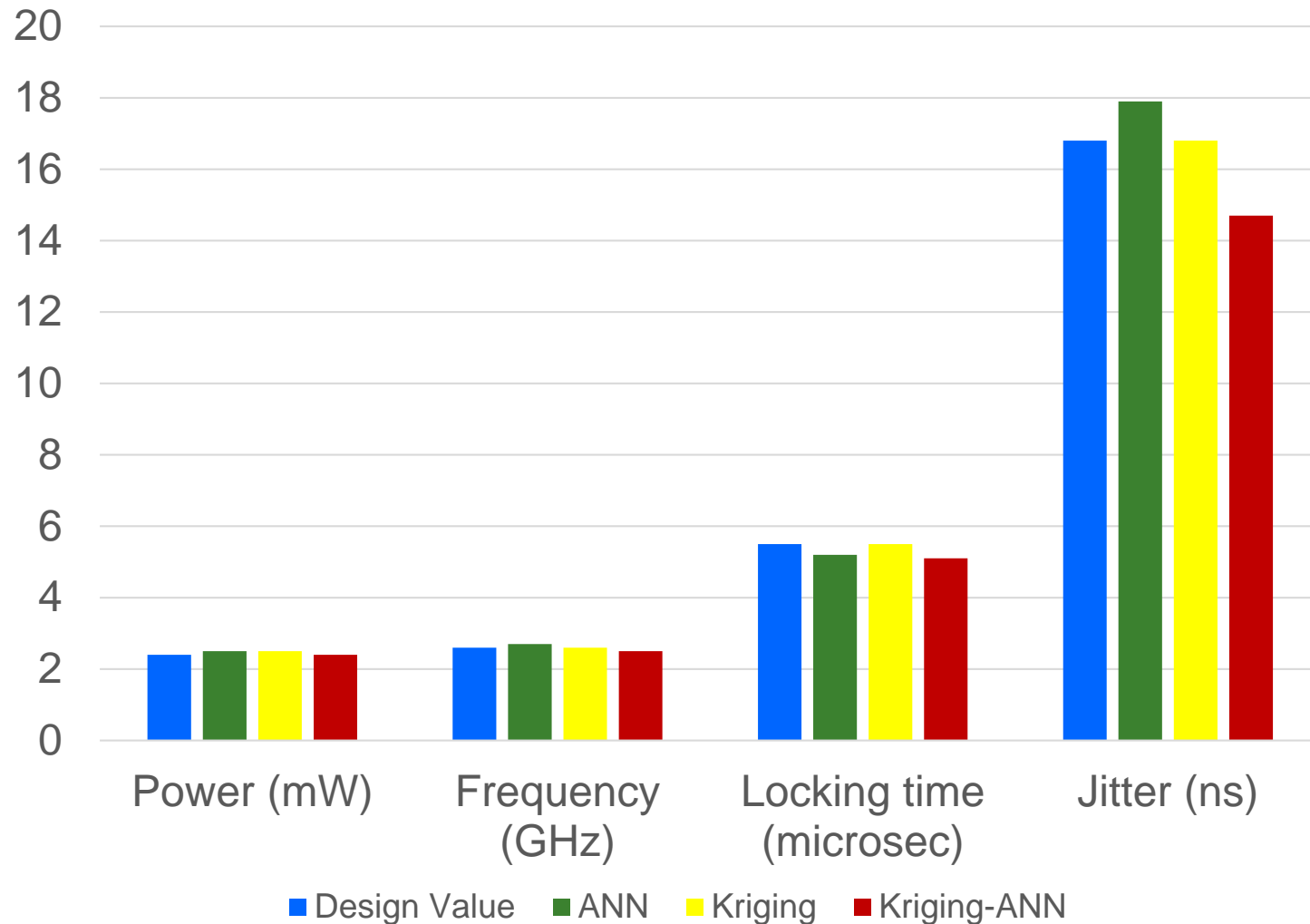
# Metamodel Comparison: Polynomial Vs Nonpolynomial

180nm CMOS PLL with Target Specs:  $f = 2.7\text{GHz}$ ,  $P = 3.9\text{mW}$ ,  $8.5\mu\text{s}$ .

Figures-of-Merits (FoM)	Polynomial # of Coefficients	RMSE	Nonpolynomial (Neural Network)
Frequency	48	77.9 MHz	48 MHz
Power	50	2.6 mW	0.29 mW
Locking Time	56	1.9 $\mu\text{s}$	1.2 $\mu\text{s}$

- 56% increase in accuracy over polynomial metamodels.
- On average 3.2% error over golden design surface for NN metamodels.
- Nonpolynomial is more suitable for large design.

# Nonpolynomial Metamodel Accuracy



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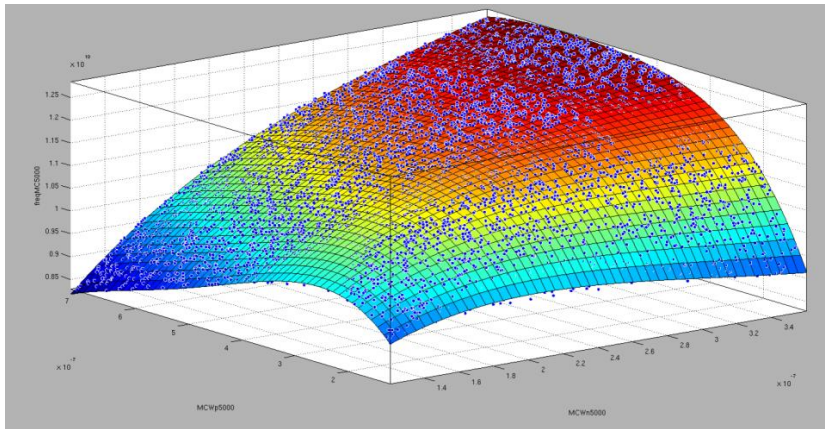


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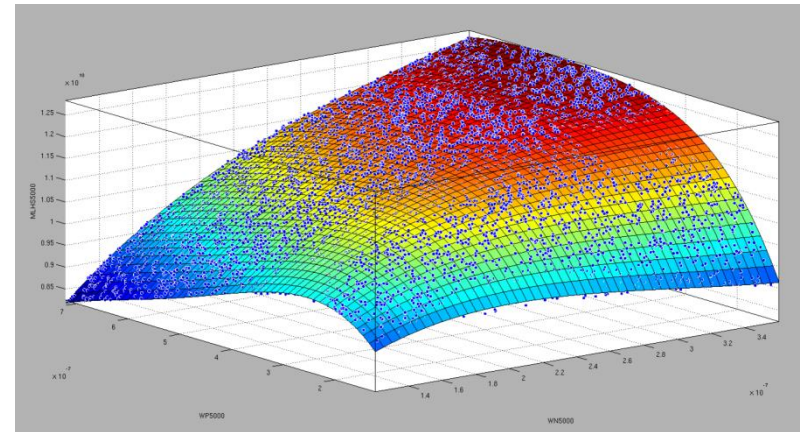


# Sampling Techniques: 45nm Ring Oscillator Circuit (5000 points)

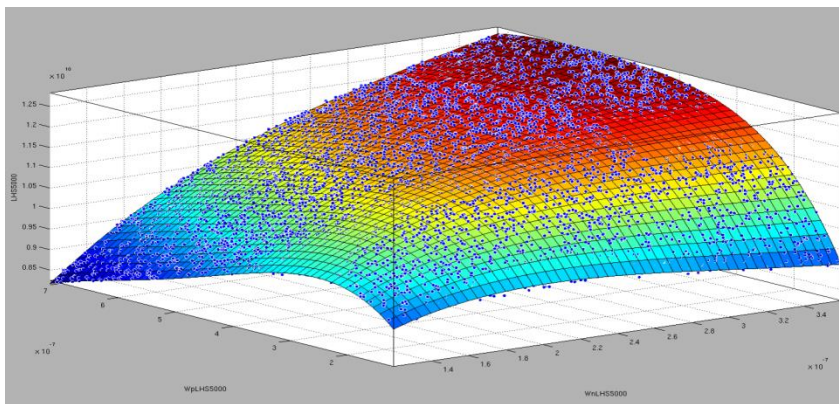
Monte Carlo



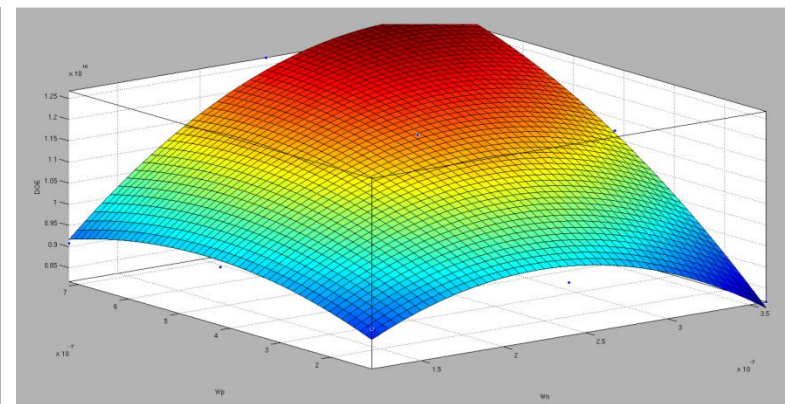
MLHS



LHS

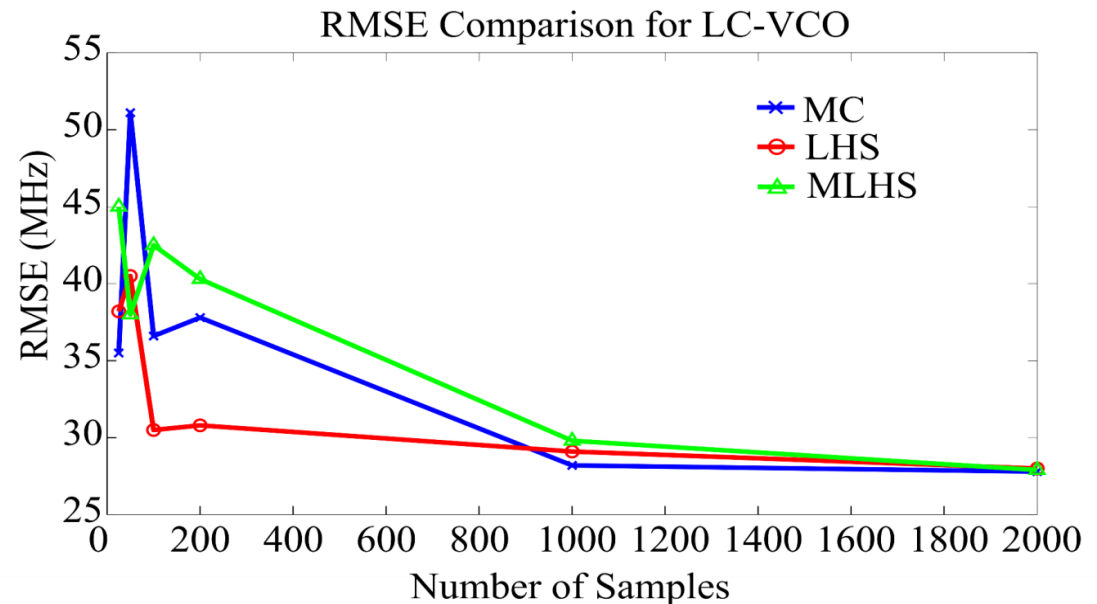
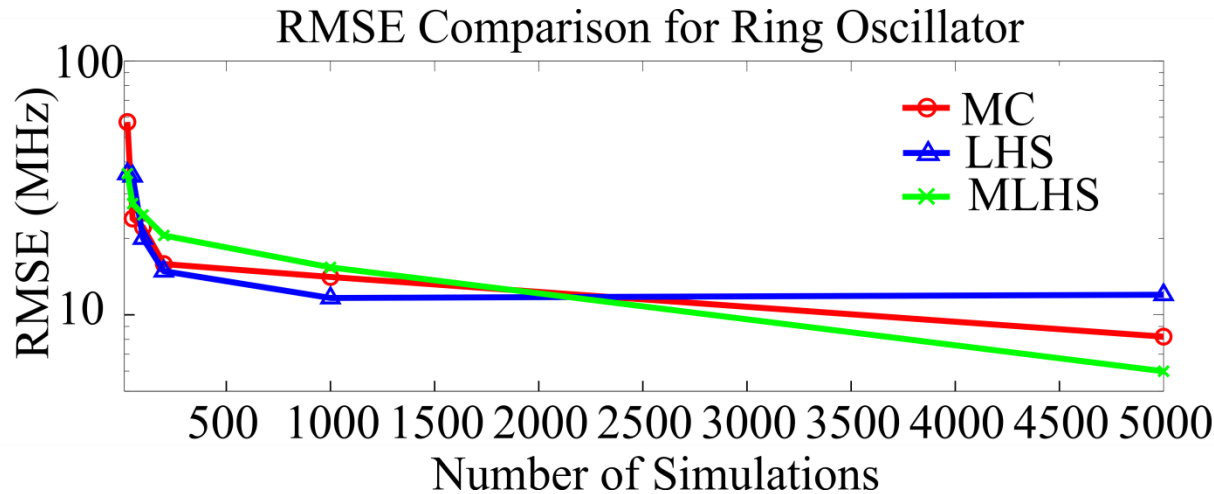


DOE



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# Sampling Comparison: RO / LC-VCO



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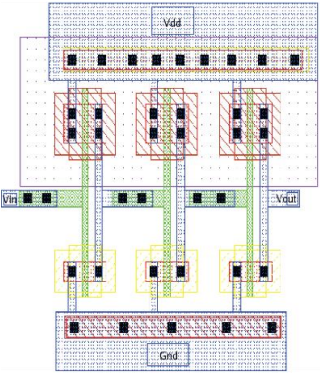


# What do we with iVAMS ?

- Use for accurate design verification
- Use for ultra-fast design optimization

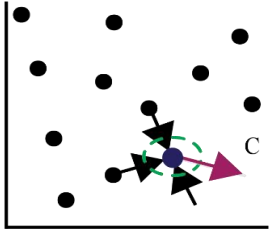
# iVAMS-Based Ultrafast Design Flow

## Baseline Layout of an AMS-SoC Component

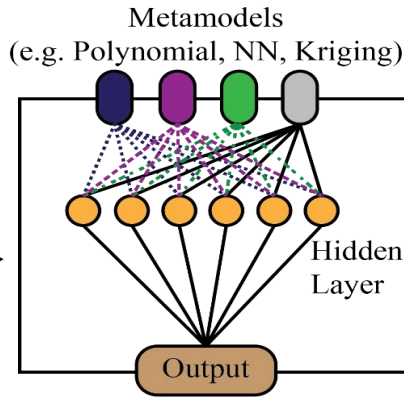


# SPICE Netlist

## Design Space Sampling

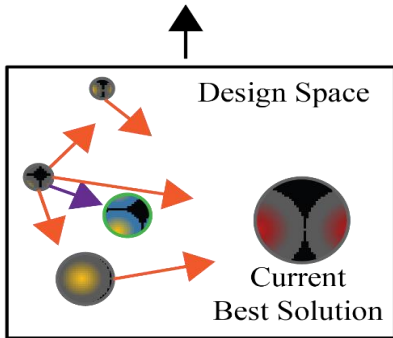


## Metamodel Generation



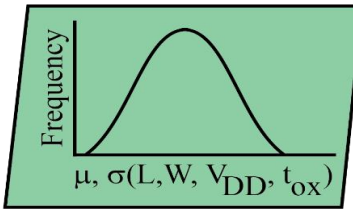
iVAMS  
Generated

## Optimal Design Variables for Baseline Design Modification

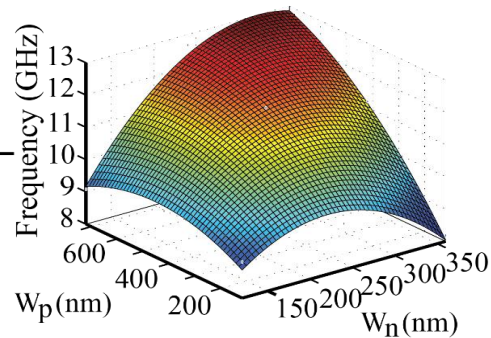


### Optimization Algorithm

## Device Parameter Statistical Distributions



## Monte Carlo Analysis over Metamodels

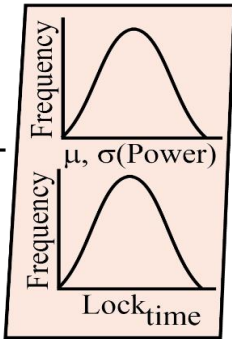


## Design Space Generated From Metamodels

# Optimization over iVAMS

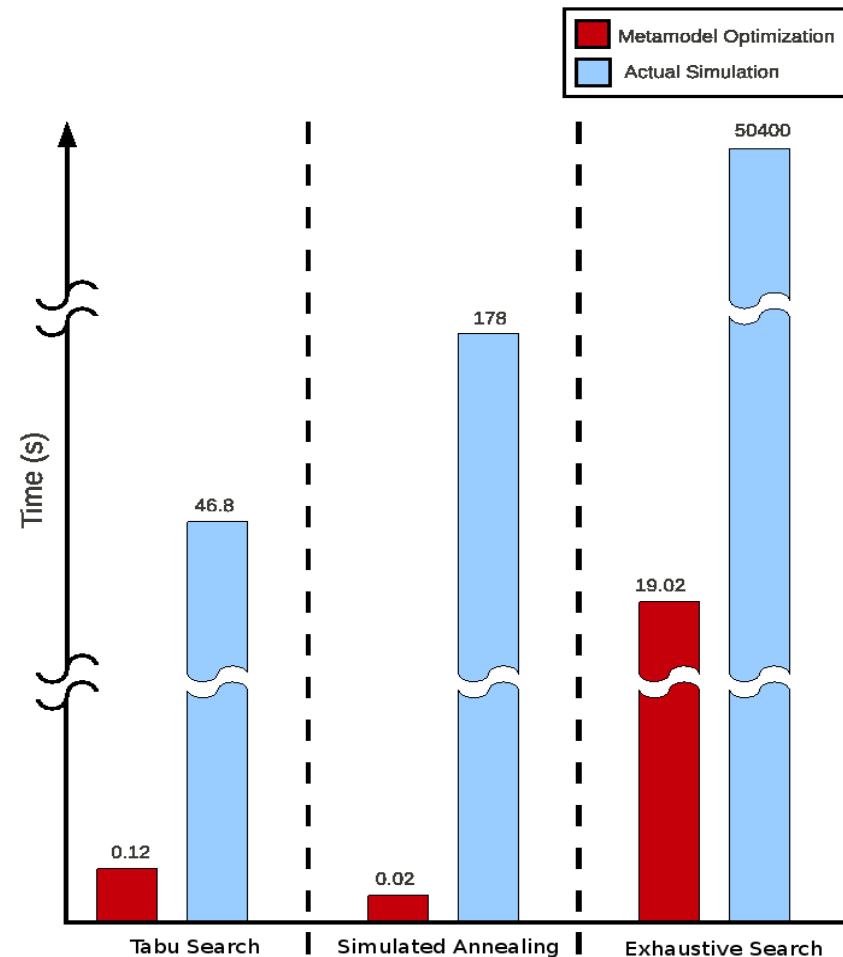
## Distributions of Circuit Characteristics

## Statistical Analysis



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# Comparison of the Running Time: 45nm RO Optimization



- **Optimization without metamodels:** the tabu search optimization is faster by  $\sim 1000\times$  than the exhaustive search and  $\sim 4\times$  faster than the simulated annealing optimization.
- **Optimization with metamodels:** the simulated annealing optimization is faster by  $\sim 1000\times$  than the exhaustive search and  $\sim 6\times$  faster than the tabu search optimization.

# Optimization in PLL: Poly Vs NN

## Bee Colony Optimization Results

FoM	Polynomial Metamodel	NN Metamodel
Average Power	3.9 mW	3.9 mW
Frequency	2.69 GHz	2.70 GHz

## Bee Colony Optimization Time Comparison

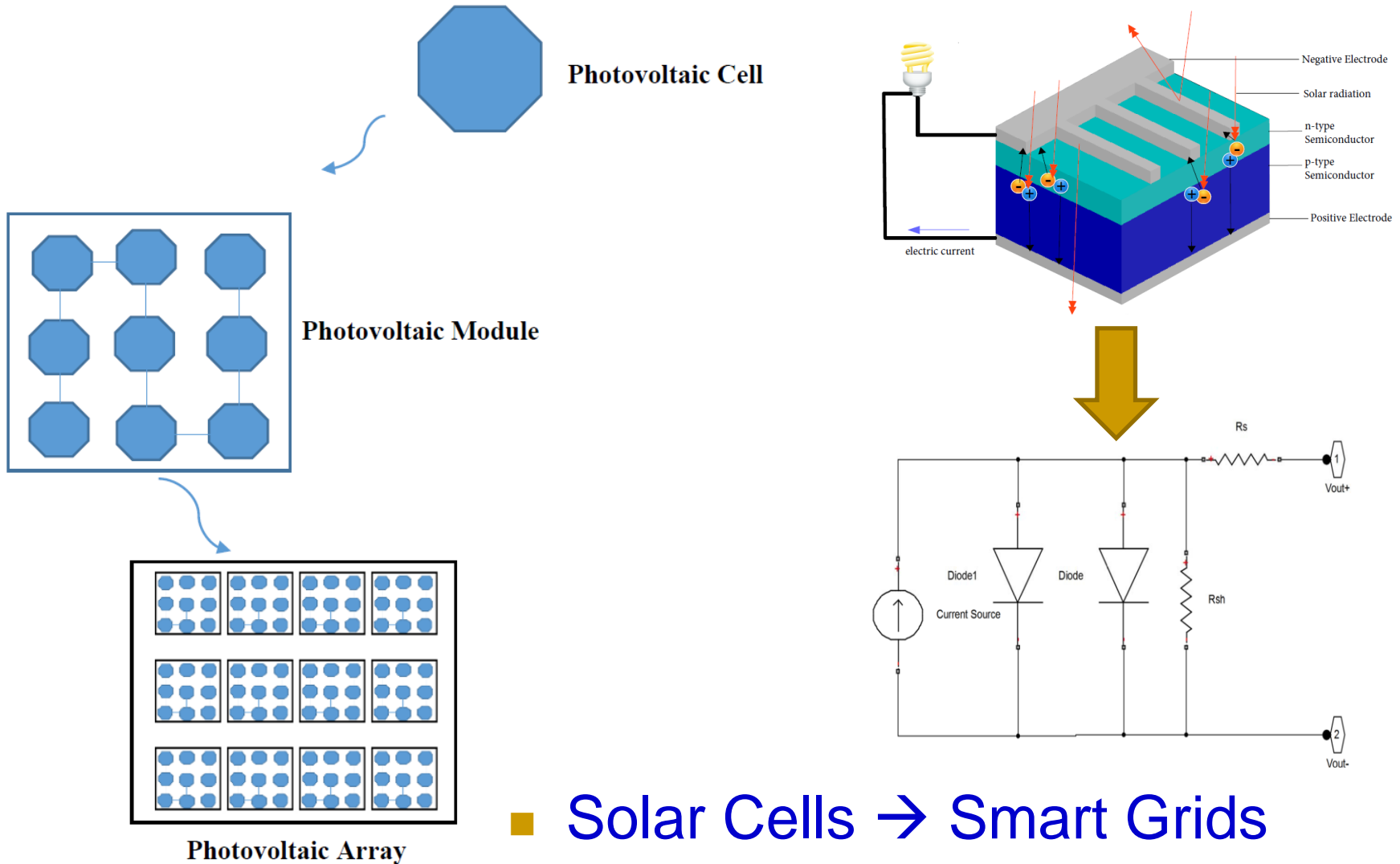
Algorithm	Circuit Netlist	Polynomial Metamodel	NN Metamodel
<b>Bee Colony (100 iterations)</b>	#bees(20) * 5 min * 100 iteration = 10,000 minutes = <b>7 days (worst case)</b>	5 mins	0.12 mins
<b>Metamodel Generation</b>	0	11 hours for LHS + 1 min creation	11 hours for LHS + 10mins training and verification.

# OP-AMP: Optimization Results

Performance	Constraint	Optimal <sub>POM</sub>	Optimal <sub>SCH</sub>
$A_0$ (dB)	$> 43$	56.4	52.8
BW (kHz)	$> 50$	58.9	85.5
PM (degree)	$> 70$	84.4	87.7
SR (mV/ns)	$> 5$	7.1	8
<b>Objective</b>			
$P_D$ ( $\mu$ W)	$\sim 65$	65.5	68.1

Performance	Optimal <sub>SCH</sub>	Optimal <sub>POM</sub>
Power Reduction	$\times 3.71$	$\times 3.86$
Number of iterations	1200	1200
Computation Time	12.5 h	2.6 s
Normalized Speed	1	$\times 17120$

# Ongoing: iVAMS for other “Things”



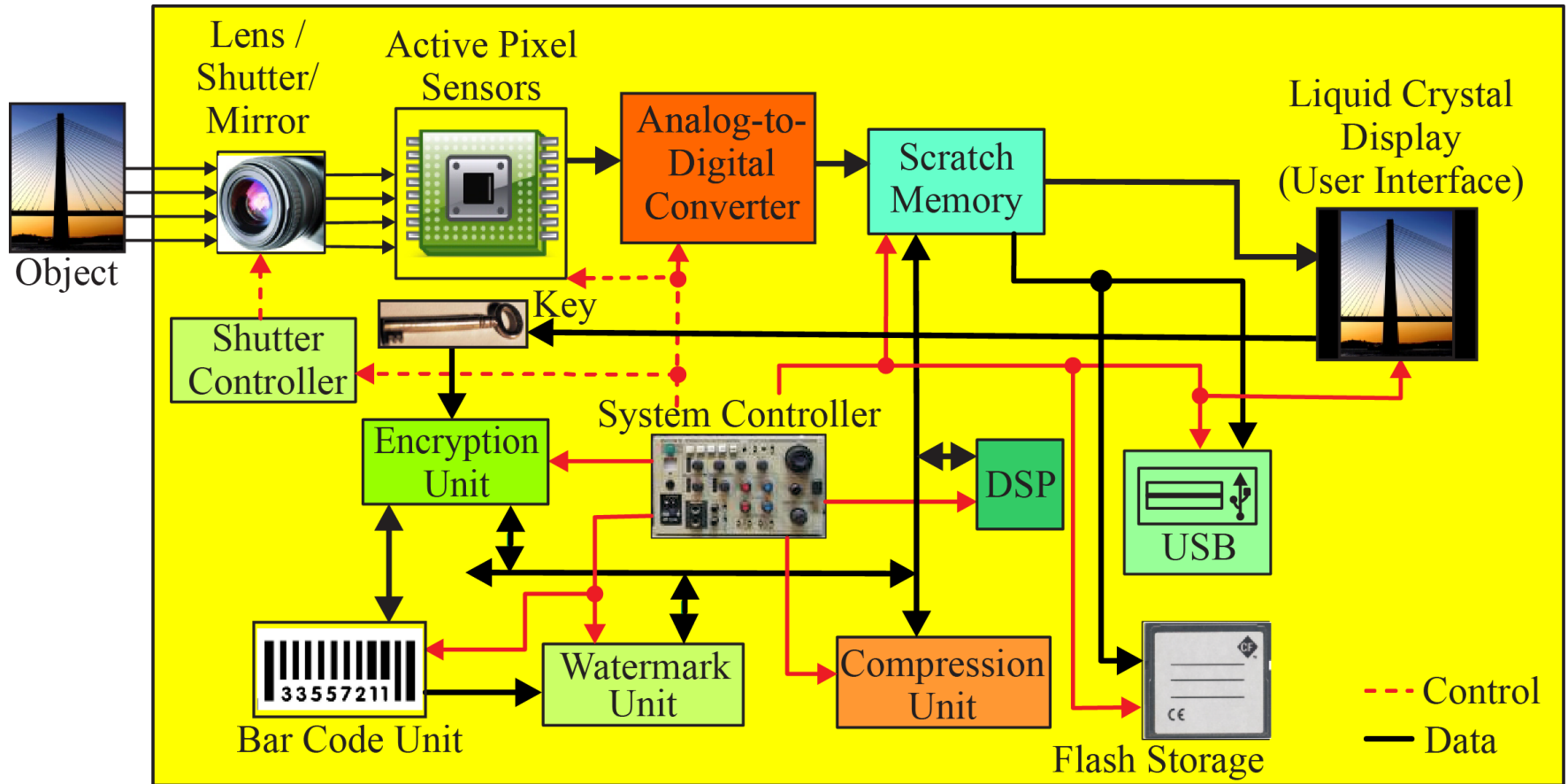
■ Solar Cells → Smart Grids

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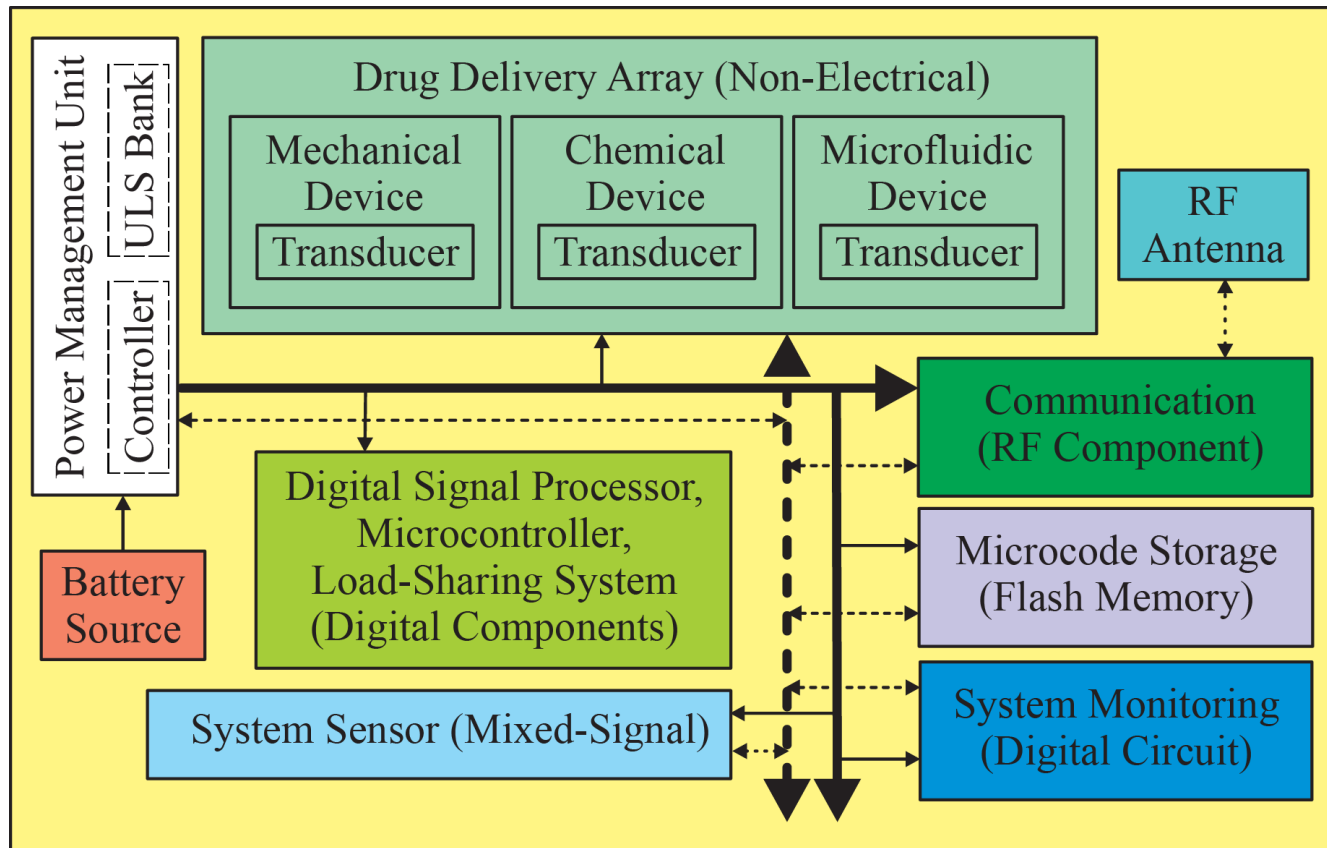
# Ongoing: iVAMS for other “Things”



- Secure Digital Camera: For Secure Imaging/Video

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# Ongoing: iVAMS for other “Things”



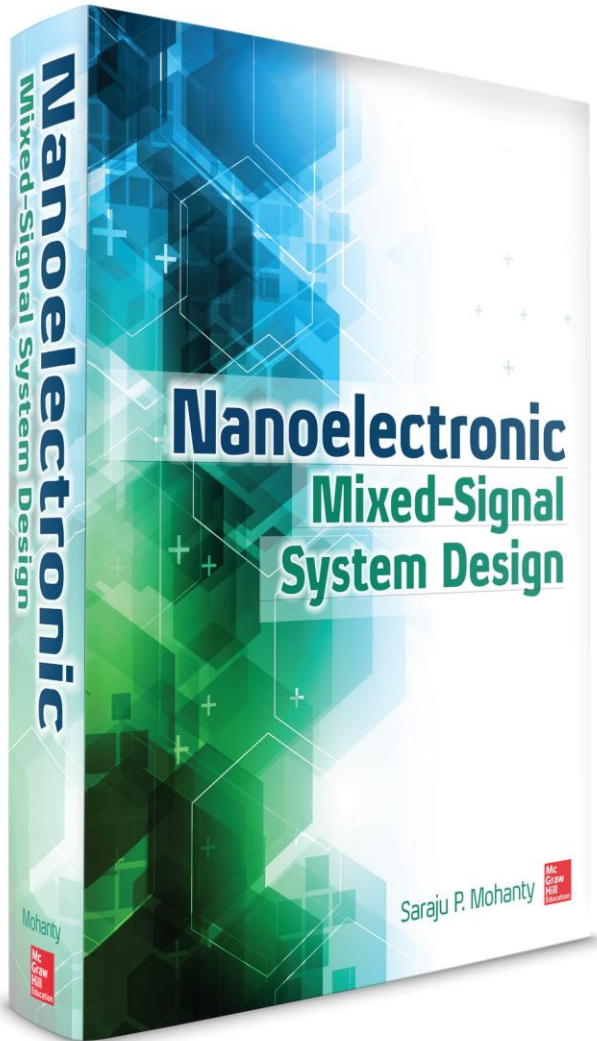
- Nano-Electro-Mechanical-Systems (NEMS) → Smart Health Care

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# Conclusions

- IoT components and “Things” have multifold challenges.
- Intelligent Verilog-AMS (iVAMS) is a unique framework for IoT components simulation, verification, and optimization.
- iVAMS can be used for individual components and architecture following hierarchical approach.
- Use of iVAMS and optimization algorithm speed up the design-space exploration for the design.
- Polynomial metamodels are easier create but can be applied for small designs.
- Increase in accuracy is observed using feed forward neural network over polynomial metamodels.
- Kriging and NN metamodels can handle large designs.
- iVAMS for “multidiscipline” “things” needs research.

# Some Advertisement



- Winner of the Association of American Publishers' 2016 PROSE Award in the Textbook in Physical Sciences & Mathematics category.
- Cutting-edge nanoelectronic mixed-signal system design methods

Design discusses mixed-signal circuit and system design based on existing and emerging nanoelectronic technologies. The book features coverage of both digital and analog applications using nanoscale CMOS and post-CMOS. Key techniques required for design for excellence and manufacturability are discussed in this practice-driven text.

❖ Color lecture slides are available.

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- O. Okobiah, S. P. Mohanty, and E. Kougianos, "Exploring Kriging for Fast and Accurate Design Optimization of Nanoscale Analog Circuits", in *Proceedings of the 13th IEEE Computer Society Annual Symposium on VLSI*, 2014, pp. 244--247.
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- G. Zheng, S. P. Mohanty, E. Kougianos, and O. Okobiah, "iVAMS: Intelligent Metamodel-Integrated Verilog-AMS for Circuit-Accurate System-Level Mixed-Signal Design Exploration", in *Proceedings of the 24th IEEE International Conference on Application-specific Systems, Architectures and Processors*, 2013, pp. 75--78.



A close-up, slightly blurred image of a blue microchip with a central square area containing a smaller chip. The chip is surrounded by numerous gold pins. The background is a soft-focus grid pattern.

# Thank You !!!

Slides Available at:  
<http://www.smohanty.org>