A Low-Cost Mixed Clock Generator for High Speed Adiabatic Logic

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Introduction

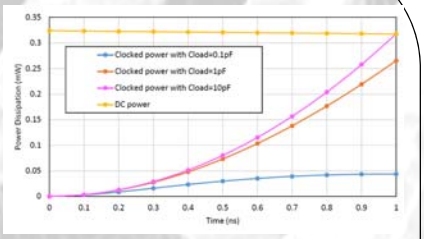
- Adiabatic logic is one of effective methods of low power VLSI design. The essence of adiabatic logic includes lowering charging speed and clocked power supply, both of which can reduce power dissipation to a large degree.
- How to drive adiabatic logic using clocked power decides the performance of following system.
- Currently mainstream adiabatic systems need four-phase clocked power to achieve energy recovery and correct data flow.
- Most of well used clock blocks are built by integrating passive devices, such as tank capacitor, LC oscillator, which occupy more chip area. The mismatch of dimensions also will largely degrade the accuracy of frequency.
- In using TSMC 180nm fabrication process, we propose a novel mixed clock generator with low cost.

Major Contributions

- We mathematically analyzed the slow charge and three types of clocked powers used for adiabatic logic in the view of power dissipation.
- Based on the mainstream designs of clocked power, we propose a novel mixed clock generator without passive devices, driven by a single sinusoidal signal.
- The novel clock generator includes four-phase source, switch controller and clock MUX, all of which are designed in digital IC block.
- We used *SPICE* simulation (TSMC 180nm) to demonstrate the feasibility of our design. The test shows that below 600MHz, the proposed design has negligible signal attenuation with low power dissipation.

Slow Charging in Adiabatic Logic

$$P_{diss} = \frac{V_{DD}^2 t^2}{T^2 R_{ON}} e^{-\frac{2t}{R_{ON} C_{load}}}$$



The larger charging time is, more energy saved. Thus adiabatic logic is a trade-off between power dissipation and speed.

Three ways of clocked power:

- Step clock

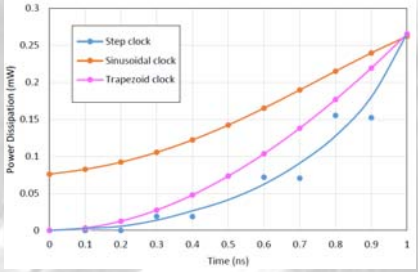
$$P_{diss\_step} = \frac{\left(\frac{V_{DD}}{\alpha}\right)^2 \left[\frac{t}{T_S}\right]^2 e^{-\frac{2T_S}{R_{ON} C_{load}}}}{R_{ON}}$$

- Sinusoidal clock

$$P_{diss\_sin} = \frac{V_{DD}^2 \left[\sin\left(\frac{\pi}{2}\frac{t}{T_{sin}} - \frac{\pi}{4}\right) + 1\right]^2}{4R_{ON}} e^{-\frac{2t}{R_{ON} C_{load}}}$$

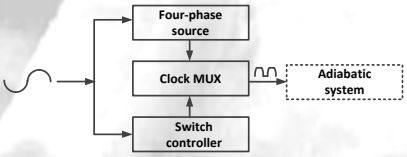
- Trapezoidal clock

$$P_{diss\_trap} = \frac{V_{DD}^2 t^2}{T^2 R_{ON}} e^{-\frac{2t}{R_{ON} C_{load}}}$$

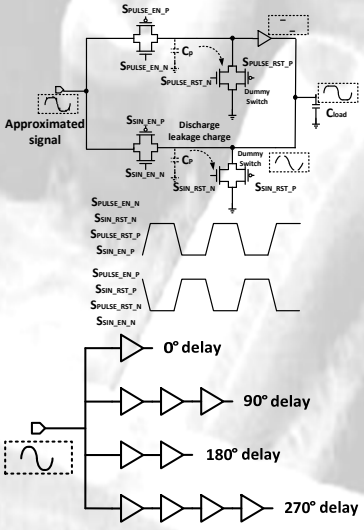


Most clocked power are designed by passive devices.

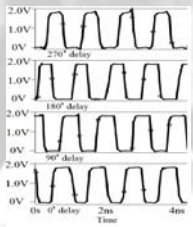
Mixed Clock Generator



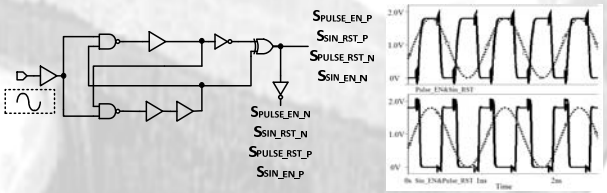
Block Diagram of the Proposed Clock Generator



Clock MUX:
Dummy switch is to let undesired charge leak to the ground to confirm signal accuracy in high speed work.
All of clock signals are built by the switch controller.

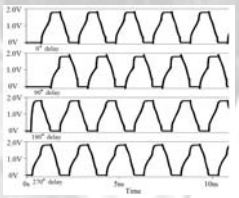


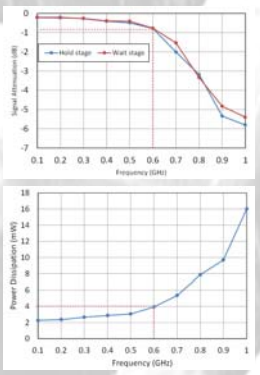
Four-Phase Source: Using Large Dimension Inverters to Construct Different Signals



Switch Controller: Used Non-overlapping clock is modified to construct signals to control MUX.

Results





Simulation Results@500MHz

Performance is acceptable under 600MHz.

Conclusions

- A low cost clocked power is designed without passive devices.
- Further work at the chip level design is being carried-out using this clock generator to drive high speed adiabatic system in 180nm CMOS.