Lecture 11: Efficient Design of Flash ADC

CSCE 6933/5933
Advanced Topics in VLSI Systems

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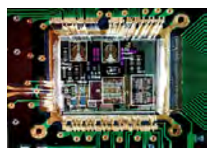
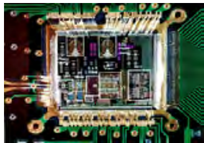
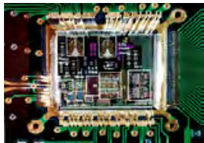


A 45*nm* Flash Analog to Digital Converter (ADC)



Outline

- Introduction and Motivation
- Specifications
- Related Research Works
- Design of flash ADC
- The TIQ principle
- TIQ Comparator
- Sizing of transistors
- Functional Simulation
- Ideal vs Actual Characteristics
- DNL
- INL
- SNDR
- Instantaneous Power Plot
- Conclusion and Future Works



Introduction and Motivation

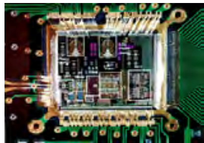
- ADCs are interfaced with digital circuits in mixed signal chips, where digital signal processing is performed.
- Supply voltage decreasing rapidly for digital circuits as technology scales.
- Analog to digital converters required to be operating with these devices at the same voltages.
- The proposed design meets both criteria: Low supply voltage (0.7*V*) and technology (45*nm*).

Specifications

- Resolution : 6 bits.
- Technology : 45*nm*.
- Speed : 1*Gs/sec*.
- V_{LSB} : 500μV.
- V_{DD} : 0.7*V*.
- INL : 0.46*LSB*.
- DNL : 0.70*LSB*.
- SNDR : 31.9*dB*.

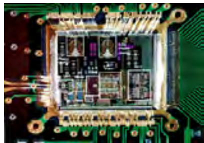
Related Research Works

Reference	Resolution (bits)	Technology (nm)	DNL (LSB)	INL (LSB)	SNDR (dB)	VDD (V)	Power (mW)	Samples/sec.
Choi 2001	6	350	<±0.3	<±0.3	32	3.3	545	1.3G
Donovan 2002	6	250	-----	-----	33	2.2	150	400M
Geelen 2001	6	350	<0.7	<0.7	5.6 (ENOB)	3.3	300	1.1G
Lee 2002	6	250	1.04	0.81	-----	2.5	59.91	1.11G
Mehr 1999	6	350	<0.32	<0.2	>5(ENOB)	3.3	225	500M
Sandner 2005	6	130	<0.4	<0.6	32.5	1.5	160	600M
Scholtens 2002	6	180	-----	0.42	5.7(ENOB)	1.95	328	1.6G

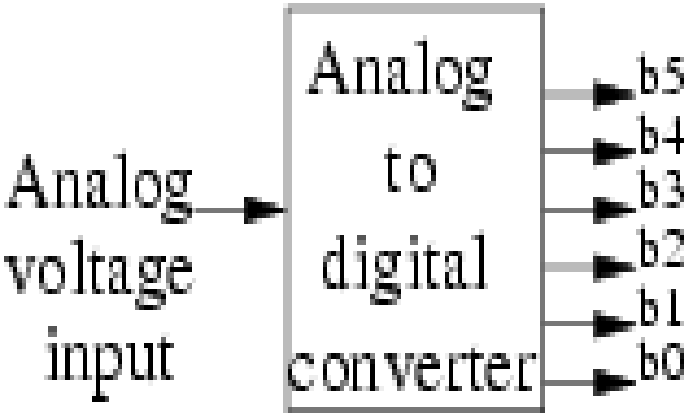


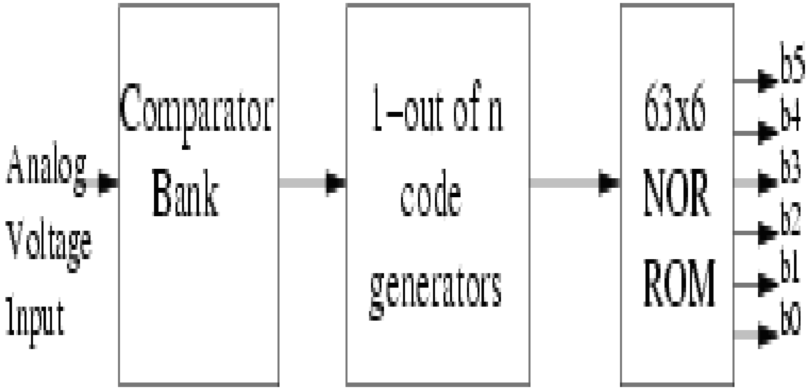
Related Research Works….

Reference	**Resolution (bits)**	**Technology (nm)**	**DNL (LSB)**	**INL (LSB)**	**SNDR (dB)**	**VDD (V)**	**Power (mW)**	**Samples/sec.**
Song 2000	6	350	-0.6	0.7	33.5	1	10	50M
Srinivas 2006	6	350	0.3	0.3	33.6	3.3	50	160M
Tseng 2004	6	250	<±0.1	<±0.4	32.7	2.5	35	300M
Uyttenhove 2000	6	350	-----	-----	32	3.3	-----	1G
Uyttenhove 2002	6	250	0.42	0.8	32	1.8	600	1.3G
Yoo 2001	6	250	-----	-----	-----	2.5	66.87	1G
This Design	**6**	**45**	**0.7**	**0.46**	**31.9**	**0.7**	**45.42µW**	**1G**



Design of flash ADC



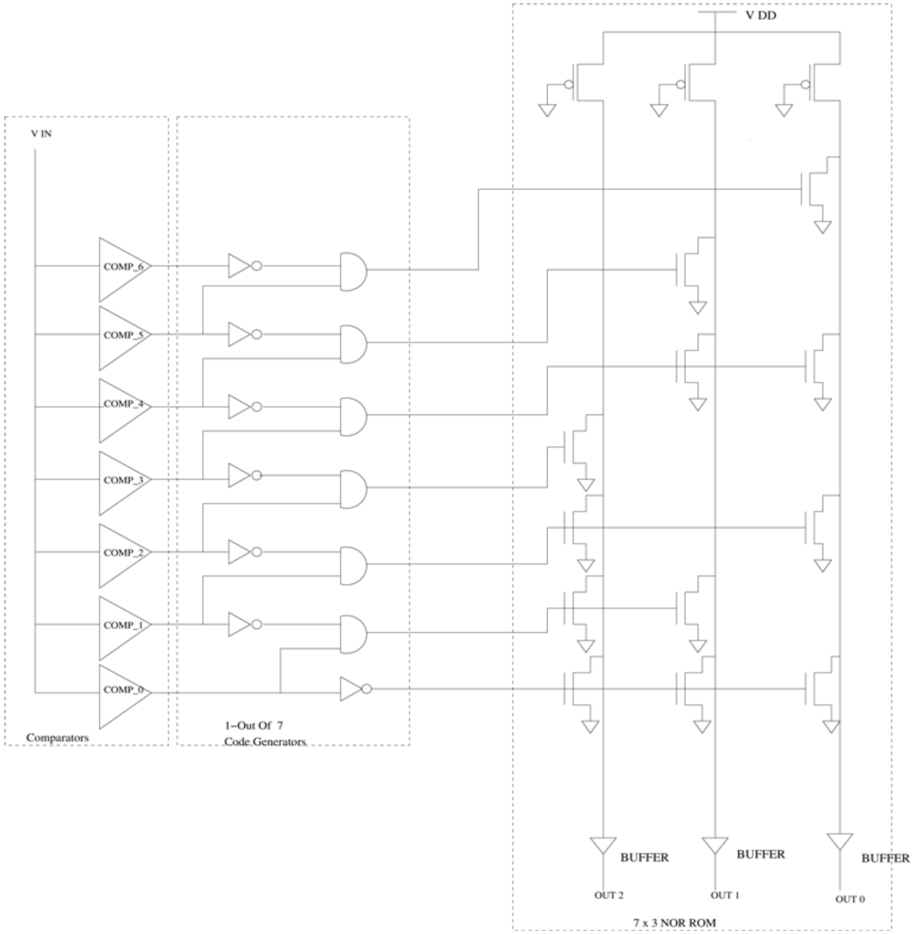


- High level block diagram of ADC.
- Input is analog (generally ramp or sine wave).

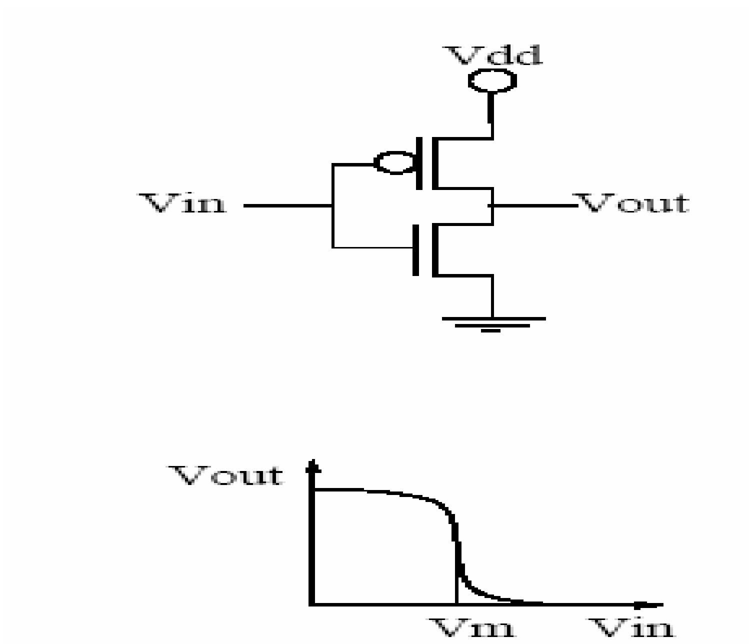
- Output of Comparator Bank is thermometer code.
- Converted to 1-out of n code using 1-out of n code generators.
- NOR ROM converts the 1-out of n code to binary code.

Design of flash ADC

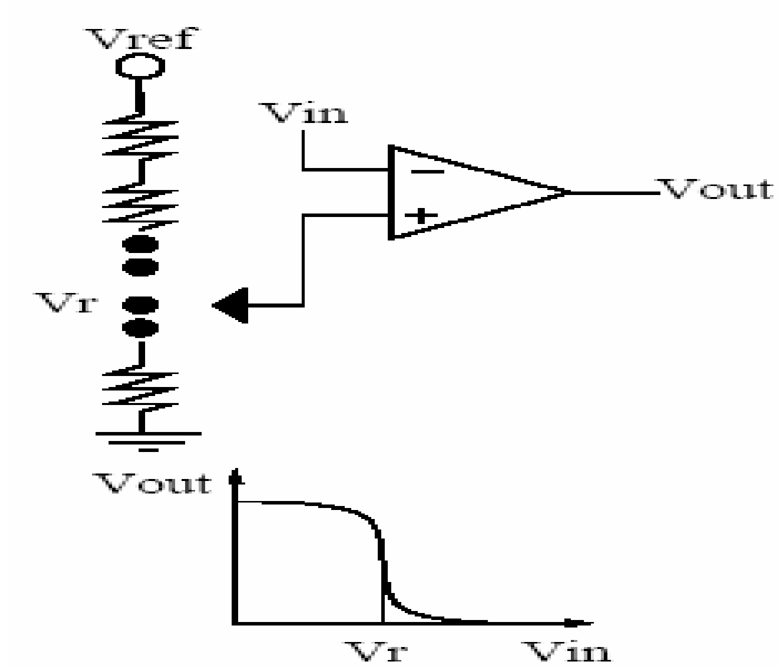
- For an n-bit ADC we need: 2^n-1 Comparators.
- 1-out of n code generators.
- NOR ROM : 2^n-1 X n.
- For discussion purposes,3-bit flash ADC is shown. 6-bit ADC has similar structure.



Threshold Inverter Quantization Principle

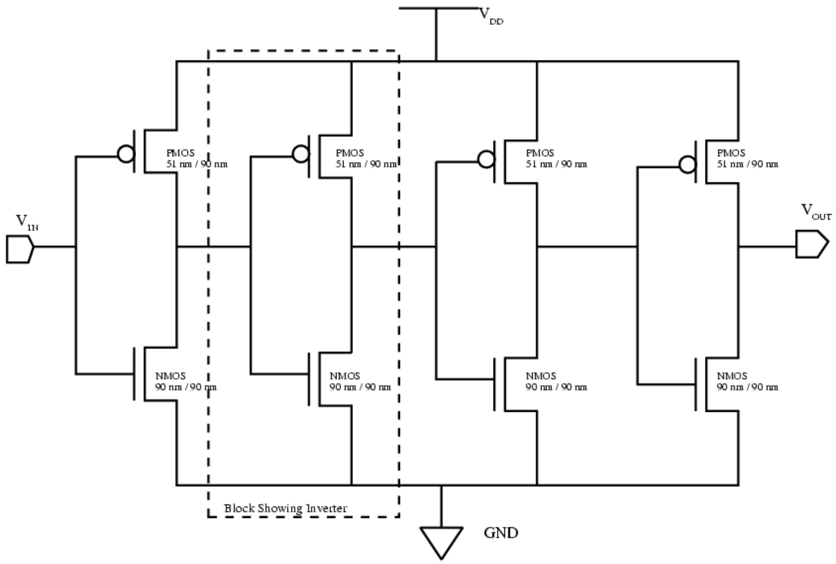


- TIQ comparator.
- Formed by cascading of digital inverters.
- Sizing of transistors determine switching point.



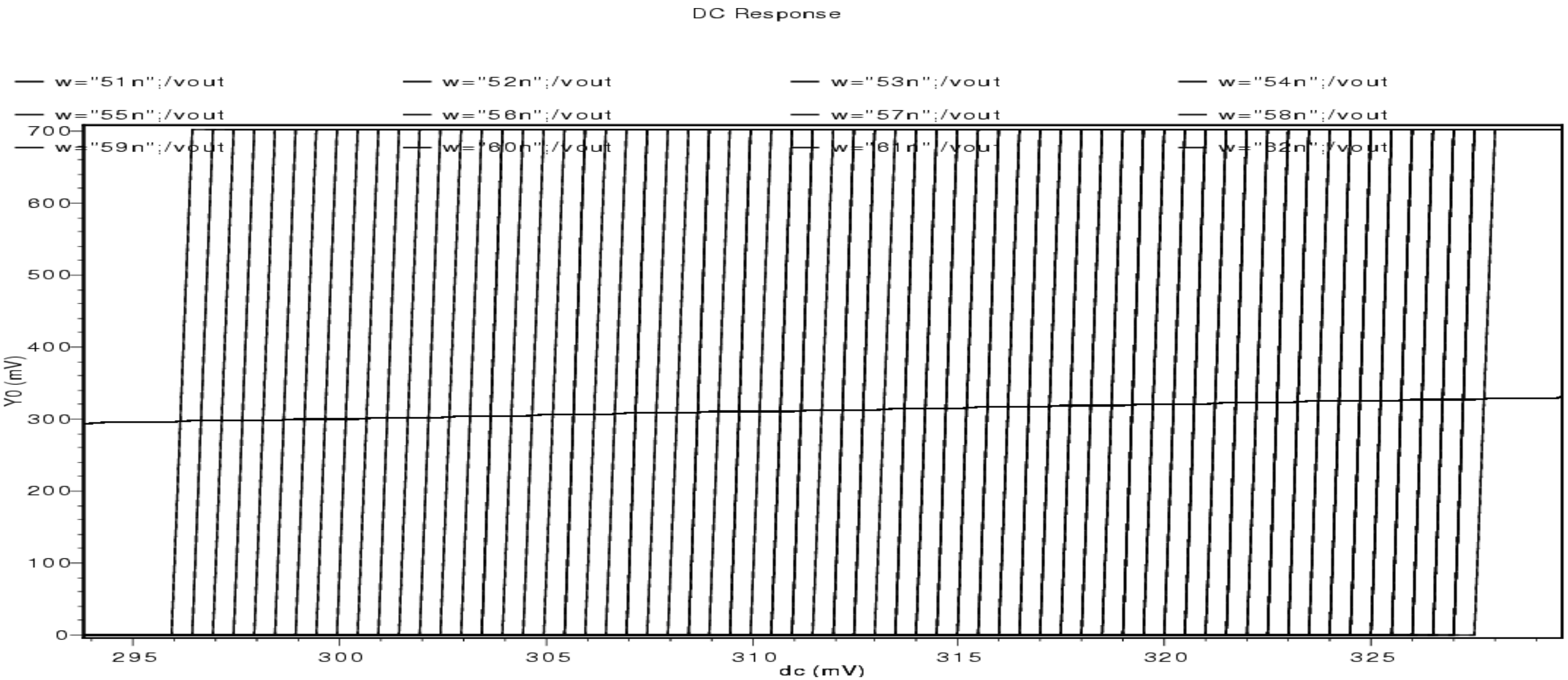
- Differential comparator.
- Require resistive ladder network.
- Area overhead increases.

TIQ Comparator



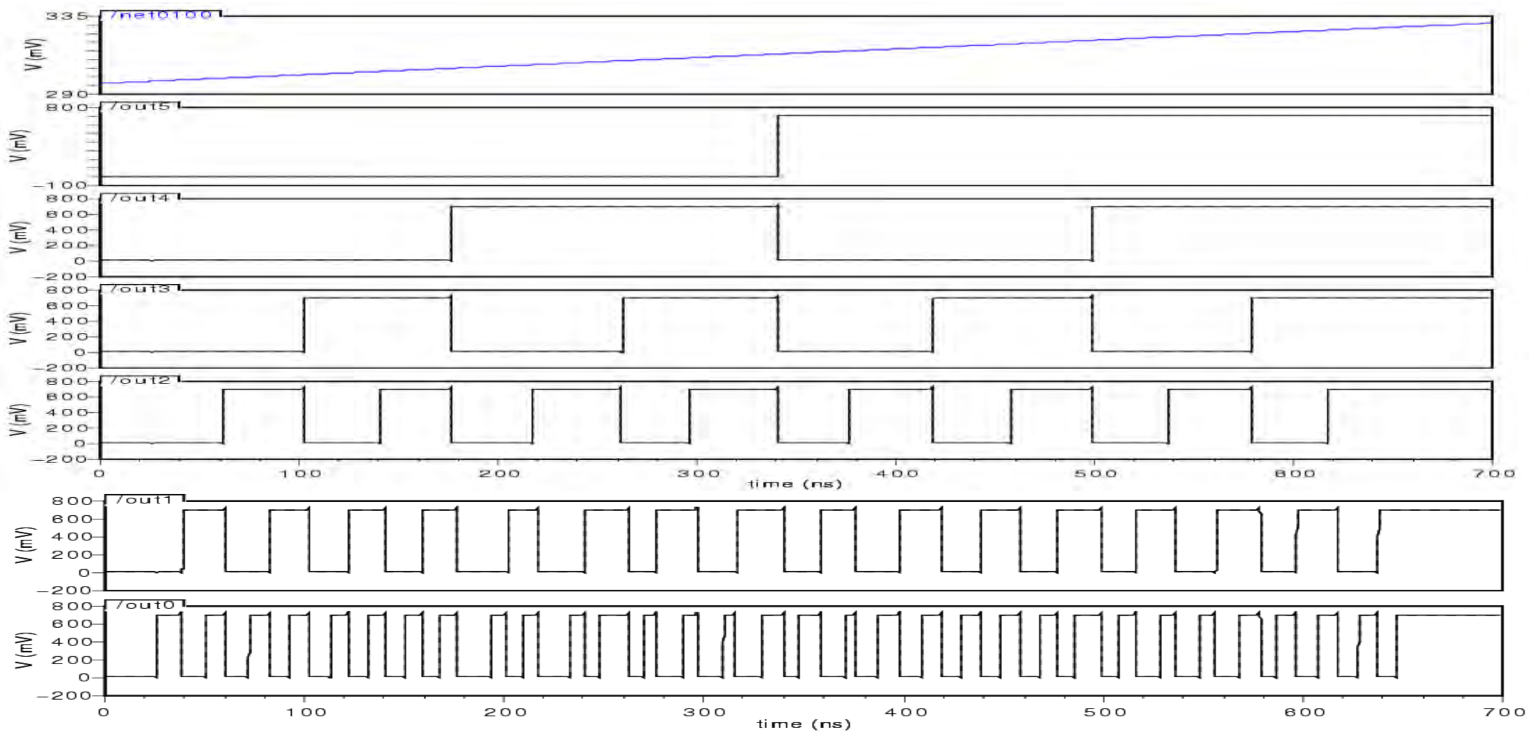
- Formed by four cascaded inverters.
- Provide a sharper switching for the comparator and full voltage swing.
- Sizes of PMOS and NMOS in a comparator are same, but different for different comparators.

Transistor sizing

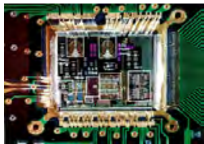


- ☐DC parametric sweep is used to determine the transistor sizes.
- ☐Input voltage varied from 0 to 0.7V in steps of 500μV.
- ☐W/L for NMOS transistors kept as 90nm/90nm. L for PMOS transistors kept as 90nm. W for PMOS transistors was given a parametric sweep in steps of 1nm. Minimum width=51nm,maximum width=163nm.

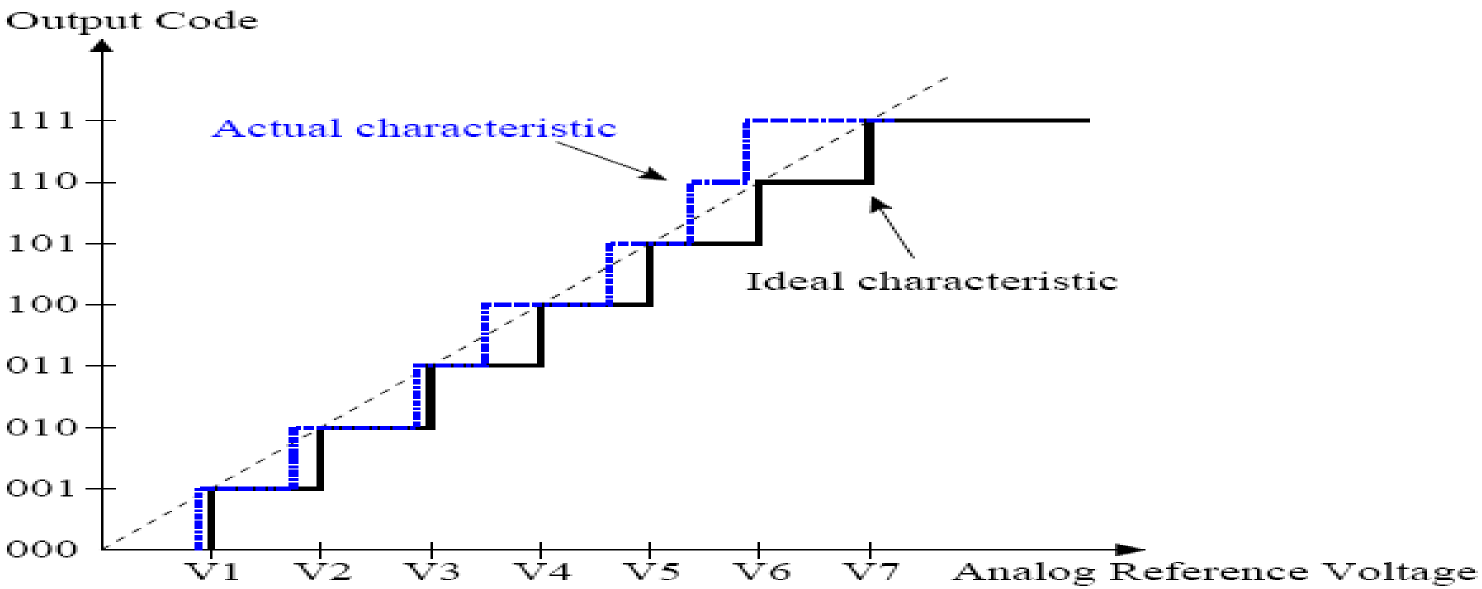
Functional Simulation



- Transient analysis carried out.
- Ramp generated from 296.3*mV* to 327.8*mV*. Digital codes going from 0 to 63 are obtained at the output.

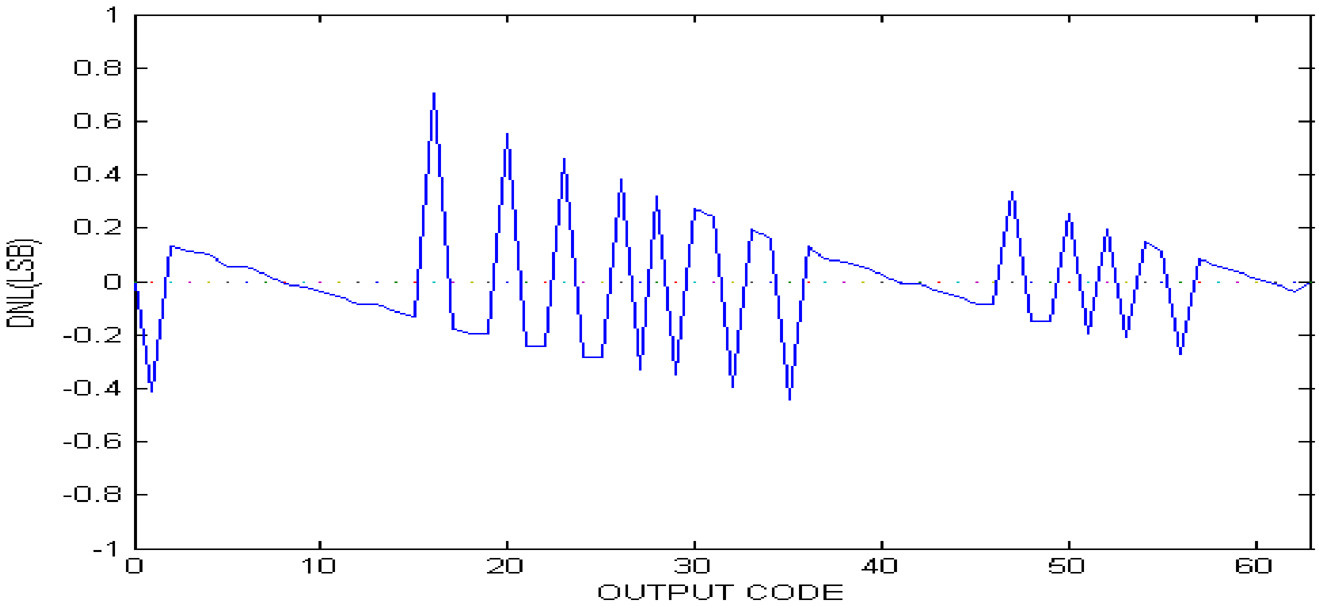


Ideal vs Actual Characteristics



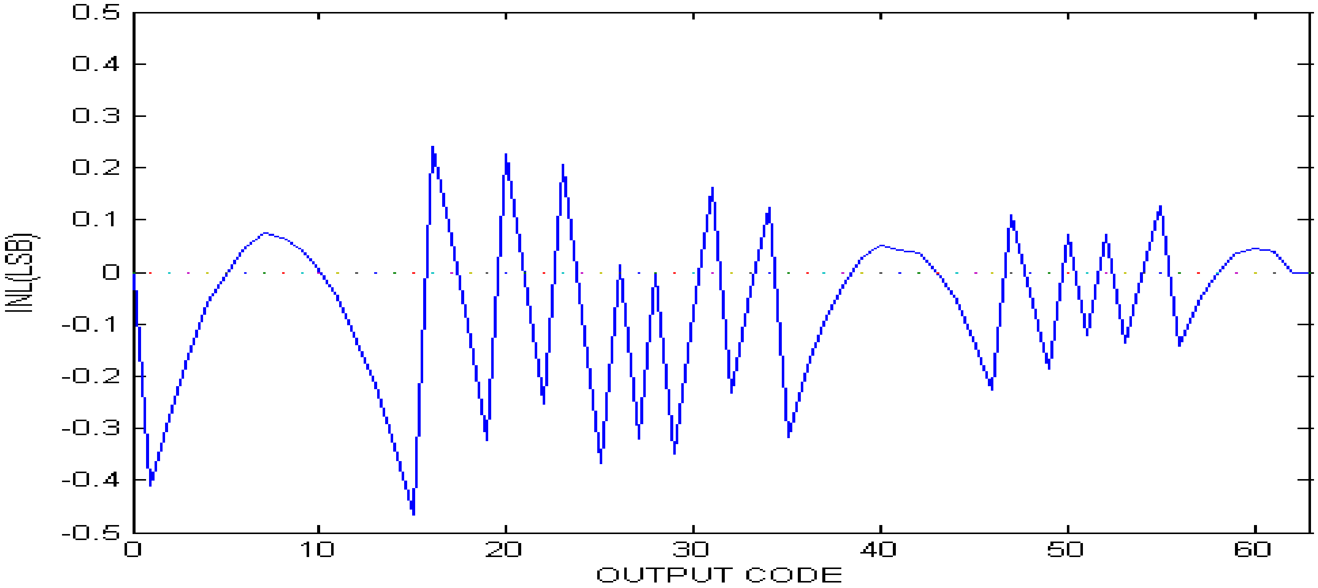
- Ideal vs actual transfer function
- Due to transistor implementation, actual transfer function never equal to ideal transfer function.
- Characterized using DNL and INL.

Max DNL of ADC = 0.7*LSB*



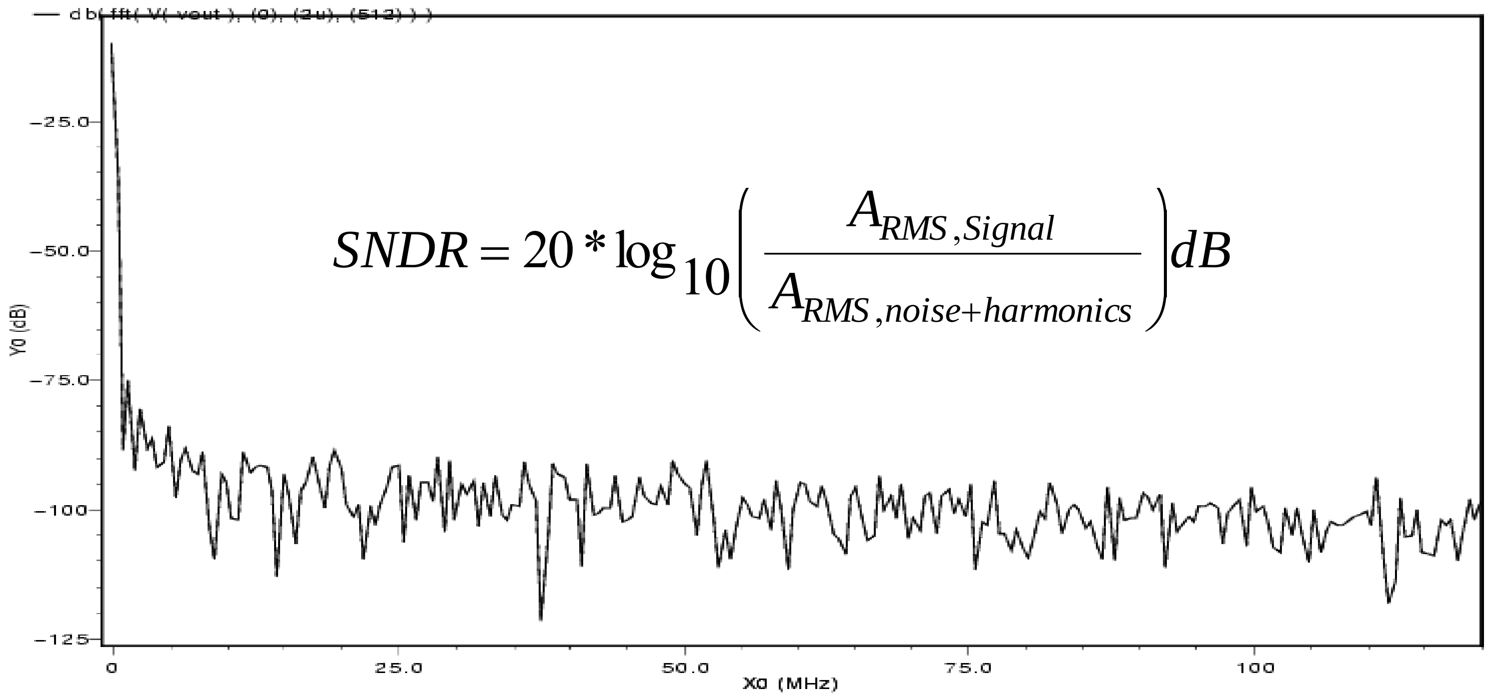
- Differential Non-Linearity. Difference between actual step width and ideal value of 1LSB.
- Modeled as Verilog-A block. Uses histogram method. DNL<1*LSB* ensures monotonicity.

Max INL of ADC =0.46*LSB*



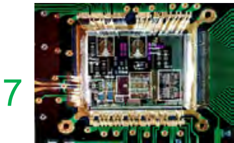
- Integral No-linearity. Deviation of actual transfer function from a straight line. expressed in *LSB*.
- Verilog-A block used. Slowly varying ramp given as input, covering full scale range in 4096 steps.

$\mathrm{SNDR} = 31.9dB$

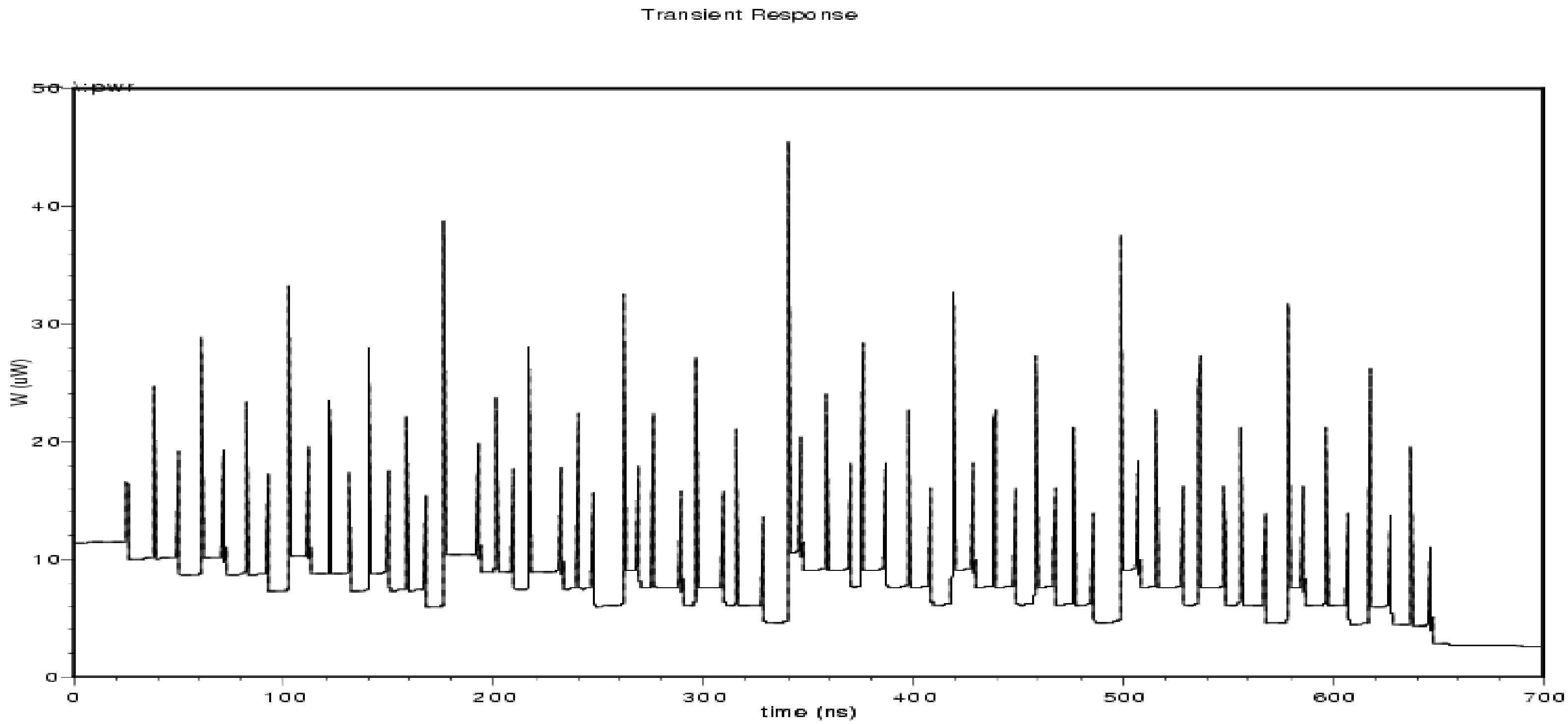


$$SNDR = 20 * \log_{10}\left(\frac{A_{RMS,Signal}}{A_{RMS,noise+harmonics}}\right) dB$$

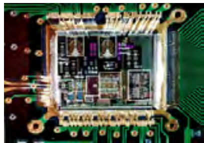
- Signal to noise and distortion ratio.
- ADC output fed to Ideal DAC. FFT of DAC output obtained. SNDR calculated from this.



Instantaneous Power Plot

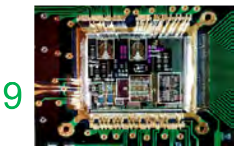


- Peak Power=45.42μW.
- Avg. Power=8.8μW.
- Low power design.

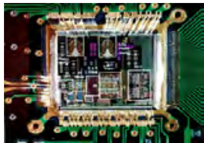


Conclusions

- Successful ADC design at nano-scale (45*nm*)technology.
- DNL=0.7*LSB*,INL=0.46*LSB*.
- SNDR=31.9*dB*, Low power design (Avg. Power = 8.8μW).
- Layout using 90*nm* general process design kit.
- Scaling the layout rules to perform layout at 45*nm*.

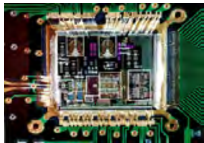


A Process and Supply Variation Tolerant Low Voltage, High Speed ADC



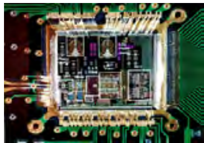
Outline of the Talk

- Introduction and Motivation
- Contributions, Design issues and Solutions
- Related Prior Research Works
- Transistor level design of the proposed ADC
- Physical design and Characterization of ADC
- Process and Supply variation Characterization
- Conclusion and Future Works



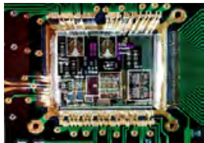
Introduction: Why Nano-CMOS ADC

- A large number of SoCs manufactured at the *90nm* process, *65nm, 45nm* closely following.
- Challenge is to meet performance of analog circuit with that of digital portion.
- Systems that once worked at *3.3/2.5V* need to work at *1.8V* without performance degradation.
- New circuit design techniques required to accommodate lower supply voltages.
- Analog/Mixed signal circuits should be designed using standard CMOS digital process.



Introduction: Nano-CMOS ADC

- ADC is a true mixed signal circuit used to bridge the gap between analog circuits and digital logic world.
- ADC circuit designs often contain matched transistors. In analog circuits, threshold voltage mismatch needs to be considered.
- For SoC capability, supply voltage variation should also be accounted.
- The demand for emerging application-specific, nanoscale mixed-signal SoCs which need process (threshold voltage mismatch) and power supply voltage variation tolerant ADC interfacing has motivated this research.



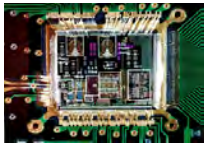
Design Issues and Solutions

- Logical and physical design of a **process** and **supply variation tolerant ADC** using **90nm** technology, suitable for SoC integration.
- Post-layout simulation results presented.
- Low supply voltage (V_{dd} = 1.2V), low power (Power α V_{dd}^2). Low V_{dd} puts constraint on the choice of 63 quantization levels (for 6-bit ADC in this paper). *LSB = 1mV* chosen for this design.
- *INL* degradation (*INL > 1LSB*) observed in the initial physical design, due to IR drop in the supply lines. *INL =0.344LSB,* by using large number of contacts and widening the supply lines.
- Power analysis with *100fF* reveals ADC consumes minimal power.

Related Prior Research Works

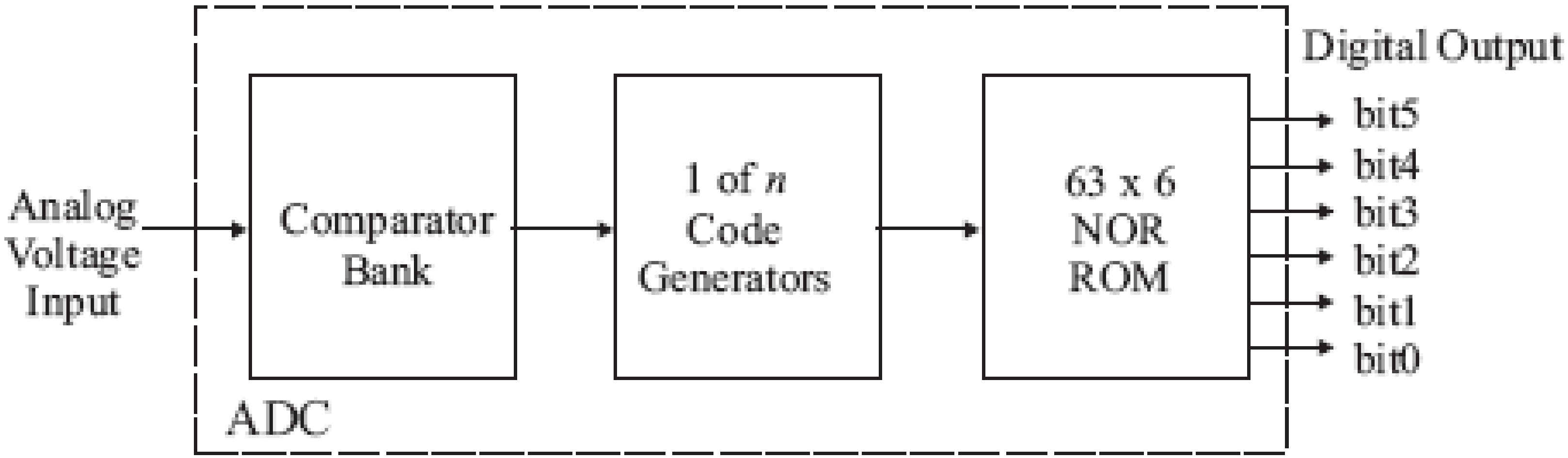
Works	Tech. (nm)	DNL (LSB)	INL (LSB)	V_{dd} (V)	Power *(mW)*	Rate (GS/s)
Geelen[9]	350	< 0.7	< 0.7	3.3	300	1.1
Uytttenhove [19]	350	---	---	3.3	---	1
Donovan [6]	250	---	---	2.2	150	0.4
Tseng [8]	250	< 0.1	< 0.4	2.5	35	0.3
Yoo [11]	250	---	---	2.5	66.87	1
Scholtens [16]	180	---	0.42	1.95	328	1.6
Sandner [7]	130	< 0.4	< 0.6	1.5	160	0.6
This Work	**90**	**0.459**	**0.344**	**1.2**	**3.875**	**1**

- ☐ Low Technology, low voltage, low power, high speed design with satisfactory *DNL*, *INL* performance.



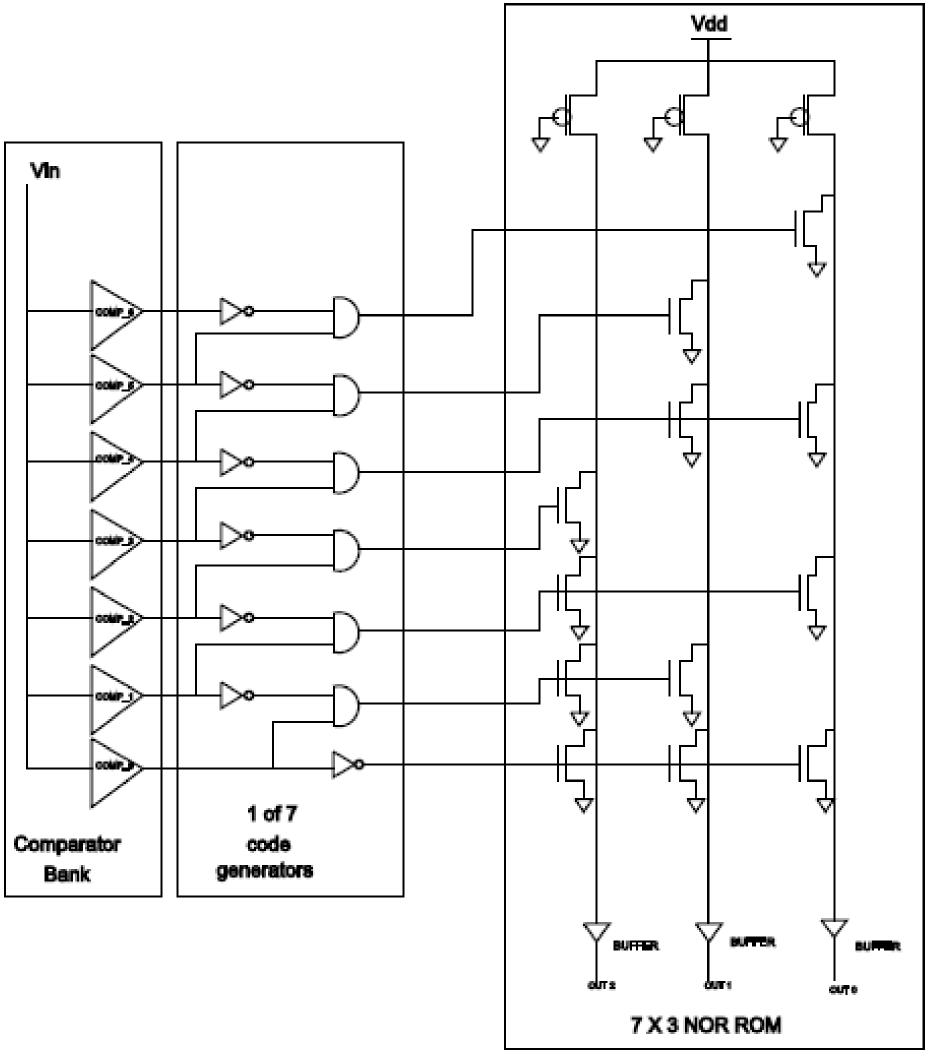
Transistor Level Design of the Proposed ADC

ADC: Block Diagram



- Output of Comparator Bank is thermometer code.
- Converted to 1-of n code using 1-of n code generators.
- NOR ROM converts the 1-of n code to binary code.

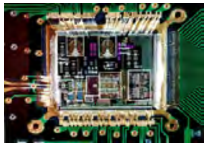
ADC : Circuit Diagram



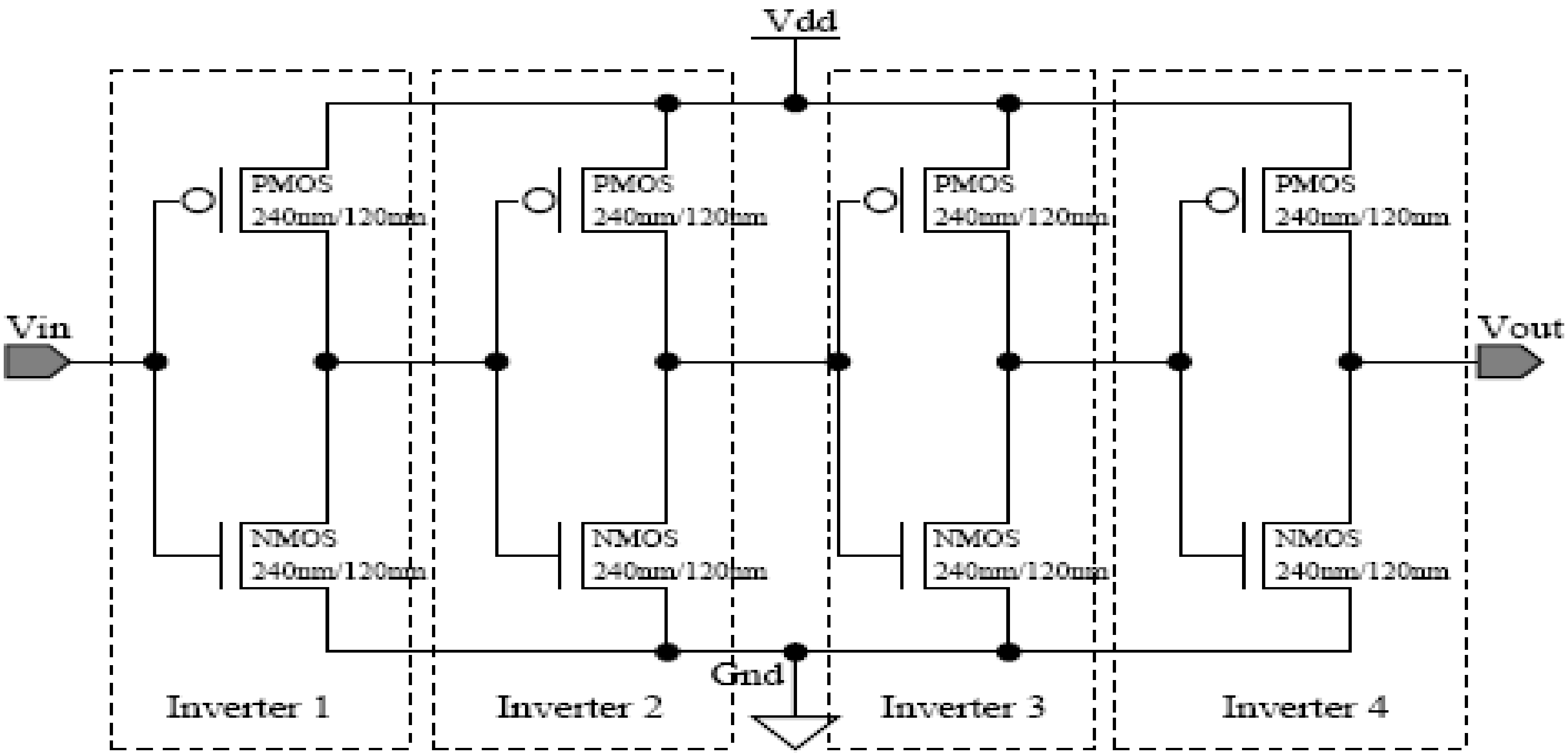
Comparator Design : Technique

- Comparator designed using Threshold Inverting (TI) technique.
- Advantages of TI technique:

1. High speed.
2. Simplicity.
3. Eliminates the need for inherently complex high-gain differential input voltage comparators and additional resistor ladder circuit.



Comparator Design : Circuit



- $V_{switching}$ set internally based on transistor sizes.
- Inverter 1 and 2 form the baseline comparator, while Inverter 3 and 4 provide increased gain and sharper switching.

Comparator Design : Equations

For short channel transistors:

$$V_{switching} = V_{dd}\left(\frac{R_n}{R_n + R_p}\right),$$

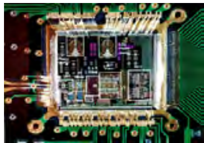
R_n = NMOS effective switching resistance.
R_p = PMOS effective switching resistance.

$$InputVoltageRange = V_{dd} - \left(V_{tn} + \left|V_{tp}\right|\right),$$

V_{dd} = supply voltage.
V_{tn} = NMOS threshold voltage.
V_{tp} = PMOS threshold voltage.
Values chosen *493mV* to *557mV*.

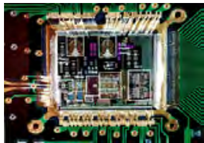
$$V_{LSB} = \left(\frac{InputVoltageRange}{2^n}\right),$$

For our design,
V_{LSB} = *1mV*.



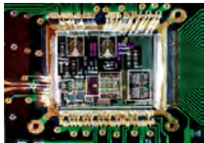
1 of n code generator Design

- Converts thermometer code into 1 of n code.
- Consists of AND gates as combination of an inverter followed by a NAND gate.
- Output from each of the AND gates is fed to the input of the NOR ROM.
- One of the two inputs to the AND gate is fed from the TI comparator output.
- The other input to the AND gate is the inverted output from the next level comparator.

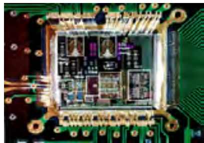


NOR ROM Design

- Converts 1-of-n code to binary code.
- Consists of PMOS (*135nm/180nm*) pull-up and NMOS (*180nm/180nm*) pull-down devices.
- 63 word lines , 6 bit lines, 63 x 6 NOR ROM designed.
- *Wp* < *Wn,* to ensure PMOS is narrow enough for NMOS to pull down output safely.
- Buffers, consisting of two cascaded inverters (PMOS: *480nm/120nm*, NMOS: *240nm/120nm*) are applied at the outputs to obtain symmetrical waveforms, with equalized rise and fall times.

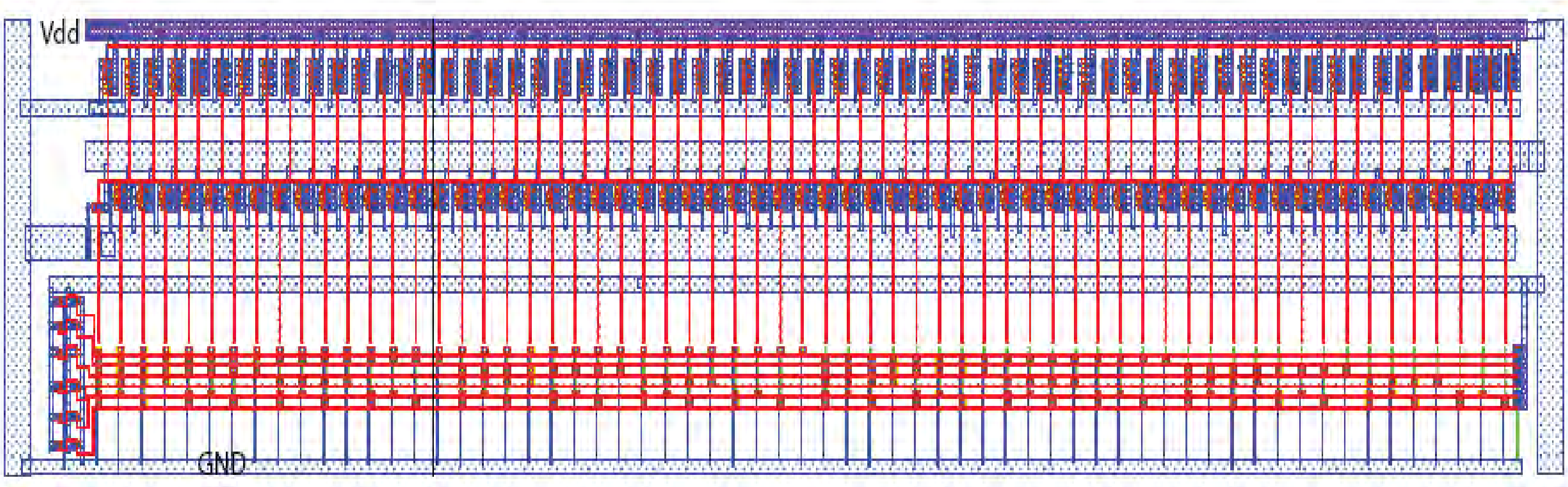


Physical Design and Characterization of ADC



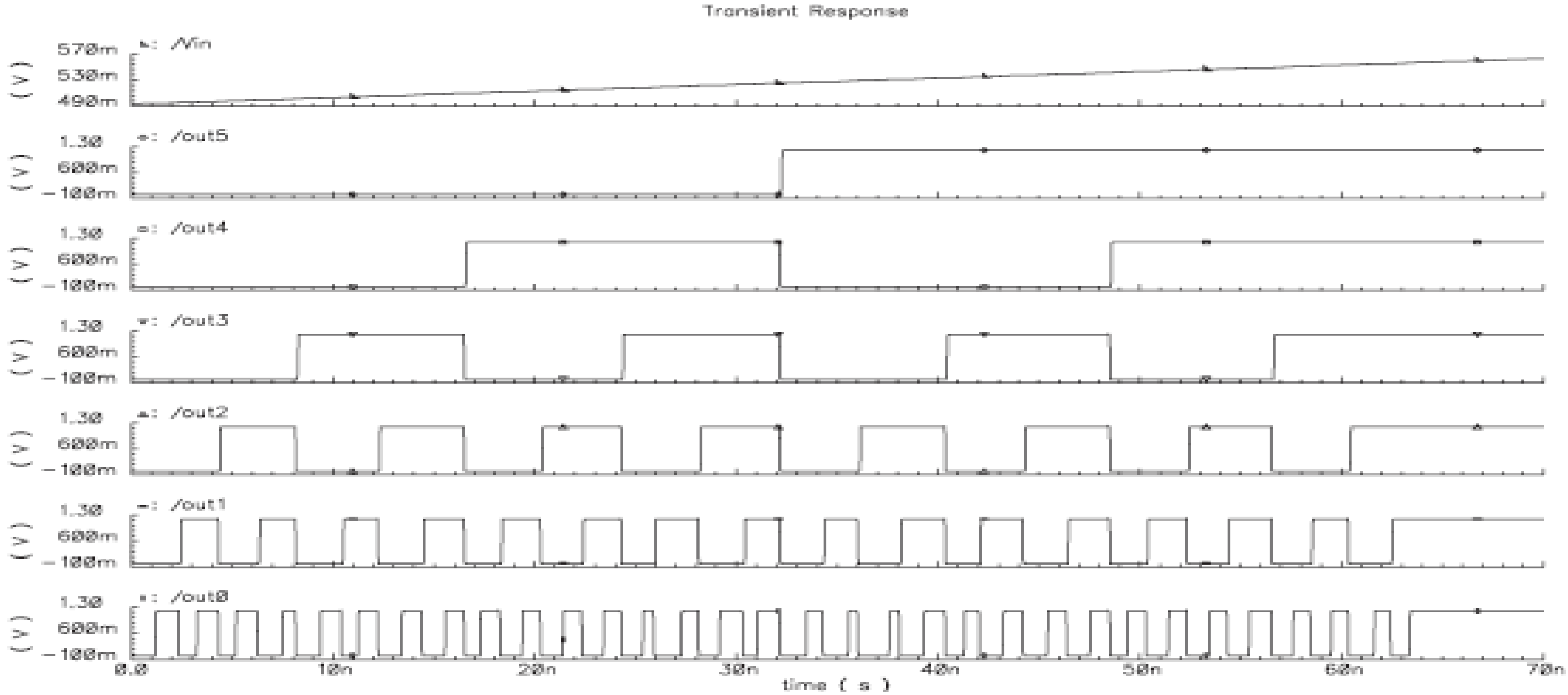
ADC: Physical Design

- Physical design of the ADC carried out using 90nm Salicide "1.2V/2.5V 1 Poly 9 Metal" digital CMOS pdk, demonstrating SoC readiness.
- To ensure minimal IR drop, power and ground routing comprises of wide vertical bars and generous use of contacts has been made.



Post Layout Functional Simulation

- Transient analysis is carried out, where a linearly varying ramp covering full scale range of ADC, is given as input.
- Output digital codes from 0 to 63 obtained correctly, with no missing codes. Maximum sampling speed - 1GS/s.



Characterization: Equations

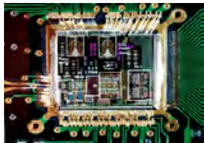
- ADC characterized for static performance.
- Nominal characterization: Histogram test used to determine *INL* (Integral Non-Linearity), *DNL* (Differential Non-Linearity).
- Equations for *INL, DNL*:

$$INL[i] = width[i] + INL[i-1] - 1$$

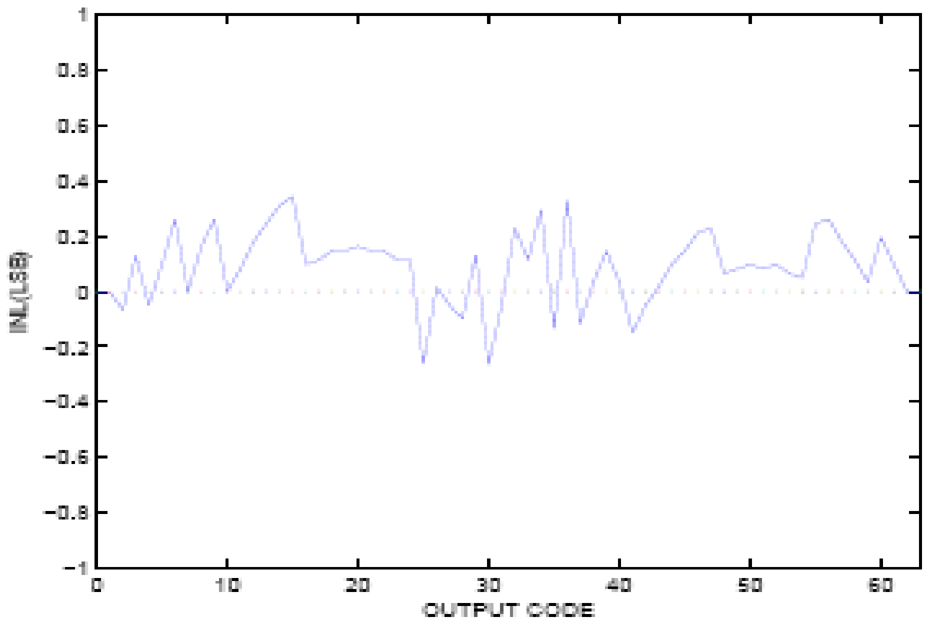
$$DNL[i] = width[i] - 1$$

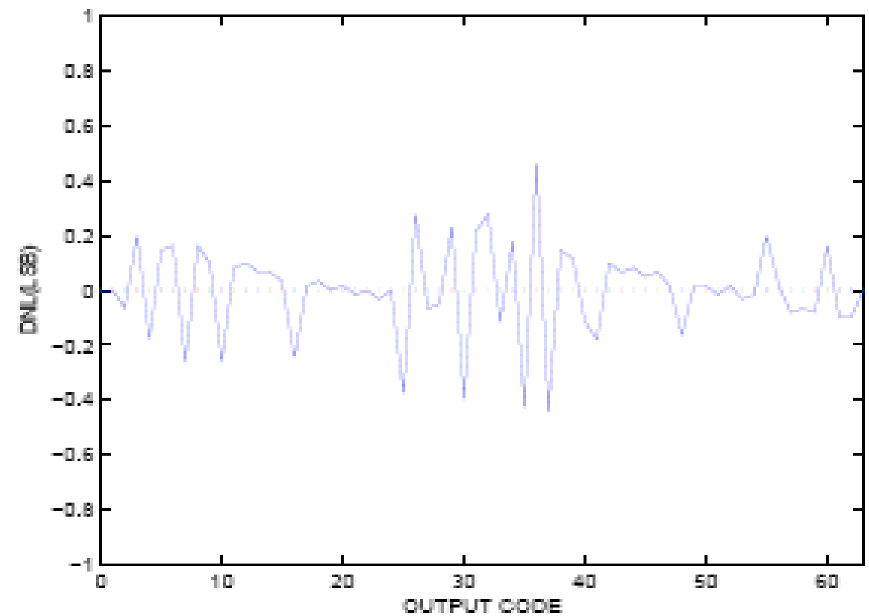
$$width[i] = \frac{1 * bucket[i]}{hits * (NUM_{CODES} - 2)}$$

- where ***bucket*** holds the number of code hits for each code.
- ***width*** holds the code width calculations.
- Total hits between codes 1 and 62 is denoted as ***hits***.
- $\boldsymbol{NUM_{CODES}}$ is the number of codes, 64 for a 6-bit ADC.



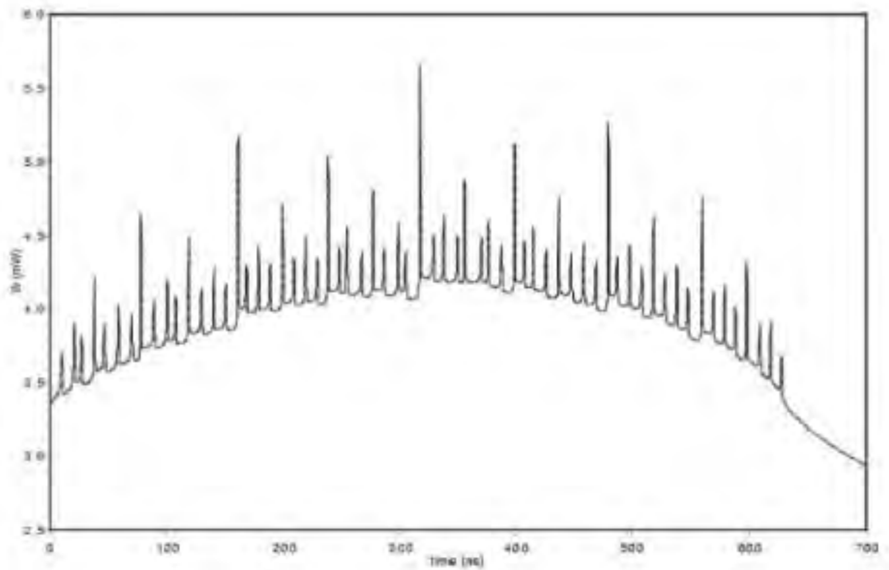
Characterization: *INL and DNL* Plots





- Maximum *INL=0.344LSB.*
- Maximum *DNL=0.459LSB.*

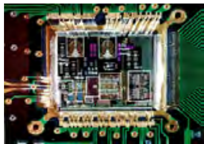
Power Analysis



Instantaneous Power Plot.

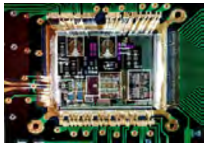
- Power analysis of the ADC performed with a capacitive load of *100fF.*
- Peak Power = *5.794mW.*
- Average Power = *3.875mW.*

ADC Components	**Average Power *(mW)***
Comparator Bank	**3.68125 (95%)**
1 of n code Generators	**0.03875 (1%)**
NOR ROM	**0.155 (4%)**
Total	**3.875**

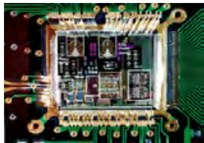


ADC Performance

Parameter	**Value**
Technology	*90nm* CMOS 1P 9M
Resolution	6 bit
Supply voltage (V_{dd})	*1.2V*
Sampling Rate	*1GS/s*
INL	*0.344LSB*
DNL	*0.459LSB*
Peak Power	*5.794mW@1.2V*
Average Power	*3.875mW@1.2V*
Input Voltage Range	*493mV to 557mV*
V_{LSB}	*1mV*



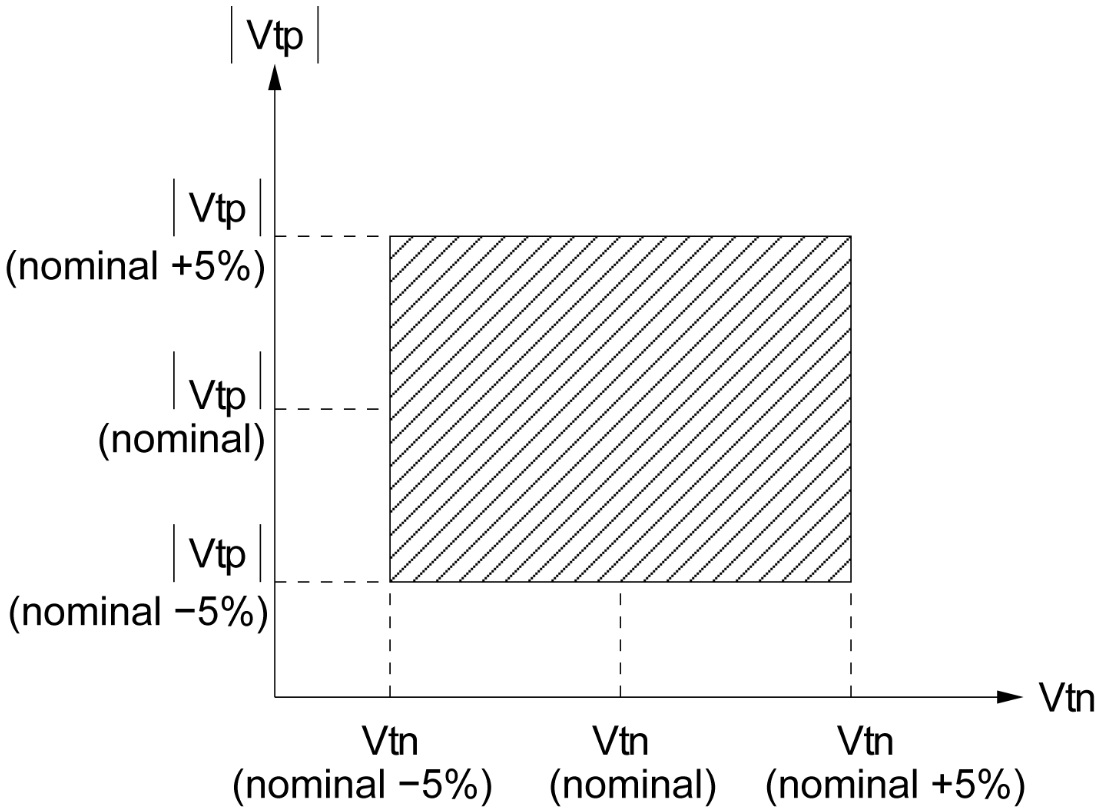
Process and Supply variation Characterization



Process Variation

- Corner-based methodology is used.
- NMOS threshold voltage (V_{tn}) and PMOS threshold voltage (V_{tp}) varied by ±5% from nominal value in the pdk.
- Shift in *INL*, *DNL*, input voltage range recorded.
- *INL* shows maximum variation of *10.5%.*
- *DNL* shows maximum variation of *5.7%.*

Process Variation: Corner Method



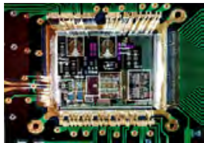
Process Variation: *INL* and *DNL*

Vtp, Vtn	**Input Range *(mV)***	V_{LSB} ***(mV)***	**INL *(LSB)***	**DNL *(LSB)***
nominal	*493-557*	*1*	*0.344*	*0.459*
+5%, +5%	*495-557*	*0.96875*	*0.333*	*0.46*
-5%, -5%	*491-556*	*1.015625*	*0.345*	*0.477*
-5%, +5%	*500-564*	*1*	*0.36*	*0.485*
+5%, -5%	*501-566*	*1.015625*	*0.38*	*0.479*

Supply Variation : *INL* and *DNL*

- Nominal supply voltage *(1.2V)* varied by ±10%.
- *INL*, *DNL*, and input voltage range values are recorded.
- *INL* shows maximum variation of *4%.*
- *DNL* shows maximum variation of *4.8%.*

Vdd(V)	**Input Range *(mV)***	**V_{LSB} *(mV)***	**INL *(LSB)***	**DNL *(LSB)***
1.08V (-10%)	*448-500*	*0.8125*	*0.359*	*0.467*
1.2V (nominal)	*493-557*	*1*	*0.344*	*0.459*
1.32V (+10%)	*537-614*	*1.203*	*0.339*	*0.481*



Conclusion and Future Works

- Design of a process and supply variation aware low voltage, high speed flash ADC presented.
- Comparators designed using threshold inverting (TI) technique.
- ADC subjected to ±10% supply variation, ±5% threshold voltage mismatch.
- Nominal *INL=0.344LSB,* maximum variation of *10.5%.*
- Nominal *DNL=0.459LSB,* maximum variation of *5.7%.*
- It is demonstrated that the design of low voltage, high speed and SoC ready ADCs is possible at *90nm* technology and below.
- We plan to carry out the complete design cycle for this ADC at *45nm*.
- Alternative encoder architectures will be explored to achieve higher sampling speeds.