

# Failure Analysis for Ultra Low Power Nano-CMOS SRAM Under Process Variations

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**Abstract**—Several design metrics have been used in the past to evaluate the SRAM cell stability. However, most of them fail to provide the exact stability figures as shown in this paper. Therefore, we investigate new stability metrics and report the stability analysis for typical a SRAM cell. In particular, a concept called power metric is introduced. From this metric we derive two new stability figures; static power noise margin (*SPNM*) and write trip power (*WTP*). It is shown that these new figures provide better cell stability analysis. Furthermore, we have exhaustively analyzed the impact of different parameters variations such as cell ratio, supply voltage  $V_{dd}$  and threshold voltage  $V_{th}$  on *SPNM* and *WTP*. Statistical models for estimating *SPNM* and *WTP* from intra-die  $V_{th}$  variations are presented. The estimated results match well with the Monte Carlo (MC) simulations.

## I. INTRODUCTION

Increasing trends of subthreshold digital circuit design as a low power solution, require integration of SRAM that should be compatible with subthreshold combinational logic. But, sensitivity of the process variations such as intra-die variations in  $V_{th}$  due to random dopant fluctuations [3] increases with subthreshold operation of SRAM. Further stability constraints arise due to line edge roughness and poly gate grain size variations [2], [5]. Thus, the SRAM cell stability will be a major hurdle for future VLSI design due to process variations. A stable read and write operations of a SRAM cell represent significant limitations. To quantify these limitations, static noise margin (*SNM*) voltage obtained from the butterfly curve as shown in Fig. 1(b) has been widely used as a metric for SRAM cell stability quantification [8]. However, major drawbacks of *SNM* metric, as would be evident from Section II, are the followings: (a) the ideal voltage transfer characteristic (VTC) obtained from the butterfly curve delimits to a maximum  $0.5V_{dd}$ , (b) inability to measure it with a automatic inline tester, (c) inability to generate statistical information of SRAM failures, and (d) it does not provide *current flow* information which is equally important for stability analysis. An alternative approach for stability analysis that satisfies the above requirements is the use of N-curve of a SRAM [10].

The *contribution of this paper* is exploration of the N-curve based power metrics, such as *SPNM* and *WTP*. Our technique fundamentally differs from previous works in the following facts: previous works consider either *SNM* or the N-curve for analysis, whereas here we have taken both the figures into account. In other words, in power metrics both the voltage and current information are taken into account so these can provide better stability analysis of an SRAM cell. Furthermore, statistical models for estimating the *SPNM* and *WTP* are given for process variations in  $V_{th}$ , which can be extended for variations in any process and design parameters. We have also analyzed the dependencies on cell ratio and  $V_{dd}$  for power metrics and compared with the *SNM* that could be useful for optimization of size and power of an SRAM cell.

Rest of the paper is organized as follows. The limitations of the

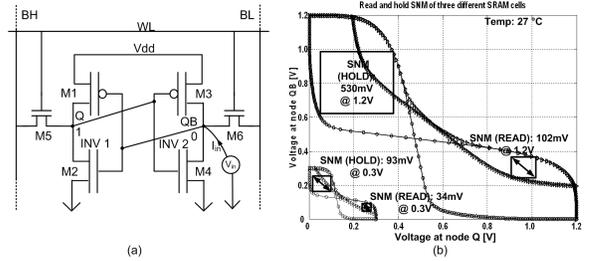


Fig. 1. (a) 6T-SRAM cell structure and (b) read SNM plots.

existing stability metrics based on *SNM* is presented in Section II. In Section III, N-curve based metrics and derived power metrics *SPNM* and *WTP* are presented. The subthreshold *SPNM* and *WTP* dependencies for cell ratio,  $V_{dd}$  and intra-die variations in  $V_{th}$  are presented in Section IV. The SPICE simulation results are presented in Section V. Section VI, concludes the paper.

## II. LIMITATIONS OF SNM METRIC

The stability of SRAM cell is commonly defined by the *SNM* as a maximum value of DC noise voltage that can be tolerated without changing the internal storage node state [1], [6], [9]. A successful data retention during hold and functional operations read and write are determined by hold *SNM*, read *SNM* and write trip voltage respectively. These three metrics are widely used for design and performance analysis of SRAM cell but none of the metrics carry the *current flow* information which is having extensive importance. For example, in hold state the hold *SNM* is highly dependent on the driving capability of the pull down NMOS transistors, whereas read *SNM* is strongly dependent on the driving capability of the NMOS access and pull down transistors.

To illustrate this strong dependence between voltage and current in SRAM cell, we simulated three different SRAM cell designs with different transistor sizes. It is observed that there is no change in hold and read *SNM* for different designs. Fig. 1(b) shows the results obtained from three different SRAM cell designs for both hold and read state at  $V_{dd} = 1.2V$  and  $V_{dd} = 0.3V$  represent the identical *SNM*, but it does not mean that they are equally stable. This confirms that the *SNM* fails to provide exact stability figure and it is hard to decide which design is stable based on this information. If we incorporate the *current* information along with the voltage based metrics *SNM*, than it provides better stability figure and is easy to predict which design has better stability. Fig. 2 shows the N-curve at  $V_{dd} = 1.2V$  for three different SRAM cell designs obtained from experimental setup shown in Fig. 1(a). Thus, it is evident from the Fig. 1(b) and Fig. 2 that a wrong conclusion can be drawn based on the read and hold *SNM* of the SRAM cell. From the N-curves we can conclude that the design having

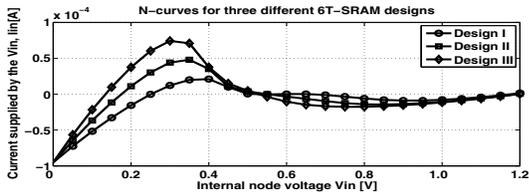


Fig. 2. Read N-Curve plots for three different designs of a 6T-SRAM cell at  $V_{dd} = 1.2V$ .

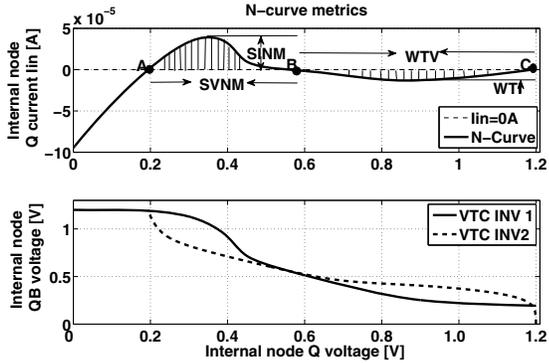


Fig. 3. Read access N-curve of a standard 6T-SRAM cell and corresponding butterfly curve.

higher current should be more stable even when the  $SNM$  voltages are equal. Thus,  $SNM$  does not provide better stability figure for analysis of SRAM design.

### III. N-CURVE METRICS

The experimental setup of a standard 6T-SRAM cell used for extracting the N-curve is shown in Fig. 1(a). At the beginning of read access both bitlines (BL and BH) are precharged to ‘1’ and wordline is activated to ‘1’. Without loss of generality, we assume that the internal storage nodes Q and QB at ‘1’ and ‘0’ respectively. A voltage sweep  $V_{in}$  from 0 to  $V_{dd}$  is applied at the node QB and corresponding current  $I_{in}$  is measured, resulting relationship between  $V_{in}$  and  $I_{in}$  is called the N-curve as shown in Fig. 3. The N-curve has three intersection points, A, B, and C; point A and C correspond to stable state points while point B is a meta-stable point. At these points current supplied by the sweep voltage source  $V_{in}$  is zero. At the beginning, when both  $V_{in}$  and node QB at 0V, the access transistor M6 and transistor M4 are in saturation and linear region respectively. Therefore, drain current of M5 is larger than the drain current of M4. Thus, the difference of these currents,  $I_{in}$  flows into the sweep voltage source in order to maintain node QB at 0V. When the difference of these currents is equal to 0 A (i.e.  $I_{in} = 0$  A), which is corresponding to point A, a further increase in sweep voltage  $V_{in}$ , increases  $I_{in}$  as indicated by the change in sign and devices operation region remain unchanged up to point B. As the operation region of M4 moves from linear to saturation region, M3 is now active and working regions of all the devices M6, M4 and M3 moved to saturation region. At point C, both M6 and M3 are in linear region while M4 moves from active to cut-off region.

#### A. Voltage and Current Metrics

The stability metrics derived from the N-curve are based on the combined voltage and current information for an SRAM cell. Fig. 3 shows static voltage noise margin ( $SVNM$ ), static current noise margin ( $SINM$ ), write trip voltage ( $WTV$ ), and write trip current

( $WTI$ ). The  $SVNM$  is defined as a maximum tolerable DC noise voltage at internal nodes of the cell before its content flips and it is measured as a voltage difference between point B and A. Similarly,  $SINM$  can be defined as a maximum tolerable DC noise current injected at internal nodes of the cell before its content changes and it is measured as a peak current located between point A and B. These two metrics  $SVNM$  and  $SINM$  are used to characterize the cell read stability. However, cell’s write stability can be characterized with the help of  $WTV$  and  $WTI$ . For this purpose N-curve has to be analyzed from right to left because for write operation, pulling down of precharged bit line (BH) to ground so that the internal node Q get discharges. The  $WTV$  is the minimum voltage drop needed to change the internal nodes of the cell, which can be measured as a difference between point C and B. The  $WTI$  is defined as a minimum amount of the current needed to write the cell which can be measured as a negative current peak between point C and B as shown in Fig. 3. An overlap of points A and B or point B and C means loss of stability of SRAM cell.

#### B. Derived Power Metrics

The N-curve as shown in Fig. 3 is used to derive the power metrics which includes both the voltage and current information for read stability or write ability. So, instead of using four metrics obtained from N-curve to analyze the stability of an SRAM cell, we can combine them in two power metrics,  $SPNM$  and  $WTP$ . The  $SPNM$  is used to characterize the read stability which is defined as the area below the curve between point A and B. As the shaded part of N-curve between point A and B has formally a unit of power which is given by Eq. 1,

$$SPNM = \frac{1}{B - A} \sum_{n=A}^{n=B} I_{in}(n) * V_{in}(n). \quad (1)$$

The  $WTP$ , characterizes the write ability of a cell and which is defined as the area above the curve between point B and C which is given by Eq. 2:

$$WTP = \frac{1}{C - B} \sum_{n=B}^{n=C} I_{in}(n) * V_{in}(n), \quad (2)$$

where  $V_{in}$  is the sweep voltage source and  $I_{in}$  is the current supplied by the  $V_{in}$ . The successful write in the cell is quantified with the help of this metric. From Fig. 3 it is clear that for a successful read and write operation  $SPNM$  should be positive (i.e.,  $SPNM > 0$ ) and  $WTP$  should be negative (i.e.  $WTP < 0$ ).

### IV. DEPENDENCIES OF SPNM AND WTP

The stability of the cell degrades with lowering supply voltage  $V_{dd}$ , minimum cell size and process variability which will limit advanced technology node to operate at lower voltage due to degraded read  $SNM$  and reduced write margin. Read  $SNM$  degradation results in destructive read operation whereas reduced write margin cause unsuccessful write operation. The SPICE simulation results presented in this section for a standard 6T SRAM cell are based on the predictive technology model (PTM) 65nm node.

#### A. Dependence on the Cell Ratio

The stability as well as the size of the SRAM cell is primarily determined by the cell ratio, which is defined as the ratio of pull down transistor’s ( $W/L$ ) to the access transistor’s ( $W/L$ ). Fig. 4 shows the impact of cell ratio on  $SPNM$  and  $WTP$  at  $V_{dd} = 1.2V$  during hold, read and write operations. As shown in Fig. 4, the  $SPNM$  is almost linearly increases with the cell

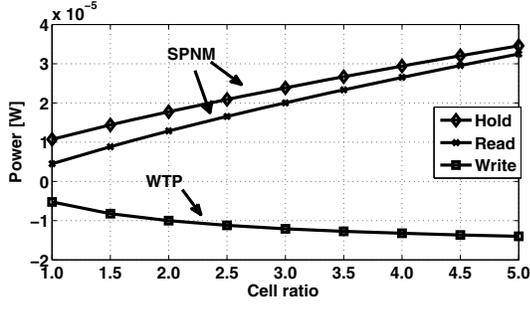


Fig. 4. Cell ratio dependency of SPNM and WTP at  $V_{dd} = 1.2V$ .

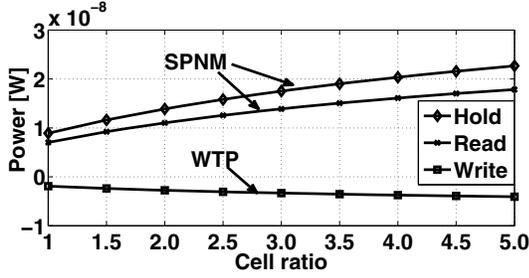


Fig. 5. Cell ratio dependency of SPNM and WTP at  $V_{dd} = 0.3V$ .

ratio. The linear dependence of  $SPNM$  on cell ratio is because of the drain current of the pull down transistors and access transistors increases linearly with the cell ratio. Fig. 5 shows that the cell ratio has clear impact on  $SPNM$  at subthreshold  $V_{dd} = 0.3V$  during hold, read and write operations. In subthreshold, the dependence of  $SNM$  obtained from the butterfly curve has very little (unnoticeable) impact of cell ratio [4]. However, power metric  $SPNM$  and  $WTP$  obtained from N-curve at sub-threshold  $V_{dd} = 0.3V$  shows the consistent trend as it is at  $V_{dd} = 1.2V$ . Hence, the proposed metrics provides better information compare to  $SNM$  at ultra low voltage and can be useful for stability analysis at this regime.

### B. Dependence on the Supply Voltage $V_{dd}$

The  $SNM$  obtained from the VTC delimits to a maximum  $0.5V_{dd}$  because of the two sides of the butterfly curve [4]. Fig. 6 shows the dependence of power metrics  $SPNM$  and  $WTP$  on  $V_{dd}$  for a standard 6T-SRAM cell. The power metrics  $SPNM$  and  $WTP$  for hold, read and write operations reveals that  $V_{dd}$  scaling no longer limits the SRAM cell stability to the ideal value of  $0.5V_{dd}$ . Thus, the proposed metrics dependency on  $V_{dd}$  as shown in Fig. 6 will not limit the stability analysis and can be used at a very low voltage.

### C. Dependence on Random Dopant Fluctuation

The variations in threshold voltage of an SRAM cell transistors due to random dopant fluctuations is the principal reason for parametric failures [2]. The parametric failures such as read and write failures in SRAM can be characterized by the target value of  $SPNM$  and  $WTP$  which determines the yield. The target value of the  $SPNM$  and  $WTP$  are formulated statistically to take the variability into account due to  $V_{th}$ . We assume that the variation of  $V_{th}$  as an independent random variable for all the six transistors in SRAM cell with a Gaussian distribution defined by mean  $\mu$

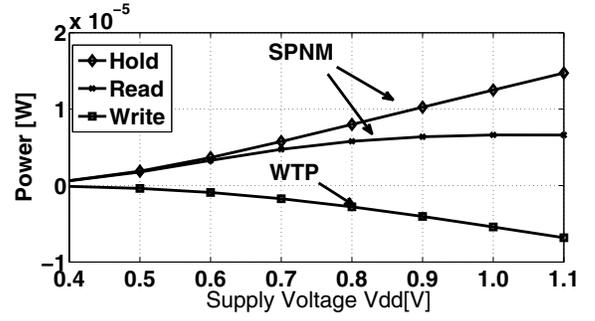


Fig. 6. Supply Voltage  $V_{dd}$  dependency of SPNM and WTP.

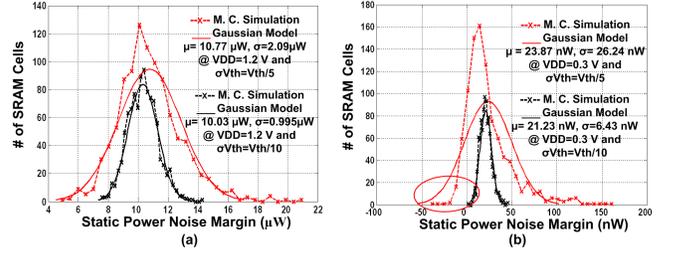


Fig. 7. The estimated SPNM from Gaussian model and MC simulation results for read access with  $V_{th} = 20\%$  and  $V_{th} = 10\%$  variations at (a)  $V_{dd} = 1.2V$  and (b)  $V_{dd} = 0.3V$ .

and variance  $\sigma^2$ . The mean ( $\mu_{SPNM}$  and  $\mu_{WTP}$ ) and variance ( $\sigma_{SPNM}^2$  and  $\sigma_{WTP}^2$ ) of the random variable  $SPNM$  and  $WTP$  can be estimated by applying the Taylor series theorem [7]. These are presented in the following equations:

$$\begin{aligned} \mu_{SPNM} = & SPNM + 0.5 \sum_{i=1}^{i=4} \left( \frac{\partial^2 SPNM}{\partial V_{th,i}^2} \sigma^2 V_{th,i} \right) \\ & + 0.5 \sum_{i=1}^{i=2} \left( \frac{\partial^2 SPNM}{\partial V_{th,ATi}^2} \sigma^2 V_{th,ATi} \right), \end{aligned} \quad (3)$$

$$\begin{aligned} \sigma_{SPNM}^2 = & \sum_{i=1}^{i=4} \left( \frac{\partial SPNM}{\partial V_{th,i}} \right)^2 \sigma^2 V_{th,i} \\ & + \sum_{i=1}^{i=2} \left( \frac{\partial SPNM}{\partial V_{th,ATi}} \right)^2 \sigma^2 V_{th,ATi}, \end{aligned} \quad (4)$$

$$\begin{aligned} \mu_{WTP} = & WTP + 0.5 \sum_{i=1}^{i=4} \left( \frac{\partial^2 WTP}{\partial V_{th,i}^2} \sigma^2 V_{th,i} \right) \\ & + 0.5 \sum_{i=1}^{i=2} \left( \frac{\partial^2 WTP}{\partial V_{th,ATi}^2} \sigma^2 V_{th,ATi} \right), \end{aligned} \quad (5)$$

$$\begin{aligned} \sigma_{WTP}^2 = & \sum_{i=1}^{i=4} \left( \frac{\partial WTP}{\partial V_{th,i}} \right)^2 \sigma^2 V_{th,i} \\ & + \sum_{i=1}^{i=2} \left( \frac{\partial WTP}{\partial V_{th,ATi}} \right)^2 \sigma^2 V_{th,ATi}. \end{aligned} \quad (6)$$

Where  $V_{th,i}$  and  $V_{th,ATi}$  are the threshold voltage of  $i^{th}$  and  $ATi^{th}$  transistors. We use Eqs. 3- 6 to estimate the process variation tolerance in Section V.

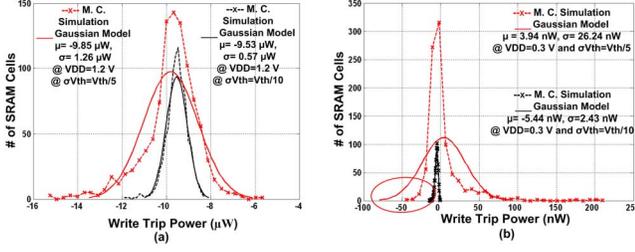


Fig. 8. The estimated WTP from Gaussian model and MC simulation results with  $V_{th} = 20\%$  and  $V_{th} = 10\%$  variations at (a)  $V_{dd} = 1.2V$  and (b)  $V_{dd} = 0.3V$ .

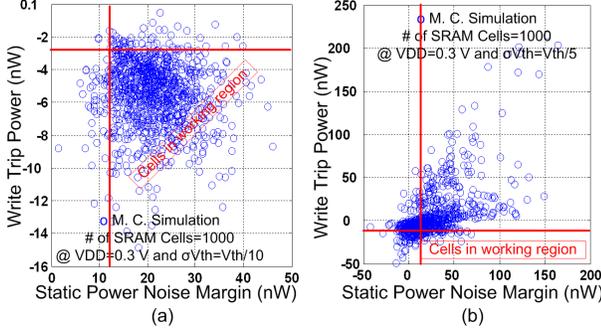


Fig. 9. MC simulation results for SPNM and WTP at  $V_{dd} = 0.3V$  and threshold voltage (a)  $V_{th} = 10\%$  variations and (b)  $V_{th} = 20\%$  variations.

## V. STATISTICAL ANALYSIS OF THE DERIVED METRICS

Fig. 7 and 8 shows the MC simulations and estimated mean  $\mu$  and standard deviation  $\sigma$  at  $V_{dd} = 1.2V$  and  $V_{dd} = 0.3V$  for intra-die variations in threshold voltage ( $V_{th} = 20\%$  and  $V_{th} = 10\%$ ). Fig. 7 (a) shows that all the cells have enough  $SPNM$  at  $V_{dd} = 1.2V$ . But, the  $\sigma_{SPNM}$  at  $V_{th} = 20\%$  is 2X higher than the  $\sigma_{SPNM}$  at  $V_{th} = 10\%$  and mean  $SPNM$  is roughly equal for  $V_{th} = 20\%$  and  $V_{th} = 10\%$  variations. The similar trend for  $WTP$  as indicated in Fig. 8(a) with higher standard deviation at  $V_{th} = 20\%$ . These statistical results of  $SPNM$  and  $WTP$  are summarize in Table I.

The estimated  $SPNM$  and  $WTP$  for subthreshold operation ( $V_{dd} = 0.3V$ ) with 20% and 10% variations in  $V_{th}$  is shown in Fig. 7 and 8 (b). We set the upper and lower bounds of the target parameters  $SPNM$  and  $WTP$  for working ( $SPNM > 0$  and  $WTP < 0$ ) and non-working ( $SPNM < 0$  and  $WTP > 0$ ) cells based on SPICE simulations results.

The  $SPNM$  of about 93 cells in subthreshold operation is negative as encircled in Fig. 7(b), which indicates the read access failure of the SRAM cell according to the set bounds. The  $WTP$  for subthreshold operation at 20% variations in  $V_{th}$  causes about 90% cells failure, as the mean  $WTP$  is positive and standard deviation is very large, also very fewer number of cells having negative  $WTP$  as marked in Fig. 8(b). In Fig. 9 we put both the metrics together  $SPNM$  versus  $WTP$  obtained from MC simulations and divided them in working and non-working regions according to the set bounds. In Fig. 9 (a) some of the cells are having very small positive  $SPNM$  and positive  $WTP$ , which causes about 10% cells failure indicated as cells in working region, whereas in Fig. 9 (b) a large number of cells showing positive  $WTP$  and fewer cells showing positive  $SPNM$ , which causes 90% of cells failure indicated as cells in working region. These statistical results of  $SPNM$  and

TABLE I

STATISTICAL DISTRIBUTION OF  $SPNM$  AND  $WTP$  AT  $V_{dd} = 1.2V$

$V_{dd} = 1.2V$	Mean ( $\mu$ )		Std.Devi. ( $\sigma$ )	
	10% $V_{th}$	20% $V_{th}$	10% $V_{th}$	20% $V_{th}$
$SPNM(\mu W)$	10.03	10.77	0.99	2.09
$WTP(\mu W)$	-9.53	-9.85	0.57	1.26

TABLE II

STATISTICAL DISTRIBUTION OF  $SPNM$  AND  $WTP$  AT  $V_{dd} = 0.3V$

$V_{dd} = 0.3V$	Mean ( $\mu$ )		Std.Devi. ( $\sigma$ )	
	10% $V_{th}$	20% $V_{th}$	10% $V_{th}$	20% $V_{th}$
$SPNM(nW)$	21.23	23.87	6.43	26.24
$WTP(nW)$	-5.44	3.94	2.43	26.93

$WTP$  are summarize in Table II.

## VI. CONCLUSIONS

The stability analysis of an SRAM cell based on power metrics,  $SPNM$  and  $WTP$  is presented in this paper. The limitations of the  $SNM$  as a stability metric for ultra low power nano-CMOS SRAM cell are highlighted and compared with the proposed metrics. We have exhaustively analyze the impact of different parameter variations on  $SNM$ ,  $SPNM$ , and  $WTP$  for a 6T-SRAM cell in subthreshold. Simulation results shows that the derived power metrics provides better stability analysis for ultra low power nano-CMOS SRAM cell. Also, derived metrics  $SPNM$  and  $WTP$  confirm the normally distributed results estimated from the MC simulations.

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