

# Single Ended Static Random Access Memory for Low- $V_{dd}$ , High-Speed Embedded Systems

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**Abstract**—Single-ended static random access memory (SE-SRAM) is well known for their tremendous potential of low active power and leakage dissipations. In this paper, we present a novel six-transistor (6T) SE-SRAM bitcell for low- $V_{dd}$  and high-speed embedded applications with significant improvement in their power, performance and stability under process variations. The proposed design has a strong  $2.65\times$  worst case read static noise margin (SNM) compared to a standard 6T SRAM. A strong write-ability of logic ‘one’ is achieved, which is problematic in SE-SRAM cells even at lower voltage. The proposed bitcell design is mainly targeted for word-organized SRAMs. A  $16 \times 16 \times 32$  bit SRAM with proposed and standard 6T bitcells is simulated (including parasitics) for  $65nm$  CMOS technology to evaluate and compare the different performance parameters, such as, read SNM, write-ability, access delay and power. The dynamic and leakage power dissipation in the proposed 6T design is reduced by 28% and 21%, respectively, as compared to standard 6T design.

## I. INTRODUCTION

Embedded systems particularly targeted towards low duty-cycles and portable applications such as mobile phone or PDAs require extremely low energy consumption as they are often battery powered. In such systems, a significant amount of power is consumed during memory accesses which determines the battery life. Hence, efficient active and leakage power saving SRAM designs need to be explored for higher reliable and longer operation of battery powered applications. There are mainly two areas with strong potential of active power saving: (a) reduction in charging capacitance or static current by partial activation of multi-divided word and bit lines and (b) lowering operating voltage resulting from external power supply reduction and half- $V_{dd}$  precharging [10]. In [13], 30% to 70% of the total active power is dissipated in bit lines charging and discharging during read and write operation. Hence, reduction in charging capacitance or static current has strong prospect of active power saving. *In the proposed design we have exploited this fact to reduce the active power despite of full- $V_{dd}$  precharging of the bitline.* The precharging of bitline to full- $V_{dd}$  is mainly to achieve strong write-ability of logic ‘one’ into the bitcell which makes easier to operate the SRAM at lower  $V_{dd}$ .

Lowering supply voltage to reduce power (energy) consumption is one of the first choice of designers for ultra-low-power applications. However, ultra-low-power design of

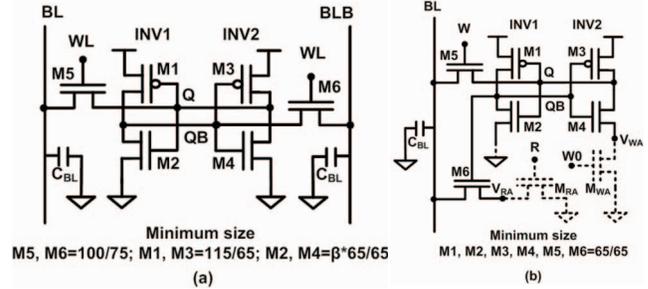


Fig. 1. The proposed single-ended 6T SRAM cell with dotted read and write assist transistors shown in (b) with respect to standard 6T SRAM cell shown in (a).

high-density SRAMs in which the operating voltage is below the transistor threshold voltage is extremely challenging. This is due to reduced static noise margin (SNM) and increased variability in design and process parameters in the nanoscale CMOS (nano-CMOS) technology. As we move from  $130nm$  to  $65nm$  technology node, the area occupied by the memory increases from 71% to 82% [1]. In modern system on chips (SoCs) when total power and total area is dominated by the SRAM, reduction in  $V_{dd}$  for SRAMs can save both active energy and leakage power [9]. Also for system integration, SRAM must be compatible with subthreshold combinational logic operating at ultra-low voltages [14]. However, this leads to increase in sensitivity of design and process parameter variability. This problem will worsen in nanometer technologies with ultra-low voltage operation and makes SRAM design and stability analysis more challenging. These practical challenges limit standard 6T SRAM bitcells and architectures to higher  $V_{dd}$ . A standard 6T SRAM bitcell in  $65nm$  CMOS technology is shown in Fig. 1 (a) [11]. The data storage node Q and QB in standard 6T bitcell are most vulnerable to capacitive coupling noise due to bitlines (BL and BLB) and voltage division effect between access transistors and pulldown transistors. A proper sizing of these transistors is important to maintain data stability and functionality as shown in Fig. 1(a).

This paper introduces a 6T bitcell and its word-organization for robust and high density SRAMs in the subthreshold regime. In proposed 6T SEIO bitcell: 1) read current path is isolated from the data storage node Q and QB hence, less vulnerable to noise; 2) isolation of read current path improves the read SNM  $2\times$  compared to standard 6T bitcell with  $\beta = 2$  and at

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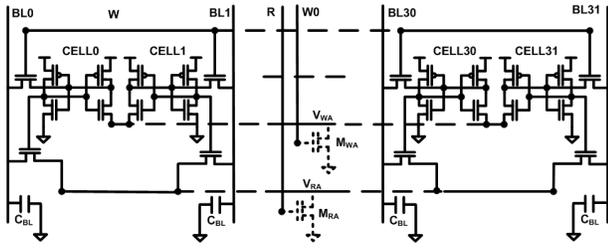


Fig. 2. A 32-bit word organization of the proposed 6T SE-SRAM cell with dotted read and write assist transistors.

$V_{dd} = 0.2V$  and  $1.0V$ ; 3) process variation degrade the read SNM of proposed 6T and standard 6T SRAM bitcells by up to 13% and 50% respectively thereby,  $2.65\times$  tolerance to process variability. A model for determining the size of the read/write assist transistors is developed for estimation of read access delay with accuracy of up 95%. The dynamic and leakage power dissipation in the proposed 6T design is reduced by 28% and 21%, respectively, as compared to its counterpart design.

The rest of the paper is organized as follows: Section II introduces the proposed bitcell and word-organized SRAM design. In Section III, statistical analysis of parametric failures is presented. Read and write assist transistors sizing issues are discussed in Section IV. In Section V, dynamic and leakage power of the standard and proposed designs are compared. Section VI provides a summary of the key conclusions.

## II. A PROPOSED SEIO 6T SRAM BITCELL DESIGN

Fig. 1 (b) shows the proposed single ended input/output 6T SRAM bitcell schematic with minimum feature sized transistors for a 65nm CMOS technology. The proposed 6T SRAM bitcell consists of a cross coupled inverter pair (INV1 and INV2) connected to a bitline (BL) using access transistor (M5) and a storage node isolation transistors (M6). The dotted transistors in the figure ( $M_{WA}$  and  $M_{RA}$ ) represent read and write assist transistors, respectively, for a memory word. A memory word can be 8, 16, or 32 bit. Three control signals  $W$ , its complement  $W0$  and  $R$  are used for controlling the write and read operations. The write operation is controlled by  $W$  and  $W0$ . These signals are respectively connected to M5 and  $M_{WA}$ . While read operation is controlled by  $R$  which is connected to  $M_{RA}$ .

In the following, we illustrate the word-organized SARM design architecture with proposed bitcell. Let,  $n$  be the number of cells in a word-organized memory which contains more than 1-bit per word, that is,  $n \geq 2$ . For instance, the word-organization of the proposed 6T SRAM bitcell for  $n = 32$ , is shown in Fig. 2. Since read and write operations access the  $n$  bits of a word simultaneously, one could share the read/write assist transistors of a bitcell as shown dotted in Fig. 1(b). Therefore, we need only one read/write assist transistor per word. Consequently, each bitcell in a word consists of six transistors with two additional dotted transistors per word (Fig. 2). Sizing issues of these shared (dotted) transistors are

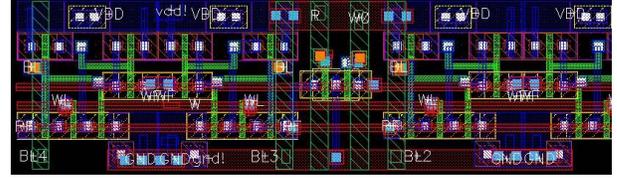


Fig. 3. Layout of the proposed word-organized 6T SRAM bitcell with four bitcells and read/write assist transistors in the middle.

explained in Section IV.

Fig. 3 shows the layout of the proposed word-organized 6T SRAM bitcell with four bitcells and read/write assist transistors. We present only four cells for clarity. The propped bitcell layout area is  $0.68\mu m^2$  ( $0.55\mu m \times 1.22\mu m$ ), which is 8% higher (because of additional contacts) than the standard 6T SRAM bitcell for  $\beta = 2$ . While, read/write assist transistors occupies merely half of the bitcell area per word. We have used three metal layers (M1, M2 and M3). Metal layer M1 is used for routing the supply rails ( $V_{dd}$  and  $G_{nd}$ ), M2 is used for routing the shared contacts among bitcells, read and write signals. While, M3 is used for routing the bitlines. The design has been successfully laid-out for different word sizes. Parasitic were extracted and included in a SPICE deck for simulation results presented in this paper.

### A. Read Operation

Information read out from the proposed SRAM bitcell is carried out via single ended bitline (data-line). Prior to read operation, BL is precharged to  $V_{dd}$  and the read signal ( $R$ ) is asserted high ( $W$  is low) to turn on the  $M_{RA}$ , which is essentially applicable for reading '0'. For reading '1', BL has to remains at precharged level ( $\sim V_{dd}$ ) because transistor M6 is turned off. It is important to notice that only the read '0', high to low transition is affected by the insertion of the  $M_{RA}$  and that the read '1', low to high transition will not be affected. As a result, reading '1' is directly sensed from the precharged BL. In both the cases either reading '1' or '0', storage nodes are isolated from the read current path. It results reduced capacitive coupling noise due to BL and hence, significantly enhancing the data stability during read and hold state. Also compared to standard 6T bitcell the read current path has equal number (two) of series connected transistors with minimum feature size resulting in better performance of proposed 6T bitcell.

Read static noise margin (SNM) of the proposed 6T and standard 6T SRAM bitcells are shown in Fig. 4 for a comparative perspective. The proposed 6T bitcell has an SNM of  $0.302V$ , while the standard 6T bitcell SNM is  $0.152V$  at a supply voltage of  $1.0V$  and  $\beta = 2$  (Fig. 4(a)). The SNM of the proposed 6T bitcell at a supply voltage of  $0.3V$  is equal to that of the standard 6T bitcell at  $0.5V$  and  $\beta = 4$  (Fig. 4(b)). However, the SNM normalized to supply voltage for different

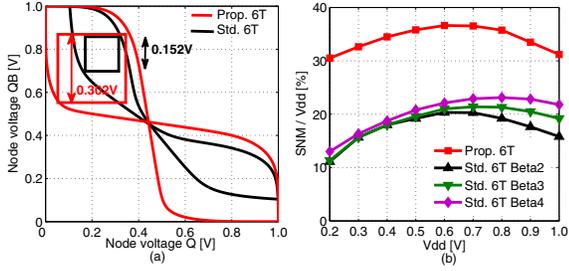


Fig. 4. SNM comparison of standard SRAM and proposed SRAM cell during a read operation at  $V_{dd} = 1V$  in Fig. (a). SNM normalized to supply voltage for different cell ratio ( $\beta = 2, 3$  and 4) is shown in Fig. (b).

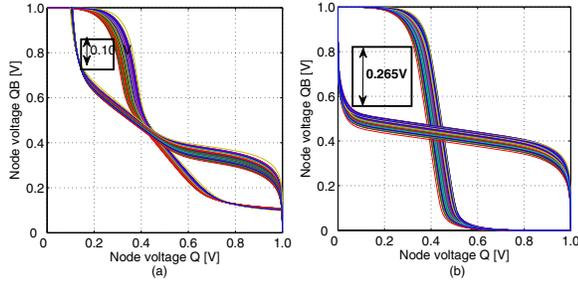


Fig. 5. Monte Carlo simulation of voltage transfer characteristics (VTCs) shown with worst case SNM during read operation under process variations: (a) for standard SRAM and (b) for proposed SRAM bitcell.

cell ratio ( $\beta = 2, 3$  and 4) in Fig. 4(b) shows that the variation of SNM in the proposed 6T bitcell (for minimum feature size) is smaller than that of the standard 6T bitcell, which is mainly because of reduced capacitive coupling noise due to BL and isolation of read current path from the storage node Q and QB.

### B. Write operation

It is well known that the write operation in single ended SRAM cell is difficult because of strongly cross coupled inverters. A write assist transistor  $M_{WA}$  is used to alleviate this problem, which is controlled by W0 for a successful write operation. The usage of  $M_{WA}$  is to weaken the cross coupling of proposed 6T SRAM bitcell inverters during write access time.

Initially assume that the node Q= 0 and QB= 1, we need to change these node states. In write mode, write signal (W) is asserted high to turn on the write access transistor M5 that connects the precharged bit line to node Q. As both the inverters (INV1 and INV2) are strongly cross coupled so forcing the node Q to '1' is difficult through an NMOS (M5) pass device. Hence, we weaken the pull down strength of INV2 by inserting a series transistor  $M_{WA}$ , which is controlled by a complement of write signal W0 to turned off during write operation. In other words,  $M_{WA}$  is used to weaken the strongly cross coupled inverters.

The timing waveforms of read and write control signals (R and W), input and output data (Data-Write and Data read), and bitcell node Q are shown in Fig. 6. While the timing

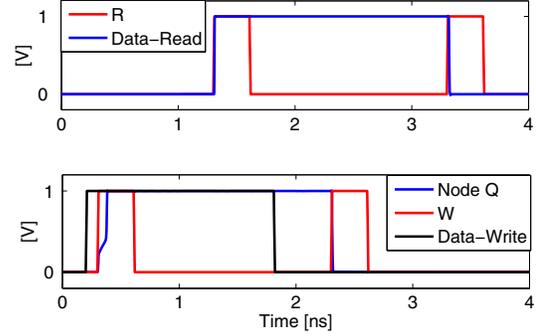


Fig. 6. Timing simulation waveforms for write and read operations of proposed 6T bitcell.

waveforms of clock, decode, precharge, and sense stage signals are not shown. One can observed that the information has been effectively written and readout from the proposed word-organized 6T SRAM bitcell design.

## III. STATISTICAL ANALYSIS OF PARAMETRIC FAILURES

The variations in threshold voltage of an SRAM cell transistors due to random dopant fluctuations is the principal reason for parametric failures [4]. Parametric failures in standard 6T SRAM bitcell can occur due to (a) destructive read (cell may flip when access for read), (b) un-successful write i.e., bitcell cannot be written within the write access time, which is measured in terms of trip voltage of an inverter, and (c) read access failure i.e., incorrect read operation, which is a strong determinant of performance and power of the SRAM. For parametric failure analysis, we assume a 15% variation in  $V_{th}$  with  $3\sigma$  as an independent random variable for all the transistors in SRAM cell with a Gaussian distribution.

### A. Destructive read

Data retention of the 6T SRAM bitcell during the read and hold operation is an important functional constraint, which is measured in terms of read and hold SNM. The SNM is a widely used metric for stability analysis of an SRAM bitcell usually defined as the maximum value of dc noise voltage ( $V_n$ ) that can be tolerated by the SRAM cell without flipping the node states. During the read operation, voltage at node QB (= 0) is most vulnerable to noise due to potential divider action in read current path of M5 and M2 to a positive value of  $V_n$ . If  $V_n$  is higher than the trip voltage of the INV2, then the cell flips resulting destructive read failure. In the proposed 6T SRAM bitcell the nodes (Q and QB) are isolated from the read current path to circumvent the noise vulnerability. Process variations in  $V_{th}$  degrade the read SNM of standard 6T and proposed 6T SRAM cell by up to 50% and 13% respectively compared to nominal design corner as shown in Fig. 5. The proposed 6T SRAM bitcell provide 2.65X higher worst-case read SNM as compared to the standard 6T SRAM bitcell under same process variations. Thus, the proposed 6T bitcell has better noise margin, worst-case read stability and process variation tolerant.

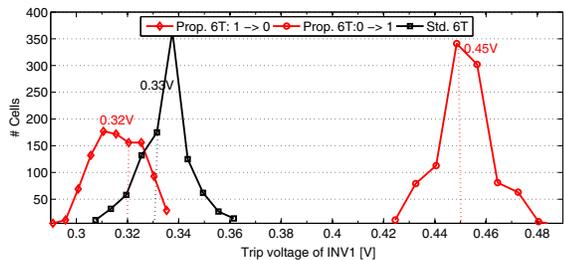


Fig. 7. Monte Carlo simulation of write trip voltage of the standard and proposed 6T SRAM bitcell.

### B. Un-successful write

Write ability of a standard 6T SRAM bitcell is best characterized using write trip voltage which is defined as the maximum voltage on the bitline needed to flip the bitcell content [6]. Due to asymmetric nature of the proposed 6T SRAM bitcell, we need to analyze both the state write ‘1’ and ‘0’. In order to write ‘1’ ( $Q = 1$  and  $QB = 0$ ) to a cell storing ‘0’ ( $Q = 0$  and  $QB = 1$ ), low internal node Q of the cell is pulled up above the trip voltage of the INV1. Since, pull down strength of the INV2 has been weakened during write access time due to stacked transistor  $M_{WA}$ , which makes pulling up of low internal node Q above the trip voltage easier. Similarly, writing ‘0’ ( $Q = 0$  and  $QB = 1$ ) to a cell storing ‘1’ ( $Q = 1$  and  $QB = 0$ ), high internal node Q of the cell has to discharge via bitline (BL) well below the trip voltage of the INV1 so that the cross-coupled inverter pair starts working and the cell content gets flipped. To guarantee that a correct write operation will occur, it is important that the node Q should be pulled up (down) above (below) the trip voltage of INV1 within the write access time when W is high otherwise a write failure will occur. Under process variation, statistical analysis of write-ability shows that the mean value of the write trip voltage for writing  $1 \rightarrow 0$  is  $0.32V$ , whereas for writing  $0 \rightarrow 1$  is  $0.45V$ . However, mean value of write trip voltage for writing ‘1/0’ of standard 6T bitcell is  $0.33V$ . The write trip voltage standard deviation due to process variations in standard and proposed 6T bitcells are almost equal of about  $10mV$ , as shown in Fig.7. Thus, the write ability of the proposed bitcell has not degraded under process variation

### C. Read access failure

The bitcell read access time or critical path in SRAM memories typically determines the memory performance and ensures the correct read operation. For a successful read operation, read access time is defined as the time required to produce a pre-specified voltage difference between two bit lines of a standard 6T SRAM bitcell [3], [12]. In proposed 6T SRAM bitcell the critical read access time correspond to reading ‘0’, which determines the performance of the proposed bitcell. Since ‘1’ is directly sensed from the precharged bitline. The read access time (for ‘0’) of the proposed bitcell is defined as the time required to produce a pre-specified voltage difference between reference and single bitline voltage. Statistical read

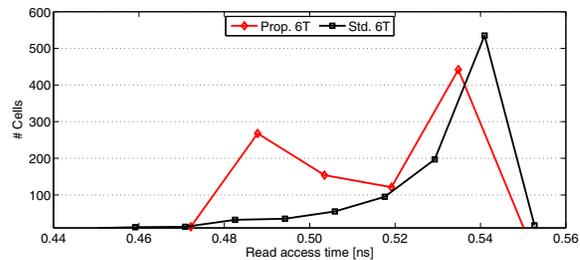


Fig. 8. Monte Carlo simulated read access time of the standard and proposed 6T SRAM bitcells.

access time distribution of standard and proposed 6T SRAM bitcells are shown in Fig. 8. Under process variation, mean value of the read access time of standard 6T bitcell is  $0.53ns$ , which is 4% higher ( $0.51ns$ ) than the proposed 6T bitcell. While, standard deviation in read access time of standard 6T bitcell ( $0.020ns$ ) which is 14% higher ( $0.017ns$ ) than the proposed 6T bitcell. Thus, the proposed cell has better process variation acceptance than the standard 6T bitcell.

## IV. SIZING OF READ AND WRITE ASSIST TRANSISTORS

Proper sizing of read/write assist transistor is very crucial because whole functioning and performance of a memory block depends on these transistors. If we overestimate their size, then there is a wastage of valuable silicon area and increase of switching power dissipation because of larger loading. Similarly, if we underestimate the size, then the read and write operations would be too slow because significant delay due to the increased resistance to ground. Usage of both the transistors is fundamentally different because one (read assist) transistor has to provide low resistive path to read current during read operation. On the other hand (write assist) transistor has to provide high resistance path for successful write operation to weaken the cross coupling of bitcell inverters. As both read and write requirements are conflicting in nature, so we need to analyze the sizing issues separately for read and write assist transistors.

### A. Sizing of read assist transistor

As we have seen in Section III, the read assist transistor forms the critical path, essentially when reading ‘0’ from the proposed bitcell. Hence, performance of the proposed SRAM is determined by the ‘0’ read access time, which is mainly dependent on the size of  $M_{RA}$ . Consequently, size of the  $M_{RA}$  in word-organized SRAM design when a word has common read assist transistor ( $M_{RA}$ ) is critical for proper functioning of SRAM. We have developed a simple model to determine the minimum size of  $M_{RA}$  and corresponding ‘0’ read access delay for a single cell, which is extended for proposed word-organized SRAM design. The proposed model is inspired by well-established power gating techniques in which sleep transistor is used to gate the power supply [7]. In the literature [7], [8], it was shown that the sleep transistor can be approximated as a linear resistor to create a virtual ground because  $V_{ds} < (V_{gs} - V_{th})$  of sleep transistor. Here,

this sleep transistor is referred as read assist transistor ( $M_{RA}$ ). The amount of current flowing through the linearly-operating  $M_{RA}$  transistor can be approximated as [5]:

$$I_{RA} \approx \mu_n C_{ox} \left( \frac{W}{L} \right)_{RA} (V_{dd} - V_{th}) V_{RA}, \quad (1)$$

where  $\mu_n$  is the mobility of electrons,  $C_{ox}$  is the oxide capacitance and  $V_{th}$  is the threshold voltage. Since, the  $M_{RA}$  is approximated as linear resistor and operating in a linear region, then the  $M_{RA}$  resistance  $R_{RA} \approx \frac{V_{RA}}{I_{RA}}$ . Thus, the size of the read assist transistor can be expressed as:

$$\left( \frac{W}{L} \right)_{RA} = \frac{1}{R_{RA} \mu_n C_{ox} (V_{dd} - V_{th})}. \quad (2)$$

If  $R_{RA}$  is known, then the size of the read assist transistor  $(W/L)_{RA}$  can be determined by using the above expression 2. The  $M_{RA}$  affects only high to low transition or reading ‘0’ to discharge the precharged bitline. Since, bitline capacitance  $C_{BL}$  is discharging, and neglecting the node  $V_{RA}$  parasitic capacitance, any charge flowing out of the source of M6 will flow through the read assist resistor  $R_{RA}$  of  $M_{RA}$ . This phenomenon is modeled as a  $R$ - $C$  circuit, which comprises of series resistor  $R_{RA}$  and bit line capacitance  $C_{BL}$  charged at voltage  $V_{dd}$ . Thus, the relationship among these parameters can be expressed as follows:

$$V_{RA} = V_{dd} \times \exp\left(\frac{-t}{\tau}\right). \quad (3)$$

Where  $\tau$  is the time constant, the read sensing circuitry will detect the transition high to low i.e. read ‘0’ only when the bit line is discharged to about 36.8% of the  $V_{dd}$  after a certain amount of delay from the assertion of read control signal, which is defined as a read access delay. Under this condition the read access delay  $\tau_d$  is equal to time constant ( $\tau$ ):

$$\tau_d = R_{RA} C_{BL}. \quad (4)$$

In the word-organized SRAM array shown in Fig. 2, let the word is  $n$ -bit wide i.e. there are  $n$ -bitcells in each word and all are having individual  $M_{RA}$ . These individual  $M_{RA}$  of  $n$ -bitcells in a word are replaced by an equivalent  $M_{RA}$  to reduce the transistor count and silicon area overhead. The size of  $M_{RA}$  in worst case pattern (i.e. when all the  $n$ -cells having ‘0’ at node Q) determines the read access delay or operating frequency of the SRAM. As we have approximated the  $M_{RA}$  of a cell as a linear resistor, then all the  $n$ -bitcells  $M_{RA}$  will form a parallel combination of  $n$ -linear resistors in worst case pattern. In this case, the  $M_{RA}$  resistance will be equivalent to  $M_{RA}/n$ . Similarly,  $n$ -precharged bitlines capacitance (neglecting the node capacitance) will be replaced by an equivalent capacitance  $nC_{BL}$  because of parallel combination they form. Once we have an equivalent resistance, capacitance and target read access delay then from eqns. 2- 4, we can determine the size of the  $M_{RA}$  for any word size. The SPICE simulation and estimated results for read assist transistor size (W/L) and read access delay for different word sizes ( $n=8, 16, 32$  and 64) of the proposed word-organized SRAM designs are shown

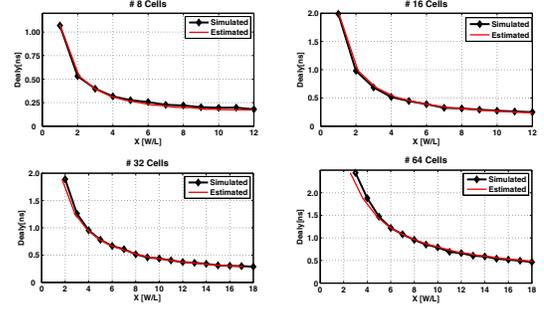


Fig. 9. Estimation of read access delay for different read assist transistor size (W/L).

in Fig. 9. One can observe that the proposed model archives up to 95% accuracy in estimation of read access delay for different word sizes.

### B. Sizing of write assist transistor

In the proposed word-organized SRAM array, all individual SRAM bitcell’s  $M_{WA}$  transistors are replaced by a single equivalent transistor ( $M_{WA}$ ). Thus,  $M_{WA}$  should be sized properly so that all the cells in that word written correctly. In worst case scenario, that can be either writing ‘1’ or ‘0’ in all the cells. The  $M_{WA}$  has to weaken the cross coupled inverters by floating the INV2 of all the bitcells in that word. Weakening of the loop doesn’t matter whether we are intended to write ‘1’ or ‘0’ in all or fewer cells in that word. The weakening of the loop of a single bitcell or all the bitcells in a word is equivalent because  $V_{ds}$  of  $M_{WA}$  is always higher than the ‘0’, when  $V_{GS}$  of  $M_{WA}$  is zero. Thus, a minimum sized transistor would be well suited for this purpose. Also after the write access time  $M_{WA}$  has to provide a ground to node  $V_{RA}$  of all the bitcells. For providing a ground to node  $V_{RA}$ ,  $M_{WA}$  has to provide only the leakage current path to all the bitcells either they are having ‘0’ or ‘1’ at node Q. Since, the transistor  $M_3$  (when node Q at ‘0’) and transistor  $M_4$  (when node Q at ‘1’) are in cutoff mode, therefore, there is only leakage current has to flow through  $M_{WA}$ . As  $M_{WA}$  has to provide only the leakage current path to all the bitcells of a word which will always less than the dynamic current of a transistor even when all the cells are writing either ‘1’ or ‘0’ simultaneously. Also, for minimum leakage and data retention it is recommended to use minimum size of transistor. The SPICE simulation for different word size of SRAM reveals that there is no significant improvement in the write-ability of the SRAM with increasing the size of  $M_{WA}$ .

## V. POWER CONSUMPTION

A  $16 \times 16 \times 32$  bit SRAM memory with 32 bitcells in a word using standard and proposed 6T bitcell designs was simulated in SPICE, operated at a clock speed of  $1GHz$  and  $V_{dd} = 1V$ . The simulation results are based on the BPTM of 65nm-technology node [2]. The dynamic power consumption of a standard and proposed bitcells under different read and

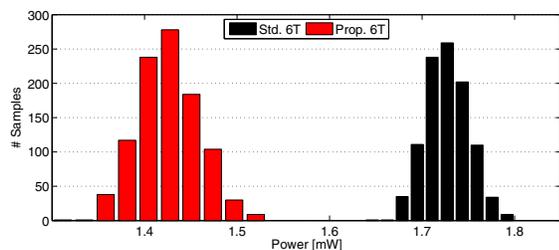


Fig. 10. Statistical distribution of leakage power for the proposed and standard SRAM.

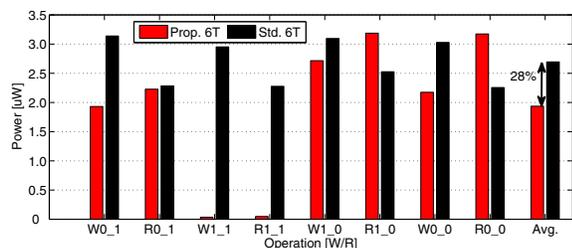


Fig. 11. Dynamic power pattern for different read/write operations of proposed and standard 6T SRAM bitcells.

write operations is shown in Fig. 11. Because proposed bitcell is asymmetric, its dynamic power consumption pattern is also asymmetric. In Fig. 11, operation W0\_1 stands for writing ‘1’ into the cell while its original content is ‘0’. Similarly, R1\_0 stands for reading ‘0’ from the cell, while previous output was ‘1’. The dynamic power consumption of the proposed bitcell under different combinations are quite different because of asymmetric nature. For operations W1\_1 and R1\_1, the dynamic power of proposed 6T bitcell is very low as compared to standard 6T bitcell, because both the operations are performed without discharging the bitline of the proposed bitcell. Under such operations precharged bitline can be used for future read/write operation. Alternatively, in standard bitcell one bitline has to discharge during these operations. However, the dynamic power for operations R1\_0 and R0\_0 in proposed 6T bitcell is 21% and 29% higher than the standard 6T bitcell. The average dynamic power under different read/write operations of the proposed 6T SRAM bitcell is 28% lower than the standard 6T bitcell [Fig. 11].

In 16X16X32 bit SRAM memory using proposed bitcells, reading a word “1110 1110....1110” consumes an average power of only 31% ( $3.86mW$ ) of the standard 6T SRAM memory array because of the reuse of the charged bitline. While, reading a word “0001 0001....0001” consumes 128% ( $15.94mW$ ) of the standard 6T SRAM memory. Reading a word with alternating values “1010 1010....1010” uses 68% ( $8.47mW$ ) of the standard 6T SRAM memory array power.

The leakage contribution pattern of the proposed bitcell is also asymmetric. When node Q= 0, it leaks more as compared to Q= 1 because the read current path transistor M6 is turned on. However, average leakage contribution in the proposed

cell is 37% less than the standard bitcell. For total leakage in  $16 \times 16 \times 32$  bit SRAM memory array (using proposed bitcells) in standby mode, when all the bitlines are charged to  $V_{dd}$ , access transistors (M5) of a word are cutoff and control signal read and write are clamped at ‘0’. Similarly, for standard 6T memory array bitlines are charged to  $V_{dd}$ , and control signals are clamped at ‘0’. The leakage power distribution under process variation for the proposed and standard SRAM array is shown in Fig. 10. The average leakage power consumption of the proposed SRAM array is  $1.4mW$ , which is 21% lower than the counterpart SRAM array. The standard deviation in leakage power of the proposed SRAM array is 42% higher ( $32\mu W$ ) than the standard SRAM array ( $23\mu W$ ).

## VI. CONCLUSION

A SEIO 6T bitcell design and its word-organization for robust and high density SRAMs is presented. The immunity to process variations (robustness) and high density in the proposed design is achieved by isolating the read current path and using minimum feature size transistors. The improved read and write-ability (data stability), reduced dynamic and leakage power dissipation compared to standard 6T, makes the new approach attractive for nanoscale technology regime in which process variation is a major design constraint. Experimental results shows that the proposed design has tremendous potential for nano-CMOS SRAM design.

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