iVAMS: Intelligent Metamodel-Integrated Verilog-AMS for Fast Analog Block Optimization

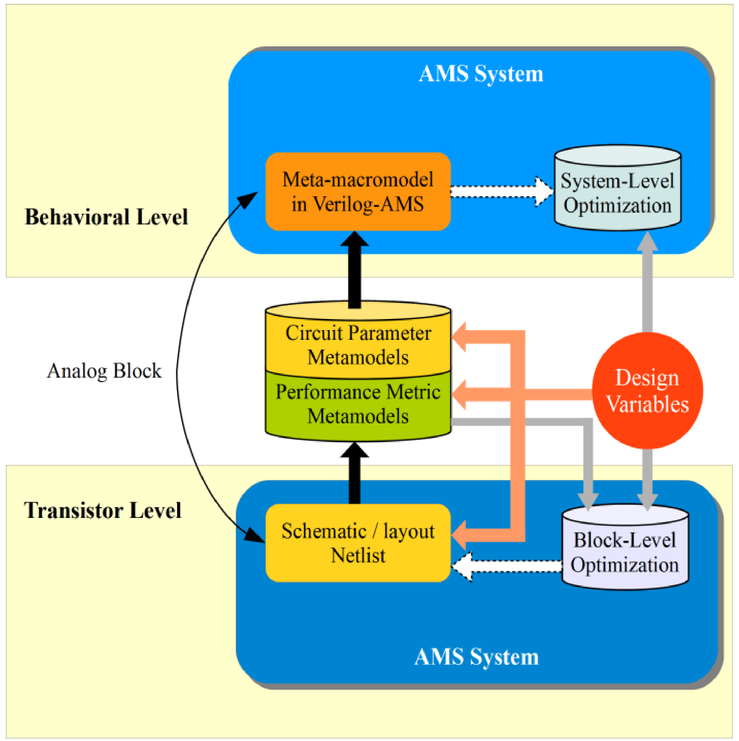
Geng Zheng, Saraju P. Mohanty, Elias Kougianos
NanoSystem Design Laboratory (http://nsdl.cse.unt.edu)
University of North Texas, TX 76203, USA.
Email: saraju.mohanty@unt.edu

Abstract

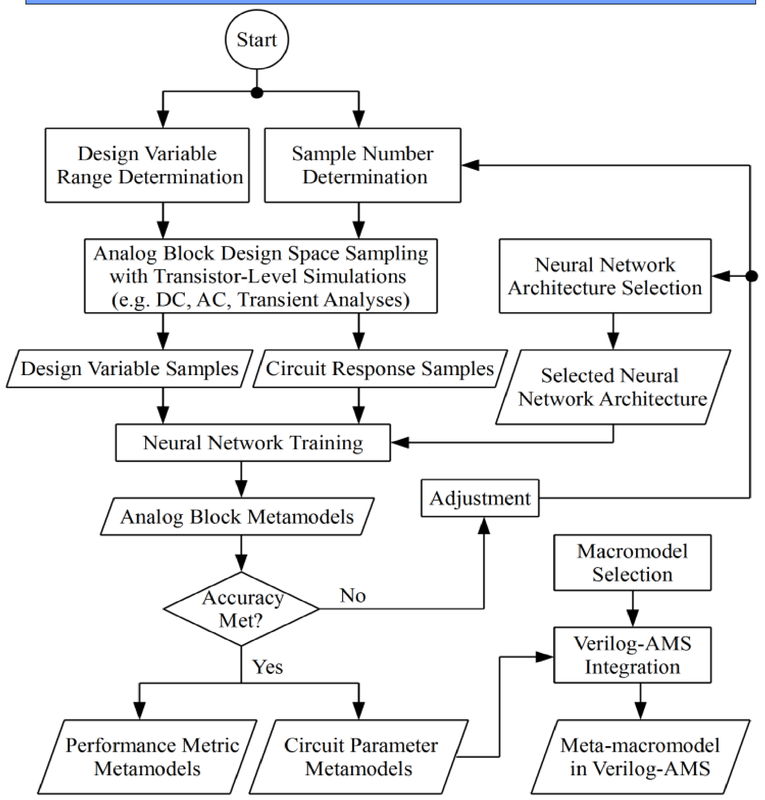
The gap between abstraction levels in analog design is a major obstacle for advancing analog and mixed-signal design automation. Intelligent surrogate models for low-level analog building blocks are needed to bridge behavioral and transistor-level simulations. Parameterized behavioral models in Verilog-AMS based on the artificial neural network (ANN) metamodels are constructed for efficient system-level design exploration. To the best of the authors' knowledge this is the first paper to integrate ANN models in Verilog-AMS. To demonstrate the application of iVAMS, a biologically-inspired "firefly optimization algorithm" is applied to an OP-AMP design. The optimization process is sped up by 5580X due to the use of iVAMS with negligible loss in accuracy.

iVAMS aims at closing the gap between behavioral- and transistor-level Analog/Mixed-Signal (AMS) design exploration

iVAMS Concept

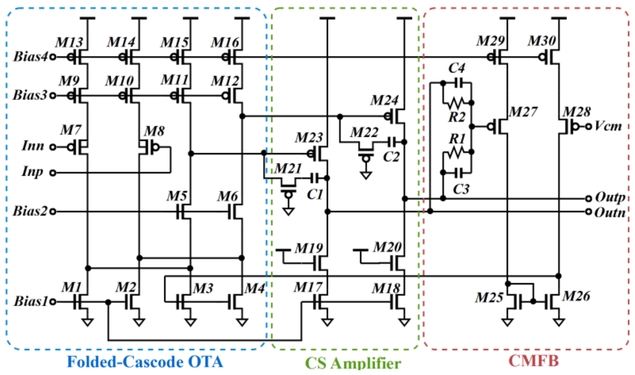


iVAMS Generation



Case Study Circuit: OP-AMP

A fully-differential OP-AMP:
- 90 nm CMOS process, 1-V supply
- 16 design variables (Ls and Ws, bias current...)



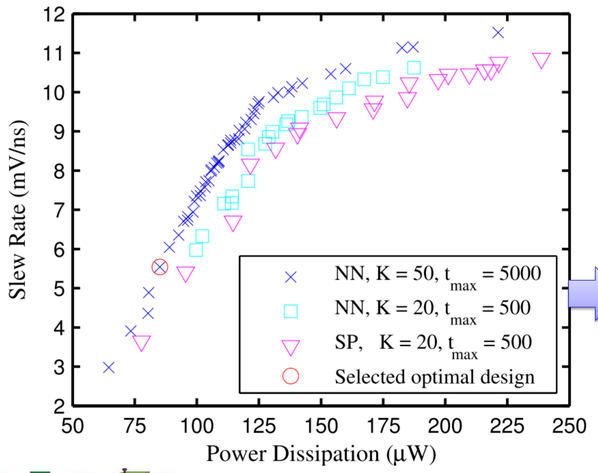
Metamodel Accuracy

- Artificial neural networks (500 samples)
- 2000-sample verification set

Metamodel		Accuracy Metric			
Output	Type	R^2	RMAE	RRSE	RMSE
A_0	NN	0.959	1.324	0.202	41.93 V/V
	PO	0.973	1.044	0.163	33.78 V/V
BW	NN	0.987	0.894	0.116	2.12 kHz
	PO	0.986	0.965	0.117	2.14 kHz
PM	NN	0.901	2.161	0.317	4.99^o
	PO	0.348	4.466	0.807	12.70^o
SR	NN	0.989	0.483	0.105	0.292 mV/ns
	PO	0.985	0.662	0.119	0.332 mV/ns
P_D	NN	0.996	0.523	0.062	8.306 μW
	PO	0.980	1.314	0.141	18.817 μW

Block-Level Optimization

A metaheuristic firefly algorithm is employed to generate the Pareto front:



Optimization #	1	2	3
Model Type	NN	NN	SP
Number of Pareto Points, K	50	20	20
Number of Iterations, t_{max}	5000	500	500
Runtime	0.57 h	84.63 s	131.18 h
Normalized Speed	–	×5580	1

Conclusion

iVAMS:
- is a circuit-level modeling framework.
- creates efficient models that bridge different abstraction levels of AMS designs
- is compatible with optimization algorithms

Future research includes yield-estimation