

Polynomial Metamodel Integrated Verilog-AMS for Memristor-Based Mixed-Signal System Design

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Abstract—This paper proposes a two-level framework for memristor based mixed-signal design exploration. First, a Verilog-A memristor model is proposed which is not source-type dependent and has advantages over existing SPICE memristor models. It includes the threshold-type behavior and nonlinear dynamics while retaining memristor parameters that are useful for circuit design. Second, a POLynomial Metamodel integrated Verilog-AMS (Verilog-AMS-POM) is proposed to enable fast circuit-accurate system-level design space exploration of such circuits. The metamodeling technique is proposed to assist their design, modeling, and higher-level integration. A memristor based programmable Schmitt trigger oscillator is presented as a case study. Polynomial metamodels are created to facilitate the analysis and verification of the programmable oscillator. The coefficients of determination of the proposed metamodels demonstrate excellent fidelity. Verilog-AMS-POM simulation achieves over 30,000× speedup compared to SPICE simulations.

I. INTRODUCTION

Many novel memristor based integrated circuits and nanoelectronic systems have emerged [1]–[3]. As in any circuit, memristor based integrated circuit design requires proper device and circuit models. For system-level integration of such circuit blocks, efficient block-level representations with reasonable accuracy are necessary for high-level design space exploration. This paper proposes a two-level framework to support memristor based circuit design. First a Verilog-A memristor model is presented. It includes the memristor threshold-type behavior and nonlinear dynamics while retaining the parameters that are useful for circuit design. Second, POLynomial integrated Verilog-AMS (Verilog-AMS-POM) is proposed to support fast circuit-accurate system-level design space exploration. Verilog-AMS-POM embeds polynomial metamodels into a Verilog-AMS module to form an efficient and parametric memristor based circuit block representation. A programmable memristor oscillator design is proposed as a case study. The programming scheme proposed in our paper does not require extra capacitors or negative and high voltages. Metamodels are used for oscillator circuit model creation and design analysis.

There have been increasing research interest on designing digital as well analog systems with memristors as core circuit elements [1], [4]. The use of memristors for digital systems is at a very early stage and representing ON and OFF for digital systems with High-Resistance and Low-Resistance of memristor needs more research. In analog systems, memristors are employed to enable circuit programmability.

The **novel contributions** of this paper are summarized as:

- 1) A Verilog-A model which includes the threshold and nonlinear dopant drift for titanium dioxide (TiO_2) thin-film memristors is presented.
- 2) A memristor programmable Schmitt trigger oscillator design and a programming scheme are proposed.
- 3) Polynomial metamodels for the proposed memristor-based programmable oscillator are presented for fast simulation.
- 4) A Verilog-AMS model for the programmable oscillator embedding the polynomial metamodels.

The rest of this paper is organized as follows: Section II presents the proposed memristor device model in Verilog-A. Section III describes a memristor based programmable oscillator design. Section IV presents the polynomial metamodels for the programmable oscillator. Section V concludes the paper.

II. VERILOG-A DEVICE-LEVEL MEMRISTOR MODEL

Several models have been proposed to address the highly nonlinear dynamics of memristors [5], [6]. The coupled variable-resistor model of a titanium dioxide (TiO_2) thin film memristor is of the following form [7]:

$$V_M = [R_{on}x + R_{off}(1 - x)]I_M, \quad (1)$$

$$\frac{dx}{dt} = \mu_v \left(\frac{R_{on}}{D^2} \right) I_M, \quad (2)$$

where $x \in [0, 1]$ is an internal state variable, μ_v is the dopant mobility, and D is the semiconductor film thickness. This model does not include the threshold-type behavior observed in fabricated devices [8]. One of the major limitations of the memristor modeling approach arises from its boundary conditions. When the value of the state variable x is pushed to its boundaries (0 or 1) by an external source, this value should stay unchanged (0 or 1) until the applied voltage/current changes its polarity. A window function may prevent the state variable from returning from its boundaries even after the polarity of the applied source has changed [6]. This issue is termed as *hard-switching* or *terminal-state* problem [6]. Moreover, it appears that the nonlinearity generated by the window function does not conform to the characteristics of the available fabricated device. Non-inclusion of an explicit threshold further limits the use of existing models.

A. The Proposed Memristor Model

We present a coupled variable-resistor model to take into account the threshold-type behavior. The modification is based on the exponential dopant drift model [9] for thin-film memristors where the drift velocity was characterized using the following expression:

$$v \approx \begin{cases} \mu_v E & \text{if } E \ll E_o, \\ \mu_v E_o e^{E/E_o} & \text{if } E \sim E_o, \end{cases} \quad (3)$$

where E is the electric field across the device and E_o is the characteristic high field that introduces the nonlinear effect. A variable-mobility model was proposed in [1] for μ_v in Eqn. (2) to incorporate the memristor threshold based on this nonlinear drift equation. μ_v , however, should be kept the same and the rest of Eqn. (2) should be modified. Assuming a uniform field, the memristor threshold V_o is related to E_o through $E_o = V_o/D$. There can be two threshold values, V_p and V_n , for different polarities of V_M . Using Eqn. (3), Eqn. (2) can be extended to the following model:

$$\frac{dx}{dt} = \begin{cases} \mu_v \frac{V_p}{D^2} e^{\frac{R_{on}}{V_p} I_M} & \text{if } V_M \geq V_p, \\ \mu_v \frac{V_n}{D^2} e^{\frac{R_{on}}{V_n} I_M} & \text{if } V_M \leq V_n, \\ \mu_v \frac{R_{on}}{D^2} I_M & \text{otherwise.} \end{cases} \quad (4)$$

The $I - V$ relation in Eqn. (1) is still valid. This way the memristor nonlinear dynamic is included in the new model while parameters such as D , R_{on} , R_{off} are kept.

B. Proposed Verilog-A memristor model

SPICE memristor models are source-type dependent, i.e. voltage-controlled based and cannot be driven by a current source and vice versa. This restricts their application. In contrast, a Verilog-A implementation is not restricted and is more suitable for mixed-signal simulation. The memristor device-level model implementation in this paper is based on the coupled variable-resistor relation from Eqn. (1) and the memristor nonlinear dynamic described in Eqn. (4). They can be described in physical modeling languages such as Verilog-A and MATLAB Simulink/Simscape. Fig. 1 shows the time-domain simulation for both implementations. A Verilog-A model used in this paper for circuit-level simulation. The memristor dynamic is implemented in integral form. A variable `integ` has been used to control the integral operation such that the boundary conditions are satisfied and the hard-switching problem is avoided.

III. MEMRISTOR-BASED PROGRAMMABLE OSCILLATOR

A. Programmable Schmitt trigger oscillator

Schmitt trigger oscillators are used in many applications such as capacitive and inductive sensing [10] and pressure sensing [11]. They are also used in implantable devices, e.g., in [12]. An investigation of three types of digitally controlled oscillators—differential ring oscillators, Source-coupled multivibrator, and Schmitt trigger oscillator—for a phase-locked loop was conducted in [13]. It demonstrated that the Schmitt

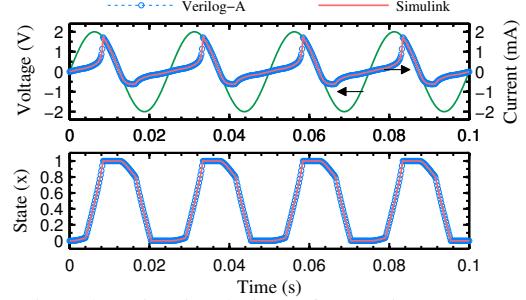


Fig. 1: Time-domain simulation of memristor. A 2-V, 40-Hz sine wave is applied to a memristor: $R_{on} = 1 \text{ k}\Omega$, $R_{off} = 10 \text{ k}\Omega$, $\mu_v = 10^{-14} \text{ m}^2/\text{s}/\text{V}$, $V_p = 1.7 \text{ V}$, $V_n = -1.7 \text{ V}$.

trigger oscillator exhibits the least phase noise. The Schmitt trigger oscillator design shown in Fig. 2a is adopted in the current paper. Its oscillation frequency (f_o) is determined by the resistance (R), capacitance (C), and the Schmitt trigger hysteresis. Replacing the resistor with a memristor R_M , as shown in Fig. 2b results in a programmable oscillator. The extra circuitry is needed for programming the memristor.

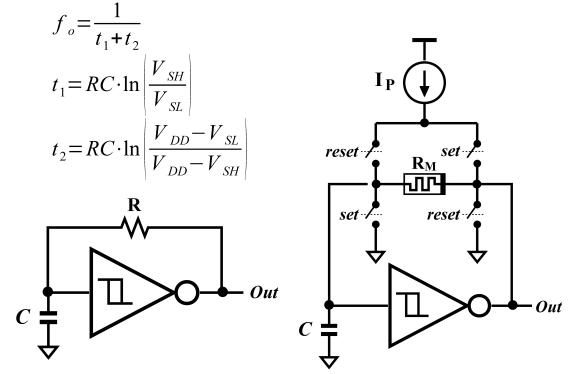


Fig. 2: The conventional Schmitt trigger oscillator and the proposed one with added programmability.

The proposed oscillator is shown in Fig. 2b. Four switches and a programming current source I_p are used for programming. The programming process consists of two phases: (1) **Reset**. The reset switches are closed and the set switches are open. Constant current I_p flows through the memristor to set the state (memristance) to 1 (R_{on}). (2) **Set**. The reset switches are open and the set switches are closed. Constant current I_p flows through the memristor reversely compared to the reset phase until the desired memristance is reached. During normal operation, all switches are open. The programmed state mainly depends on the time, t_{set} , during which the control voltage, V_{set} , to the set switches is high. An example is shown in Fig. 3 where $t_{set} = 80 \text{ ms}$ and the memristor state is programmed to $x = 0.1$.

B. Memristor based oscillator design

The hybrid CMOS-memristor technology based memristor-programmable Schmitt trigger oscillator is shown in Fig. 4. We have used a 90 nm CMOS process with 1-V power supply in this paper. All transistors have a length (L) of 100 nm.

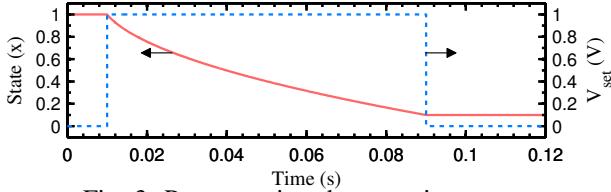


Fig. 3: Programming the memristor state.

The width (W) for transistors M1–M4 for generating I_p is $4 \mu\text{m}$. Transistors M13 and M14 for creating hysteresis have a W of $2.5 \mu\text{m}$ and $1.5 \mu\text{m}$, respectively. For all other PMOS transistors, $W = 2 \mu\text{m}$; for all other NMOS transistors, $W = 1 \mu\text{m}$. The programming current I_p is set to $100 \mu\text{A}$ and $C = 200 \text{ fF}$. The memristor R_{on} and R_{off} are $10 \text{ k}\Omega$ and $100 \text{ k}\Omega$, respectively. Table I lists the resultant characteristics of the memristor based programmable oscillator at three states.

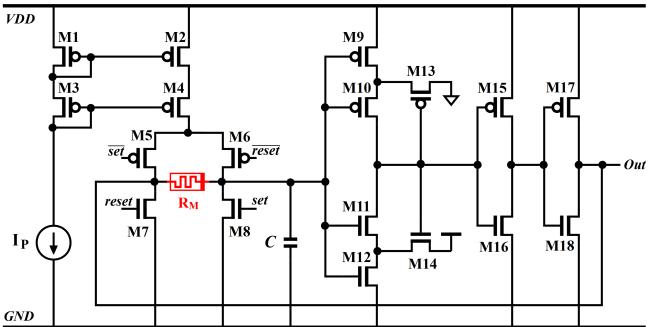


Fig. 4: Memristor based programmable oscillator design.

TABLE I: Oscillator Characteristics

Memristor based Programmable Oscillator			
$R_M(x)$	Frequency	Jitter	Power
$100 \text{ k}\Omega (0)$	34.4915 MHz	536 ps	$130.4 \mu\text{W}$
$55 \text{ k}\Omega (0.5)$	59.662 MHz	323 ps	$133.9 \mu\text{W}$
$10 \text{ k}\Omega (1)$	251.459 MHz	69 ps	$161.2 \mu\text{W}$
Schmitt Trigger Oscillator			
R	Frequency	Jitter	Power
$100 \text{ k}\Omega$	34.4887 MHz	615 ps	$130.4 \mu\text{W}$
$55 \text{ k}\Omega$	59.6531 MHz	257 ps	$133.9 \mu\text{W}$
$10 \text{ k}\Omega$	251.454 MHz	83 ps	$161.2 \mu\text{W}$

It can be seen from Table I that replacing the regular resistor with the memristor does not lead to noticeable increase in power consumption. Device noise is the major source of the simulated jitter, although the device noise of the memristor was not included in the simulations. The current flow through the memristor can cause slight fluctuation on the memristor state. This temporal variation produces additional jitter to the programmable oscillator. For a large resistance value, $R_M = R = 100 \text{ k}\Omega$, the resistor thermal noise is dominant and thus the conventional Schmitt trigger oscillator exhibits more jitter. For $R_M = R = 55 \text{ k}\Omega$, the resistor thermal noise is reduced and the memristor state variation becomes a larger jitter source. For $R_M = R = 10 \text{ k}\Omega$, the resistor thermal noise is further reduced. However, the jitter contributed by the memristor state variation is reduced by a greater amount since the memristor state is insensitive to high-frequency

signals. Therefore the programmable oscillator exhibits less jitter than a CMOS only realization. The jitter exhibited by both oscillators is expected to be comparable if the memristor device noise is added to the simulation.

IV. METAMODELS FOR THE MEMRISTOR BASED PROGRAMMABLE OSCILLATOR

Metamodels are surrogate models that attempt to approximate the characteristic response surfaces of systems. A polynomial metamodel (POM) has the following form [14]:

$$f_{POM}(\mathbf{v}) = \sum_{i=0}^{N_B-1} \beta_i \prod_{j=0}^{N_D-1} v_j^{p_{ij}}, \quad (5)$$

where $\mathbf{v} = \{v_1, v_2, \dots, v_{N_D}\}$ are circuit design variables, N_B is the number of basis functions of this POM, β_i is the coefficient of the i th basis function, p_{ij} is the power term for the j th design variable in the i th basis function, and N_D is the number of design variables. The signal propagation delay of a simple RC circuit can be approximated as $t_d = 0.7RC$. Using metamodeling, a 1st order POM describes the delay as:

$$t_{d,POM}(R, C) = \beta_0 R^0 C^0 + \beta_1 R^0 C^1 + \beta_2 R^1 C^0 + \beta_3 R^1 C^1. \quad (6)$$

It has two design variables ($N_D = 2$) and four basis functions ($N_B = 4$). The coefficients β_i are determined by sampling the circuit design space and then fitting the POM to the sampled responses by tuning the coefficient values.

TABLE II: Variables and their ranges for $x_{POM}(\mathbf{v})$.

Variable	Minimum	Maximum	Device
t_{set}	0 ms	100 ms	-
I_p	$80 \mu\text{A}$	$120 \mu\text{A}$	-
R_{on}	$8 \text{ k}\Omega$	$12 \text{ k}\Omega$	R_M
R_{off}	$80 \text{ k}\Omega$	$120 \text{ k}\Omega$	R_M
W_P	$1.6 \mu\text{m}$	$2.4 \mu\text{m}$	M9, M10
W_N	$0.8 \mu\text{m}$	$1.2 \mu\text{m}$	M11, M12
$x_{POM}(\mathbf{v}) = x_{POM}(t_{set}, I_p, R_{on}, R_{off}, W_P, W_N)$			

In this paper, two POMs were created. The first POM, $x_{POM}(\mathbf{v})$, approximates the response surface of the memristor state x . A 2nd order POM was created from 500 SPICE-simulated samples with Latin hypercube sampling (LHS). The six included variables ($N_D = 6$) and their ranges for this POM are listed in Table II. To visualize the effect of t_{set} and I_p on memristor state setting, a response surface of the programmed state x as a function of t_{set} and I_p is constructed in Fig. 5 using $x_{POM}(\mathbf{v})$ while other variables are fixed. The same response surface constructed using SPICE simulations is also shown as the true response surface for comparison. It is also worth mentioning that although only 6 variables were created, the circuit nonidealities such as the parasitics of the programming switches M5–M8 have been included in the POM during the LHS process through SPICE simulation. Hence, it is feasible to use a POM to improve the programming accuracy. This can be done by using a POM, $t_{set,POM}(x, I_p, R_{on}, R_{off}, W_N, W_N)$, to compute the required value for t_{set} for a given x . The computed t_{set} value automatically includes the compensation

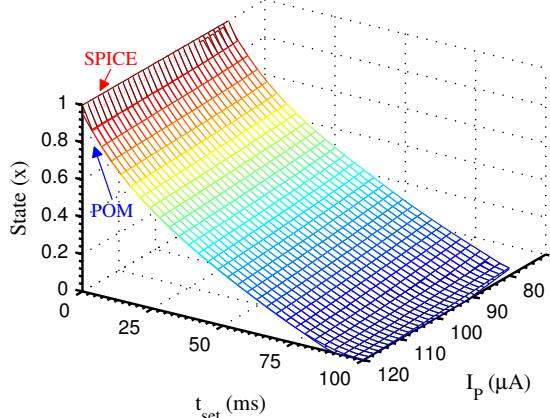


Fig. 5: Memristor state response surface as a function of the programming current and the set time.

for the circuit nonidealities, $t_{set,POM}(\mathbf{v})$ can be coded into the programming unit so the memristor state is software-defined.

The second POM, $f_{o,POM}(\mathbf{v})$, approximates the response surface of the oscillator output frequency but is not shown here due to space restrictions. This POM is useful for fast estimation of f_o variation due to various effects and for construction of a model for high-level design simulation. The 500 simulation samples in the first POM were re-used to create a 4th order $f_{o,POM}(\mathbf{v})$. For a 20 % variation in W_P and W_N , the output frequency f_o can vary from 54 MHz to 66 MHz.

In order to assess the POM accuracy, a verification set of 500 SPICE-simulated samples were generated. The values predicted by the POMs are compared with the verification samples. Metrics adopted to assess the POM accuracy include: coefficient of determination (R^2), Relative maximum absolute error (RMAE), and RMSE.

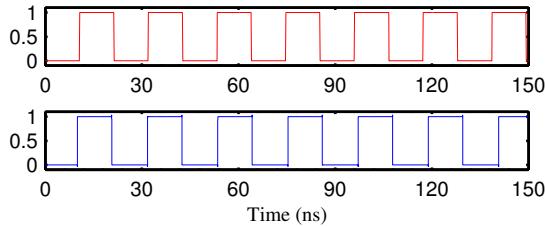


Fig. 6: Transient analyses of the memristor based oscillator using Verilog-AMS-POM (top) and SPICE netlist (bottom).

In order to evaluate the speedup achieved by employing Verilog-AMS-POM, the runtimes for the Verilog-AMS-POM and SPICE simulations with various memristor state variable values are compared in Table III. For each simulation run, the simulation time was set to be equal to 1000 oscillation cycles. Over $30000\times$ speedups were observed. The oscillator Verilog-AMS-POM bypasses the complexity of the memristor and the nanometer transistor models while including the circuit nonidealities through polynomial metamodels. With the parameterization inherited in the metamodels, the Verilog-AMS-POM is not only suited for verification tasks but also for system-level design optimization. Verilog-AMS-POM in particular can make the mixed-signal system simulation, verification, and optimization faster than existing design methods. This in turn

will reduce the design cycle time, design cost and improve chip yield.

TABLE III: Runtime of memristor-based oscillator.

x	Verilog-AMS-POM	SPICE	Speedup
0.1	10.72 ms	360.31 s	$33704\times$
0.3	11.60 ms	335.96 s	$28962\times$
0.5	11.77 ms	349.10 s	$29660\times$
0.7	11.73 ms	348.08 s	$29674\times$
0.9	10.91 ms	355.97 s	$32628\times$

V. CONCLUSIONS

A memristor device model that relates the memristor physical operation and its circuit-oriented parameters has been presented. This model is implemented in Verilog-A for higher efficiency and flexibility. Polynomial metamodels have been created for the proposed memristor based programmable oscillator. They are accurate and efficient tools for analyzing memristor based circuits. Verilog-AMS-POM construction of the memristor based oscillator has been demonstrated. Verilog-AMS-POM boosts the simulation speed of the memristor based circuit. It is thus a prominent candidate to support system-level integration, verification, and design exploration.

REFERENCES

- [1] G. S. Rose, J. Rajendran, H. Manem, R. Karri, and R. E. Pino, "Leveraging memristive systems in the construction of digital logic circuits," *Proc. IEEE*, vol. 100, no. 6, pp. 2033–2049, 2012.
- [2] S. Shin, K. Kim, and S. Kang, "Memristor applications for programmable analog ICs," *Nanotechnology, IEEE Transactions on*, vol. 10, no. 2, pp. 266–274, 2011.
- [3] Y. V. Pershin and M. Di Ventra, "Practical Approach to Programmable Analog Circuits With Memristors," *IEEE Trans. Circuits Syst. I*, vol. 57, no. 8, pp. 1857–1864, 2010.
- [4] Y. Shang, W. Fei, and H. Yu, "Analysis and Modeling of Internal State Variables for Dynamic Effects of Nonvolatile Memory Devices," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 9, pp. 1906–1918, September 2012.
- [5] K. Eshraghian, O. Kavehei, K.-R. Cho, J. Chappell, A. Iqbal, S. Al-Sarawi, and D. Abbott, "Memristive device fundamentals and modeling: Applications to circuits and systems simulation," *Proceedings of the IEEE*, vol. 100, no. 6, pp. 1991–2007, June 2012.
- [6] T. Prodromakis, B. Peh, C. Papavassiliou, and C. Toumazou, "A versatile memristor model with nonlinear dopant kinetics," *Electron Devices, IEEE Transactions on*, vol. 58, no. 9, pp. 3099–3105, 2011.
- [7] D. Strukov, G. Snider, D. Stewart, and R. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, 2008.
- [8] S. Jo, T. Chang, I. Ebong, B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems," *Nano letters*, vol. 10, no. 4, pp. 1297–1301, 2010.
- [9] D. Strukov and R. Williams, "Exponential ionic drift: fast switching and low volatility of thin-film memristors," *Applied Physics A: Materials Science & Processing*, vol. 94, no. 3, pp. 515–519, 2009.
- [10] S. Engelberg, H. Hazout, and J. Hirshowitz, "A capacitive-sensing based simple serial mouse," *Instrumentation & Measurement Magazine, IEEE*, vol. 13, no. 2, pp. 32–36, 2010.
- [11] M. Moser and H. Zangl, "Temperature and pressure monitoring of a whipped cream device," in *IEEE Sensors*, 2009, pp. 683–686.
- [12] K. Zhu, S. Islam, J. Holloman, and S. Yuan, "A low-power dual-modulus injection-locked frequency divider for medical implants," in *Radio and Wireless Symposium (RWS), 2011 IEEE*. IEEE, 2011, pp. 414–417.
- [13] H. Unterlassinger, M. Flatscher, T. Herndl, J. Jongsma, and W. Pribyl, "Design of a digitally controlled oscillator for a Delta-Sigma phase-locked loop in a $0.13\text{ }\mu\text{m}$ CMOS-process," *e & i Elektrotechnik und Informationstechnik*, vol. 127, pp. 86–90, 2010.
- [14] G. Zheng, S. P. Mohanty, and E. Kougiannos, "Metamodel-assisted fast and accurate optimization of an op-amp for biomedical applications," in *Proc. IEEE Computer Society Annual Symp. VLSI*, 2012, pp. 273–278.