

## Exploring Kriging for Fast and Accurate Design Optimization of Nanoscale Analog Circuits

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The design complexity of modern electronics devices continues to increase exponentially partially driven by consumer demand for more powerful, yet smaller devices. Aggressive scaling of technology allows for the possibility of more subcircuit system components to be integrated on a single chip. The design synthesis of such Analog/Mixed Signal Systems-on-a-Chip (AMSSoCs) however constitutes a significant challenge for designers. With increased circuit components, the numbers of parameters that must be considered in the design space exploration to meet design specifications become an undue burden to the designers. A more prominent issue in designs deep in the nanometer range is including the effects of process variation early on in the design process and mitigating other issues such as power density and subthreshold leaking. Conventional synthesis methods for optimal sizing which use time and computationally expensive computer SPICE simulations for exhaustive and accurate exploration becomes infeasible with exponentially increasing design space. Alternative methods which aim to reduce the burden of size synthesis, while producing optimal and accurate results include metamodeling design. Metamodeling techniques abstracts the expensive simulations times by providing designers fast access to the design space with an approximation of the behavioral response of the circuit to the most sensitive design parameters in the form of a mathematical function. While current metamodeling techniques have been explored and have been reported to significantly improve simulation time and efficiency, they are still unable to model the effects of process variation early on in the design process. Geostatistical Kriging based techniques use effective weighting techniques that utilize the correlation effects between parameters and can be modeled to capture process variation effects. This work explores geostatistical Kriging techniques for the fast and accurate design optimization of nanoscale AMSSoCs. An illustration with a 180nm PLL designs shows an improvement in 79 % power dissipation while reducing the simulation time by about 25X.