

ILP Models for Simultaneous Energy and Transient Power Minimization during Behavioral Synthesis

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In low-power design for battery driven portable applications, the reduction of peak power, peak power differential, cycle difference power, average power and energy are equally important. These are different forms of dynamic power dissipation of a CMOS circuit, which is predominant compared to static power dissipation for higher switching activity. The peak power, the cycle difference power, and the peak power differential drive the transient characteristic of a CMOS circuit. In this paper, we propose an ILP-based framework for the reduction of energy and transient power through datapath scheduling during behavioral synthesis. A new metric called “modified cycle power function” (CPF*) is defined that captures the above power characteristics and facilitates integer linear programming formulations. The ILP-based datapath scheduling schemes with CPF* as objective function are developed assuming three modes of datapath operation, such as, single supply voltage and single frequency (SVSF), multiple supply voltages and dynamic frequency clocking (MVDFC), and multiple supply voltages and multicycling (MVMC). We conducted experiments on selected high-level synthesis benchmark circuits for various resource constraints and estimated power, energy and energy delay product for each of them. Experimental results show that significant reductions in power, energy and energy delay product can be obtained.

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1. INTRODUCTION

The proliferation of portable systems and mobile computing platforms has increased the need for the design of low power consuming integrated circuits. The increase in chip density and clock frequencies due to technology advances has made low power design a critical issue. Low power design is further driven by several other factors such as thermal considerations and environmental concerns. In battery driven portable systems, the peak power, cycle difference power, peak power differential, average power and energy are equally critical design constraints.

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The reduction of peak power consumption is essential due to following reasons [Singh et al. 1995] : (i) to maintain supply voltage levels, (ii) to increase reliability, (iii) to use smaller heat sinks, and (iv) to make packaging cheaper. The peak power of a circuit is the maximum power consumption of the circuit at any instance during its execution. High peak power can affect the supply voltage levels. The large current flow causes high IR drop in the power line, which leads to the reduction of the supply voltage levels at different parts of the circuit. High current flow can reduce reliability because of hot electron effects and high current density. The hot electrons may lead to electrostatic discharge and runaway current failures, and high current density can cause electromigration failures. It has been observed that the mean time to failure (MTF) of a CMOS circuit is inversely proportional to the current density (or power density). Large power dissipation results in the need for expensive heat dissipation mechanisms to maintain the operating temperatures of the ICs within their tolerance limits.

The cycle difference power and the peak power differential need to be reduced for the following reasons : (i) to reduce power supply noise, (ii) to reduce cross talk and electromagnetic noise, (iii) to increase battery efficiency and (iv) to increase reliability. Power fluctuation leads to larger $\frac{di}{dt}$ causing power supply noise, (similar to IR drop), because of self inductance of power supply lines. Crosstalk is the noise voltage induced in signal line due to the switching in the adjacent signal lines [Singh et al. 1995]. The voltage induced by the mutual inductance is expressed as $L\frac{di}{dt}$ and that induced by the mutual capacitance as $C\frac{dv}{dt}$. If the power fluctuation is high, then large $\frac{di}{dt}$ and $\frac{dv}{dt}$ can introduce significant noise in the signal lines. As the power fluctuation increases, it reduces the electrochemical conversion and hence there is decrease in battery life. High current peaks (power fluctuation) in short time spans can cause high heat dissipation in a localised area of silicon die which may lead to permanent failure of the integrated circuit.

Energy and average power reduction is essential for the following reasons : (i) to increase battery life time, (ii) to enhance noise margin, (iii) to reduce cooling and energy costs, (iv) to reduce use of natural resources, and (v) to increase system reliability. The battery life time is determined by the Ah (ampere hour) rating of the battery. If the average power (and/or energy) consumption is high, this will lead to reduced battery life time. The reduction of average power is essential to enhance noise margin (to decrease functional failure). The cost of packaging and cooling is determined by average current flow and hence, the average power and energy. Due to the proliferation of the use of computers, the large amount of energy consumption leads to the need for more power generation, which could lead to environmental concerns. In integrated circuits, if the average power consumption is high, the operating temperature of the chip will increase leading to failures. It is estimated that for each $10^\circ C$ increase in the operating temperature, the failure rates of the component is roughly doubled.

Power and energy reduction can be achieved at different levels, such as the architecture, algorithm, behavioral, register-transfer, logic and transistor levels. In this work, we focus on low power datapath scheduling at the behavioral level. We propose ILP based schemes for energy and transient power minimization. The first scheme uses multiple supply voltages and dynamic frequency clocking (MVDFC) and the second scheme is based on the use of multiple supply voltages and multicycling (MVMC). We also consider traditional scheduling using single supply voltage and single frequency (SVSF) to facilitate comparison among all the schemes. In multiple supply voltage scheme, the functional units can

be operated at different supply voltages. The energy reduction due to the use of multiple voltages is often accompanied by the degradation of performance because of the increase in critical path delay. This degradation in performance can be compensated by the use of techniques such as dynamic frequency clocking [Mohanty and Ranganathan 2003b; Mohanty et al. 2002], multicycling and chaining [Park and Choi 2001], and variable latency components [Benini et al. 1998; Benini et al. 1999]. In the case of multicycling, an operation is scheduled in more than one consecutive control step and in addition, each control step is of equal length. In dynamic frequency clocking, the clock frequency may be varied on-the-fly depending on the computations being performed. In this case, an operation is scheduled in a single control step and the control steps of a schedule may vary in length.

The contributions of this paper are multifold:

- a method that facilitates the simultaneous reduction of several dynamic power components such as average power, peak power, cycle difference power, peak power differential, and energy.
- a new cycle power function called “modified cycle power function CPF*” is defined so as to capture the different dynamic power components and to facilitate integer linear programming (ILP) formulation.
- the definition of CPF* is extended for three different modes of datapath operations and denoted as, CPF-SVSF* for single voltage - single frequency, CPF-MVDFC* for multiple voltages - dynamic frequency, and CPF-MVMC* for multiple voltages - multicycling, respectively.
- the exploration of design alternatives due to the combined use of dynamic frequency clocking and multiple supply voltages.
- ILP formulations based on transforming the nonlinear objective function CPF* to linear frameworks and under different constraints.
- a set of datapath scheduling algorithms are developed for different modes of operations

The rest of the paper is organized as follows. The various related works are briefly visited in the next section. The formulation of the the modified cycle power function CPF* is presented followed by the issues in transforming the function into a linear objective function. The ILP formulations and the datapath scheduling algorithms are described in Sections 5 and 6, the experimental results in Section 7 followed by the conclusions.

2. RELATED WORK

Very few works address the reduction of peak power and peak power differential during behavioral synthesis. On the other hand, quite many works have appeared in the literature addressing average power and energy reduction during datapath synthesis. We will briefly discuss the above works followed by those related to dynamic frequency clocking.

In the work reported in [Martin and Knight 1996a], the peak power reduction is achieved through simultaneous assignment and scheduling. Specifically, the simultaneous use of SPICE and behavioral synthesis tools is described. Genetic algorithms are used for optimization of average and peak power. In [Shiue 2000], ILP based scheduling and force directed scheduling are proposed to minimize peak power under latency constraints. ILP based models to minimize both peak power and peak area are proposed in [Shiue and Chakrabarti 2000a] for latency constraint scheduling. In [Shiue et al. 2000], the authors describe a time constrained scheduling algorithm for real time systems using a modified ILP

model that minimizes both peak power and number of resources. In [Raghunathan et al. 2001], the authors propose the use of data monitor operations for simultaneous peak power reduction and peak power differential. In [Mohanty and Ranganathan 2003a], a heuristic based scheme is proposed that minimizes peak power, peak power differential, average power and energy. In [Mohanty et al. 2003], ILP based datapath scheduling schemes are described for peak power minimization under resource constraints.

Several research works, such as, [Johnson and Roy 1997; Chang and Pedram 1997; Shiue and Chakrabarti 2000b] have used multiple supply voltage method for energy reduction during datapath synthesis. The above scheduling techniques consider various concepts such as multiple supply voltages, voltage scaling, capacitance reduction, and switching activity reduction for minimizing either total energy or average power, but not both at the same time. However, these works have not considered dynamic frequency clocking or transient power reduction.

Many works considering the use of variable latency, dynamic frequency and multiple frequencies have appeared in the literature. The usage of “telescopic” units to improve the throughput of digital systems is introduced in [Benini et al. 1998; Benini et al. 1999]. The telescopic units complete execution in a variable number of clock cycles depending on the input data. The concept of dynamic frequency clocking is introduced and a SIMD linear array image processor design is discussed in [Ranganathan et al. 1996]. A low power design using multiple clocking scheme is presented in [Papachristou et al. 1999]. The usage of frequency scaling in an MPEG2 decoder design is described in [Kim and Chae 1996]. A time constrained heuristic scheduling algorithm is discussed in [Mohanty et al. 2002] that uses both frequency and voltage scaling. In [Mohanty and Ranganathan 2003b], heuristic algorithms are proposed for energy minimization using multiple voltages and dynamic frequency clocking during datapath scheduling. Several system-level approaches [Burd et al. 2000; Hsu et al. 2000; Pouwelse et al. 2001] have been investigated towards reducing power consumption in both general purpose and special purpose processors using simultaneous voltage and frequency scaling.

Most works discussed above address either average power, energy or peak power, but not all the forms of dynamic power consumption together. In this paper, we describe an ILP-based framework for the simultaneous minimization of energy, average power, peak power, cycle difference power, and peak power differential. A parameter called *modified cycle power function* (CPF*) is defined as an equally weighted sum of the normalized mean cycle power and the normalized mean cycle difference power. Minimizing CPF* using multiple supply voltages and dynamic frequency clocking or multicycling results in the reduction of both energy and transient power. The cycle difference power is modeled as the absolute deviation from the mean cycle power. The switching activity of the functional units is characterized through simulations and incorporated into the model. The datapath scheduling algorithms to minimize the CPF* using dynamic frequency clocking or multicycling and multiple supply voltages are proposed. The algorithm assumes different types and numbers of resources (such as, multipliers and ALUs) at different operating voltages and the number of allowable operating frequencies as resource constraints and attempts to minimize CPF*. The scheduling algorithm generates a parameter called *cycle frequency index*, denoted as cfi_c for control step c to be stored in the controller. This parameter serves as the clock dividing factor for the *dynamic clocking unit* (DCU) which is used to generate different frequencies on the fly.

3. MODIFIED CYCLE POWER FUNCTION

In this section, we define a metric called modified cycle power function (CPF*) that captures the average and transient power characteristics of a datapath circuit. It may be noted that though CPF* captures the average and transient power characteristics, its minimization using multiple voltages leads to reduction of energy as well. Moreover, while defining the CPF* which is a nonlinear function, we take into the account the fact that the complexity ILP formulations to be used for its minimization is reduced. We assume that the datapath is represented as a sequencing data flow graph (DFG). The definitions and notations needed for the model are given in Table I.

Table I. Notations and Definitions used in CPF* Modeling

N	: total number of control steps in the DFG
O	: total number of operations in the DFG
c	: a control step or a clock cycle in DFG
o_i	: any operation, where $1 \leq i \leq O$,
P_c	: the total power consumption of all functional units active in control step c (cycle power consumption)
P_{peak}	: peak power consumption for the DFG = $(\max(P_c)_{\forall c})$
P	: mean power consumption of the DFG (average P_c over all control steps)
P_{norm}	: normalised mean power consumption of the DFG
DP_c	: cycle difference power (for cycle c ; a measure of cycle power fluctuation)
DP_{peak}	: peak differential power consumption for the DFG = $(\max(DP_c)_{\forall c})$
DP	: mean of the cycle difference powers for all control steps in DFG
DP_{norm}	: normalised mean of the cycle difference powers for all steps in DFG
CPF*	: modified cycle power function
$FU_{k,v}$: any functional unit of type k operating at voltage level v
FU_i	: any functional unit $FU_{k,v}$ needed by o_i for its execution ($o_i \in FU_{k,v}$)
$FU_{i,c}$: any functional unit FU_i active in control step c
R_c	: total number of functional units active in step c (same as the number of operations scheduled in c)
$\alpha_{i,c}$: switching activity of resource $FU_{i,c}$
$V_{i,c}$: operating voltage of resource $FU_{i,c}$
$C_{i,c}$: load capacitance of resource $FU_{i,c}$
f_c	: frequency of control step c
f_{clk}	: operating clock frequency for MVMC or SVSF scheme
V	: operating supply voltage for MVMC or SVSF scheme

We would like to define CPF* as a multicost objective function such that minimizing it should facilitate the minimization of the multiple objectives, the different dynamic power components. The simultaneous optimization of different inter-related parameters is difficult. In general, if we have to optimize four parameters, say, a , b , c and d , the simplest approach is to form the objective function as, $\text{obj}_1 = a + b + c + d$. This function will not be effective for all parameters if the quantitative differences among the values of the parameters are large. So, one way of handling this is to use different weighting functions, and reformulate the objective function as, $\text{obj}_2 = \alpha * a + \beta * b + \gamma * c + \theta * d$, where the weighting functions can be used for tuning the objective function. In this scenario, there are eight different parameters to be handled. Another way of forming the objective function is $\text{obj}_3 = \frac{a}{b} + \frac{c}{d}$. In this case, we need to deal with only four parameters, but the question arises as to how to handle such a fractional function? Say, we want to minimize

$obj = \frac{x}{y}$, then minimization of both x and y will not minimize obj . We need to fix y and minimize obj , which in turn will minimize x . In other words, we can place a constraint on y and minimize $(obj + y)$ to achieve the simultaneous minimization of x and y . Of course, in such a scenario minimization of y is not optimal. In the proposed CPF*, a fractional form objective function, we place the denominator as a constraint and minimize the term. Moreover, the four parameters of CPF*, are P , P_{peak} , DP , and DP_{peak} . Thus, CPF* captures the average and transient characteristics of a datapath circuit. Its minimization using ILP results in optimal minimization of average power and cycle difference power, and suboptimal minimization of peak power and peak power differential. Further, its minimization in the multiple supply voltage and dynamic frequency framework results in the minimization of energy and energy delay product as well.

In general, for a set (x_1, x_2, \dots, x_n) of n observations from a given distribution, the sample mean (which is an unbiased estimator for the population mean, μ) is $m = \frac{1}{n} \sum_{i=1}^n x_i$. The absolute deviation of the observations is defined as $\Delta x_i = |x_i - m|$. The mean deviation of the observations is given by $MD = \frac{1}{n} \sum_{i=1}^n |x_i - m|$. In a datapath circuit represented as a DFG, the cycle power consumption values are represented as (P_1, P_2, \dots, P_N) for N possible control steps, in other words, P_c corresponds to x_i . The mean cycle power P is an unbiased estimate of the average power consumption of the DFG, is effectively the sample mean of N observations. Similarly, the cycle difference power DP_c is the absolute deviation of cycle power P_c from the mean cycle power P (corresponds to Δx_i). Finally, the mean cycle difference power DP is modeled as mean deviation of the cycle power P_c (which is in fact the MD in statistical sense).

The power consumption for any control step c is P_c . This is the total power consumption of all the functional units active in control step c and also includes the power consumption of the level converters. If a current resource is driven by a resource operating at lower voltage, then level converters are needed as additional resources operating in the current cycle. The peak power consumption of the DFG, P_{peak} is the maximum power consumption over all the control steps or clock cycles. The mean cycle power (P) which is an unbiased estimate of the average power consumption of the DFG is the mean of P_c . The cycle difference power (DP_c) for any control step can be defined as the absolute deviation of the cycle power from the mean cycle power consumption of the DFG. This is a measure of the cycle power fluctuation of the DFG. The peak differential power (DP_{peak}), which characterises the maximum power fluctuation of DFG over all control steps is the maximum of DP_c over all control steps. The mean cycle difference power (DP) is calculated as sample mean of DP_c . This is a measure of the power spread or distribution of the cycle power over all control steps of the DFG. Based on the above discussion, we have the various definitions as follows.

$$\begin{aligned}
 P_{peak} &= \max(P_c)_{\forall c=1,2,\dots,N} \\
 P &= \frac{1}{N} \sum_{c=1}^N P_c \\
 DP_c &= |P - P_c| \\
 DP_{peak} &= \max(|P - P_c|)_{\forall c=1,2,\dots,N} \\
 DP &= \frac{1}{N} \sum_{c=1}^N DP_c
 \end{aligned} \tag{1}$$

Now, CPF^* can be defined as the sum of the following components: the normalized mean cycle power and the normalized mean cycle difference power. The normalized mean cycle power (P_{norm}) is the mean cycle power (P) normalized with the peak power consumption (P_{peak}) of the DFG. Similarly, the normalized mean cycle difference power (DP_{norm}) is the mean cycle difference power (DP), normalised with the peak differential power (DP_{peak}). Thus, CPF^* is a nonlinear fractional function $\frac{P}{P_{peak}} + \frac{DP}{DP_{peak}}$, with absolute function in numerator and denominator. We are aiming at formulating ILP-based models for its minimization, which will be of very large complexity for such a function. Particularly, the presence of two different forms of nonlinearity, such as absolute function and fraction form, and two different denominators make the ILP-formulation cumbersome. However, for a DFG representing a datapath circuit, we deal with optimization of positive power values, so we can simplify the function to certain extent to make ILP formulations easy. It is known that the denominator parameters, P_{peak} equals to $\max(P_c)_{\forall c}$ and the DP_{peak} equals to $\max(|P - P_c|)_{\forall c}$. In the DFG for a datapath circuit, P is an positive entity, and the worst case values of P_c is zero or P_{peak} , and the average power P is upper bounded by P_{peak} . So, the maximum possible value of $\max(|P - P_c|)_{\forall c}$ is P_{peak} ; in other words, DP_{peak} is upper bounded by P_{peak} . Thus, we can normalize DP with the peak power consumption P_{peak} instead of DP_{peak} to reduce the complexity of ILP formulation.

The modified cycle power function CPF^* that is modeled as an equally weighted sum of the normalized mean cycle power (P_{norm}) and the modified normalized mean cycle difference power (DP_{norm}) is given below.

$$\begin{aligned}
 CPF^*(P_{norm}, DP_{norm}) &= P_{norm} + DP_{norm} \\
 &= \frac{P}{P_{peak}} + \frac{DP}{P_{peak}} \\
 &= \frac{P+DP}{P_{peak}} \\
 &= \frac{\frac{1}{N} \sum_{c=1}^N P_c + \frac{1}{N} \sum_{c=1}^N |P - P_c|}{P_{peak}}
 \end{aligned} \tag{2}$$

It may be noted that P_{norm} and DP_{norm} are unitless quantities in the range [0,1]. Thus, CPF^* has a value in the range [0,2]. The above function (Eqn. 2) can serve as the objective function for low power datapath scheduling. *The minimization of this objective function using multiple supply voltages, dynamic frequency clocking and multicycling can reduce various forms of dynamic power, energy and energy delay product either optimally or suboptimally.* From Eqn. 2, we observe the following about CPF^* : it is a *non-linear* function having two nonlinearity, fractional form and absolute function, and has a single denominator.

The power consumption for any control step c is given by Eqn. 3 as follows.

$$P_c = \sum_{i=1}^{R_c} \alpha_{i,c} C_{i,c} V_{i,c}^2 f_c \tag{3}$$

This power models uses generic parameters, such as $\alpha_{i,c}$, $C_{i,c}$, $V_{i,c}$ and f_c . The model can accomodate both the look-up table based energy (power) models and energy (power) macro-models. The generic model can also help in easy integration of power model in behavioral synthesis tool that uses both a behavioral power estimator and a datapath scheduler. Using the dynamic energy model proposed in [Chang and Pedram 1997], the effective

switching capacitance can be expressed as,

$$\alpha_i C_i = C_{sw_i}(\alpha_i^1, \alpha_i^2) \quad (4)$$

Here, α_i and C_i are the parameters corresponding to the functional unit FU_i as defined before. C_{sw_i} is a measure of the effective switching capacitance of the functional unit FU_i , which is a function of α_i^1 and α_i^2 ; α_i^1 and α_i^2 are the average switching activities on the first and second input operands of resource FU_i . It may be noted that in the above switching model, (in Eqn. 4) the input pattern dependencies can be handled. Moreover, the generic power model can be easily tuned to handle any of the modes of datapath circuit operation, such as, SVSF, MVDFC and MVMC. Thus, we write the cycle power consumption of any control step of a DFG as follows.

$$P_c = \sum_{i=1}^{R_c} C_{sw_{i,c}} V_{i,c}^2 f_c \quad (5)$$

The notation $C_{sw_{i,c}}$ represents C_{sw_i} for the functional unit FU_i active in control step c . α_i^1 and α_i^2 are estimated using behavioral simulation of a DFG with a set of input vectors [Landman and Rabaey 1995; Satyanarayan and Parhi 2000; Ramprasad et al. 1997]. A look-up table is constructed that stores the C_{sw} values for $(\alpha^1$ and $\alpha^2)$ combinations for different types of functional units, such as multipliers and ALUs. We use interpolation to find the C_{sw} values for the $(\alpha^1$ and $\alpha^2)$ combinations that are not available in the look-up table.

We consider three modes of datapath operation, such as MVDFC, MVMC and SVSF. It may be noted that for the SVSF operation mode, $V_{i,c}$ and f_c is the same for all c , whereas for MVMC operation mode f_c is same for all c . Using Eqn. 5, 2, and 1, we can write CPF* for various modes of datapath operation as follows. Let us assume that V is the operating voltage for SVSF mode and f_{clk} is the operating frequency for MVMC or SVSF mode of datapath operation.

$$\begin{aligned} \text{CPF-MVDFC}^* &= \frac{\frac{1}{N} \sum_{c=1}^N \sum_{i=1}^{R_c} C_{sw_{i,c}} V_{i,c}^2 f_c}{\max \left(\sum_{i=1}^{R_c} C_{sw_{i,c}} V_{i,c}^2 f_c \right)_{\forall c}} \\ &+ \frac{\frac{1}{N} \sum_{c=1}^N \left(\left| \frac{1}{N} \sum_{c=1}^N \left(\sum_{i=1}^{R_c} C_{sw_{i,c}} V_{i,c}^2 f_c \right) - \sum_{i=1}^{R_c} C_{sw_{i,c}} V_{i,c}^2 f_c \right| \right)}{\max \left(\sum_{i=1}^{R_c} C_{sw_{i,c}} V_{i,c}^2 f_c \right)_{\forall c}} \\ \text{CPF-MVMC}^* &= \frac{\frac{1}{N} \sum_{c=1}^N \sum_{i=1}^{R_c} C_{sw_{i,c}} V_{i,c}^2 f_{clk}}{\max \left(\sum_{i=1}^{R_c} C_{sw_{i,c}} V_{i,c}^2 f_{clk} \right)_{\forall c}} \\ &+ \frac{\frac{1}{N} \sum_{c=1}^N \left(\left| \frac{1}{N} \sum_{c=1}^N \left(\sum_{i=1}^{R_c} C_{sw_{i,c}} V_{i,c}^2 f_{clk} \right) - \sum_{i=1}^{R_c} C_{sw_{i,c}} V_{i,c}^2 f_{clk} \right| \right)}{\max \left(\sum_{i=1}^{R_c} C_{sw_{i,c}} V_{i,c}^2 f_{clk} \right)_{\forall c}} \quad (6) \\ \text{CPF-SVSF}^* &= \frac{\frac{1}{N} \sum_{c=1}^N \sum_{i=1}^{R_c} C_{sw_{i,c}} V^2 f_{clk}}{\max \left(\sum_{i=1}^{R_c} C_{sw_{i,c}} V^2 f_{clk} \right)_{\forall c}} \\ &+ \frac{\frac{1}{N} \sum_{c=1}^N \left(\left| \frac{1}{N} \sum_{c=1}^N \left(\sum_{i=1}^{R_c} C_{sw_{i,c}} V^2 f_{clk} \right) - \sum_{i=1}^{R_c} C_{sw_{i,c}} V^2 f_{clk} \right| \right)}{\max \left(\sum_{i=1}^{R_c} C_{sw_{i,c}} V^2 f_{clk} \right)_{\forall c}} \end{aligned}$$

The above equations can be used as the objective functions for ILP formulations and con-

sequently, for the datapath scheduling algorithms. We develop scheduling algorithms that accept, an unscheduled DFG, the resource/time constraints, switching activity information, load capacitance, voltage levels and the number of allowable frequency levels as input parameters.

4. MODELING OF NON-LINEARITIES

The “modified cycle power function” CPF^* (Eqn. 6) discussed in the previous section, is a *non-linear function*. The nonlinearity is because of the *absolute function* (abs or $| \cdot |$) and also because of the *fractional form* of the function itself. The ILP formulations need to handle these two forms of non-linearity. We first address the transformations required to derive linear models of the nonlinear functions. Let us represent the general linear programming model as follows [Rao 1996] :

$$\begin{aligned} \text{Minimize : } & \sum_j c_j * x_j \\ \text{Subject to : } & \sum_j a_{ij} * x_j \leq b_i, \forall i; \quad x_j \geq 0, \forall j \end{aligned} \quad (7)$$

where, c_j, a_{ij}, b_i are known constants and x_j are the decision variables.

4.1 LP Formulation Involving Sum of Absolute Deviations

The general form of this type of programming can be represented as given below [Panik 1996; McCarl and Spreen 1997].

$$\begin{aligned} \text{Minimize : } & \sum_i |y_i| \\ \text{Subject to : } & y_i + \sum_j a_{ij} * x_j \leq b_i, \forall i; \quad x_j \geq 0, \forall j \end{aligned} \quad (8)$$

where, y_i , is the deviation between the prediction and observation. The $|y_i|$ is non-linear because of absolute function. This can be linearized using the following transformation.

Let, y_i be represented as the difference of two non-negative variables,

$$y_i = y_i^1 - y_i^2 \quad (9)$$

Using these variables, we can rewrite the LP formulation in Eqn. 8 as follows.

$$\begin{aligned} \text{Minimize : } & \sum_i |y_i^1 - y_i^2| \\ \text{Subject to : } & y_i^1 - y_i^2 + \sum_j a_{ij} * x_j \leq b_i, \forall i; \quad x_j \geq 0, \forall j; \quad y_i^1, y_i^2 \geq 0, \forall i \end{aligned} \quad (10)$$

If the product of y_i^1 and y_i^2 is zero, then,

$$|y_i^1 - y_i^2| = |y_i^1| + |y_i^2| = y_i^1 + y_i^2 \quad (11)$$

Using the above, we can write the LP formulation expressed in Eqn. 10 as shown below.

$$\begin{aligned} \text{Minimize : } & \sum_i y_i^1 + y_i^2 \\ \text{Subject to : } & y_i^1 - y_i^2 + \sum_j a_{ij} * x_j \leq b_i, \forall i; \quad x_j \geq 0, \forall j; \quad y_i^1, y_i^2 \geq 0, \forall i \end{aligned} \quad (12)$$

The formulations in Eqn. 8 and 12 are equivalent and the minimization of Eqn. 12 will result in the minimization of Eqn. 8.

4.2 LP Formulation Involving Fraction

The general expression for the LP formulation involving fractions is considered below [McCarl and Spreen 1997].

$$\begin{aligned} \text{Minimize : } & \frac{\sum_j c_j * x_j}{\sum_j d_j * x_j} \\ \text{Subject to : } & \sum_j a_{ij} * x_j \leq b_i, \forall i; \quad x_j \geq 0, \forall j \end{aligned} \quad (13)$$

where, c_j and d_j are known constants and the denominator $\sum_j d_j * x_j$ is strictly positive. Let us assume new variables as follows :

$$\begin{aligned} z_0 &= \left| d_0 + \sum_j d_j * x_j \right|^{-1} \\ x_j &= \frac{z_j}{z_0} \end{aligned} \quad (14)$$

Using the above transformation, the original formulation in Eqn. 13 can be modified to the following.

$$\begin{aligned} \text{Minimize : } & c_0 * z_0 + \sum_j c_j * z_j \\ \text{Subject to : } & \sum_j a_{ij} * z_j - b_i * z_0 \leq b_i, \forall i \\ & \sum_j d_j * z_j + d_0 * z_0 = 1; \quad z_0, z_j \geq 0, \forall j \end{aligned} \quad (15)$$

The problems defined in Eqn. 13 and 15 are equivalent. On solving the problem in Eqn. 15, we substitute, $z_j = x_j * z_0$ to get the results for x_j .

5. ILP FORMULATIONS TO MINIMIZE MODIFIED CYCLE POWER FUNCTION

In this section, we discuss the ILP models for minimization of the ‘‘modified cycle power function’’ (CPF*). We describe the ILP models for two different scenario of ASIC design. The first one targets design with multiple supply voltages and dynamic frequency clocking (MVDFC). The other one targets multiple supply voltages and multicycling (MVMC) based designs. The single voltage and single frequency (SVSF) ILP models become trivial once these two are presented and hence, are not shown. The ILP models formulated to ensure that the dependency constraints and the resource constraints are satisfied. In order to formulate an ILP based model for Eqn. 6 and the scheduling schemes for the DFG, we use the notations shown in Table II.

Table II. Notations used in ILP Formulations

$M_{k,v}$: maximum number of functional units of type k operating at voltage level v ($FU_{k,v}$)
S_i	: as soon as possible (ASAP) time stamp for the operation o_i
E_i	: as late as possible (ALAP) time stamp for the operation o_i
$P(C_{sw_i}, v, f)$: power consumption of functional unit FU_i at voltage level v and operating frequency f used by o_i for its execution
$x_{i,c,v,f}$: decision variable which takes the value of 1 if operation o_i is scheduled in control step c using the functional unit $F_{k,v}$ and c has frequency f_c
$y_{i,v,l,m}$: decision variable which takes the value of 1 if operation o_i is using the functional unit $F_{k,v}$ and scheduled in control steps $l \rightarrow m$
$L_{i,v}$: latency for operation o_i using functional unit operating at voltage v (in terms of number of clock cycles)

5.1 Multiple Supply Voltages and Dynamic Frequency Clocking (MVDFC)

In this subsection, we describe the ILP formulation for minimization of CPF-MVDFC* using multiple supply voltages and dynamic frequency clocking. In dynamic frequency clocking [Kim and Chae 1996; Ranganathan et al. 1998; Brynjolfson and Zilic 2000], the clock frequency is varied on-the-fly based on the functional units active in that cycle. In this clocking scheme, all the units are clocked by a single clock line which switches at run-time. The frequency reduction creates an opportunity to operate the different functional units at different voltages, which in turn, helps in further reduction of power.

(a) *Objective Function* : The objective is to minimize the modified cycle power function CPF-MVDFC* described in Eqn. 6 of the whole DFG over all control steps.

$$\text{Minimize : CPF-MVDFC}^* \quad (16)$$

Using Eqn. 2, this can be restated as :

$$\text{Minimize : } \frac{\frac{1}{N} \sum_{c=1}^N P_c + \frac{1}{N} \sum_{c=1}^N |P - P_c|}{P_{peak}} \quad (17)$$

This objective function has the two types of non-linearities mentioned in the previous section. We first remove the non-linearity introduced because of the fraction by putting the denominator as a constraint. Then, the problem in Eqn. 17 transformed to the one given below.

$$\begin{aligned} \text{Minimize : } & \frac{1}{N} \sum_{c=1}^N P_c + \frac{1}{N} \sum_{c=1}^N |P - P_c| \\ \text{Subject to : } & \text{Peak power constraints} \end{aligned} \quad (18)$$

However, this transformed problem still has the non-linearity in it because of the absolute function. This can be converted to an equivalent problem using the transformation suggested in the previous section.

$$\begin{aligned} \text{Minimize : } & \frac{1}{N} \sum_{c=1}^N P_c + \frac{1}{N} \sum_{c=1}^N (P + P_c) \\ \text{Subject to : } & \text{Modified peak power constraints} \end{aligned} \quad (19)$$

The “peak power constraint” in Eqn. 18 and the “modified peak power constraint” in Eqn. 19 will be discussed in later part of the subsection. Using Eqn. 1 repeatedly, the problem expressed in Eqn. 19 is simplified to :

$$\begin{aligned} \text{Minimize : } & \left(\frac{3}{N}\right) \sum_{c=1}^N P_c \\ \text{Subject to : } & \text{Modified peak power constraints} \end{aligned} \quad (20)$$

Using the decision variables, the objective function is formulated as,

$$\begin{aligned} \text{Minimize : } & \sum_c \sum_{i \in F_{k,v}} \sum_v \sum_f x_{i,c,v,f} * \left(\frac{3}{N}\right) * P(C_{sw_i}, v, f) \\ \text{Subject to : } & \text{Modified peak power constraints} \end{aligned} \quad (21)$$

Assuming, $P^*(C_{sw_i}, v, f)$ as $P(C_{sw_i}, v, f) * \left(\frac{3}{N}\right)$,

$$\begin{aligned} \text{Minimize : } & \sum_c \sum_{i \in F_{k,v}} \sum_v \sum_f x_{i,c,v,f} * P^*(C_{sw_i}, v, f) \\ \text{Subject to : } & \text{Modified peak power constraints} \end{aligned} \quad (22)$$

(b) *Uniqueness Constraints* : These constraints ensure that every operation o_i is scheduled to one unique control step within the mobility range (S_i, E_i) with a particular supply voltage and operating frequency. We represent them as, $\forall i, 1 \leq i \leq O$,

$$\sum_c \sum_v \sum_f x_{i,c,v,f} = 1 \quad (23)$$

(c) *Precedence Constraints* : These constraints guarantee that for an operation o_i , all its predecessors are scheduled in an earlier control step and its successors are scheduled in a later control step. These are modeled as, $\forall i, j, o_i \in Pred_{o_j}$,

$$\sum_v \sum_f \sum_{d=S_i}^{E_i} d * x_{i,d,v,f} - \sum_v \sum_f \sum_{e=S_j}^{E_j} e * x_{j,e,v,f} \leq -1 \quad (24)$$

(d) *Resource Constraints* : These constraints make sure that no control step contains more than $F_{k,v}$ operations of type k operating at voltage level v . These can be enforced as, $\forall c, 1 \leq c \leq N$ and $\forall v$,

$$\sum_{i \in F_{k,v}} \sum_f x_{i,c,v,f} \leq M_{k,v} \quad (25)$$

(e) *Frequency Constraints* : This set ensures that if a functional unit is operating at a higher voltage level then it can be scheduled in a lower frequency control step, whereas, a functional unit is operating at lower voltage level then it can not be scheduled in a higher frequency control step. We write these constraints as, $\forall i, 1 \leq i \leq O, \forall c, 1 \leq c \leq N$, if $f < v$, then $x_{i,c,v,f} = 0$.

(f) *Peak Power Constraints* : As discussed before, with reference to the Eqn. 17 and 18, these constraints are introduced to eliminate the fractional non-linearity of the objective function. These constraints ensure that the maximum power consumption of the DFG does not exceed P_{peak} for any control step. We enforce these constraints as follows, $\forall c, 1 \leq c \leq N$,

$$\sum_{i \in F_{k,v}} \sum_v \sum_f x_{i,c,v,f} * P(C_{swi}, v, f) \leq P_{peak} \quad (26)$$

The P_{peak} is peak power constraint, which is an unknown value during the minimization process, so it is added alongwith the objective function and minimized.

(g) *Modified Peak Power Constraints* : To eliminate the non-linearity introduced due to the absolute function, we modify the above constraints, as outlined in Eqn. 18 and 19. The peak power constraints in Eqn. 26 is modified as, $\forall c, 1 \leq c \leq N$,

$$\frac{1}{N} \sum_c \sum_{i \in F_{k,v}} \sum_v \sum_f x_{i,c,v,f} * P(C_{swi}, v, f) - \sum_{i \in F_{k,v}} \sum_v \sum_f x_{i,c,v,f} * P(C_{swi}, v, f) \leq P_{peak}^* \quad (27)$$

The P_{peak}^* is a modified peak power constraint which is added to the objective function and minimized alongwith it.

5.2 Multiple Supply Voltages and Multicycling (MVMC)

In this subsection, we describe the ILP formulations based on the modified cycle power function CPF-MVMC* (Eqn. 6) using multiple supply voltages and multicycling. In this scheme, the functional units are operated at multiple supply voltages. The functional units operating at lower voltages may need to be active in more than one consecutive control steps to complete execution.

(a) *Objective Function* : The objective is to minimize the CPF-MVMC* for the entire DFG. Using Eqn. 1, this can be represented as :

$$\begin{aligned} \text{Minimize : } & \text{CPF-MVMC}^* \\ & = \frac{\frac{1}{N} \sum_{c=1}^N P_c + \frac{1}{N} \sum_{c=1}^N |P - P_c|}{P_{peak}} \end{aligned} \quad (28)$$

As discussed in the previous subsection, this objective function has two types of non-linearities, which are because of the absolute function and the fractional form. The fractional non-linearity is removed by introducing the denominators as a constraint. The corresponding constraints are known as “peak power constraints”. We remove the absolute function non-linearity by modifying the peak power constraints which give rises to “modified peak power constraints”. Thus, the problem in Eqn. 28 is transformed to the following.

$$\begin{aligned} \text{Minimize : } & \frac{1}{N} \sum_{c=1}^N P_c + \frac{1}{N} \sum_{c=1}^N (P + P_c) \\ \text{Subject to : } & \text{Modified peak power constraints} \end{aligned} \quad (29)$$

The “peak power constraint” and the “modified peak power constraint” are discussed in the later part of the subsection. Using Eqn. 1 repeatedly, the problem in Eqn. 29 is simplified to :

$$\begin{aligned} \text{Minimize : } & \left(\frac{3}{N}\right) \sum_{c=1}^N P_c \\ \text{Subject to : } & \text{Modified peak power constraints} \end{aligned} \quad (30)$$

Using the decision variables, the above LP objective function is formulated as,

$$\begin{aligned} \text{Minimize : } & \sum_l \sum_{i \in F_{k,v}} \sum_v y_{i,v,l,(l+L_{i,v}-1)} * \left(\frac{3}{N}\right) P(C_{sw_i}, v, f) \\ \text{Subject to : } & \text{Modified peak power constraints} \end{aligned} \quad (31)$$

Where, f is the operating frequency level of the datapath circuit in multicycling mode.

$$\begin{aligned} \text{Minimize : } & \sum_l \sum_{i \in F_{k,v}} \sum_v y_{i,v,l,(l+L_{i,v}-1)} * P^*(C_{sw_i}, v, f) \\ \text{Subject to : } & \text{Modified peak power constraints} \end{aligned} \quad (32)$$

Where, $P^*(C_{sw_i}, v, f) = \left(\frac{3}{N}\right) * P(C_{sw_i}, v, f)$, are modified power values.

(b) *Uniqueness Constraints* : These constraints ensure that every operation o_i is scheduled in appropriate control steps within the mobility range (S_i, E_i) with a particular supply voltage. Depending on the supply voltage it may be operated at more than one clock cycle. We represent them as, $\forall i, 1 \leq i \leq O$,

$$\sum_v \sum_{l=S_i}^{S_i+E_i+1-L_{i,v}} y_{i,v,l,(l+L_{i,v}-1)} = 1 \quad (33)$$

When the operators are computed at the highest voltage, they are scheduled in one unique control step, whereas, when they are to be operated at lower voltages they need more than

one clock cycle for completion. Thus, for lower voltage, the mobility is restricted.

(c) *Precedence Constraints* : These constraints guarantee that for an operation o_i , all its predecessors are scheduled in earlier control step and its successors are scheduled in later control step. These constraints should also take care of the multicycling operations. These are modeled as, $\forall i, j, o_i \in Pred_{o_j}$,

$$\sum_v \sum_{l=S_i}^{E_i} (l + L_{i,v} - 1) * y_{i,v,l,(l+L_{i,v}-1)} - \sum_v \sum_{l=S_j}^{E_j} l * y_{j,v,l,(l+L_{j,v}-1)} \leq -1 \quad (34)$$

(d) *Resource Constraints* : These constraints make sure that no control step contains more than $F_{k,v}$ operations of type k operating at voltage v . These can be enforced as, $\forall v$ and $\forall l$, $1 \leq l \leq N$,

$$\sum_{i \in F_{k,v}} \sum_l y_{i,v,l,(l+L_{i,v}-1)} \leq M_{k,v} \quad (35)$$

(e) *Peak Power Constraints* : As discussed earlier with reference to Eqn. 28 and 29, these constraints are enforced to eliminate the fractional non-linearity of the objective function. We enforce these constraints as follows, $\forall l$, $1 \leq l \leq N$,

$$\sum_{i \in F_{k,v}} \sum_v y_{i,v,l,(l+L_{i,v}-1)} * P(C_{swi}, v, f) \leq P_{peak} \quad (36)$$

Where, P_{peak} is the peak power constraint which is added to the objective function and minimized along with it.

(f) *Modified Peak Power Constraints* : These constraints are introduced to eliminate the absolute function non-linearity of the objective function. These constraints can be enforced as, $\forall l$, $1 \leq l \leq N$,

$$\frac{1}{N} \sum_l \sum_{i \in F_{k,v}} \sum_v y_{i,v,l,(l+L_{i,v}-1)} * P(C_{swi}, v, f) - \sum_{i \in F_{k,v}} \sum_v y_{i,v,l,(l+L_{i,v}-1)} * P(C_{swi}, v, f) \leq P_{peak}^* \quad (37)$$

Where, P_{peak}^* is the modified peak power constraint which is also minimized as a part of the objective function.

6. ILP-BASED SCHEDULING

In this section, we discuss the solutions for the ILP formulations obtained in the previous section and develop scheduling algorithms for MVDFC and MVMC schemes. The scheduling for SVSF is simple and not discussed here for brevity. The target architecture model assumed for the scheduling schemes is from [Johnson and Roy 1997]. Each functional unit has a register and a multiplexer associated with it. The register and the multiplexer operate at the same voltage level as that of the functional unit. Level converters are used when a low-voltage functional unit drives a high-voltage functional unit [Johnson and Roy 1997; Shiue and Chakrabarti 2000b]. A controller decides which of the functional units are active in each control step and those that are not active are disabled using the multiplexors. For MVDFC scheme, the controller has a storage unit to store cycle

frequency index (cfi_c) values obtained from scheduling. This serves as the clock dividing factor for the dynamic clocking unit. The cycle frequency f_c is generated dynamically and a functional unit operating at one of the supply voltages is activated.

The inputs to the algorithm are an unscheduled data flow graph (UDFG), the resource constraints, the number of allowable voltage levels (L_V), the number of allowable frequencies (L_f), the delay of each resource (d_{FU}), the multiplexor (d_{Mux}), the register (d_{Reg}) at different voltage levels. The delays of level converters (d_{Conv}) is represented in the form of a matrix that shows the delay in converting one at voltage level V_i to another voltage level V_j (where, both $V_i, V_j \in V_{L_V}$). The resource constraint includes the number of ALUs and multipliers at different voltage levels V_i (where, $V_i \in V_{L_V}$). The scheduling algorithm determines the f_{base} , cfi_c time stamp for each operation, and voltage level such that the function CPF* (Eqn. 6) is minimum.

Input	: UDFG, resource constraints, L_V , L_f , all $V_i \in V_{L_V}$, d_{FU} , d_{Mux} , d_{Reg} , d_{Conv}
Output	: scheduled DFG, f_{base} , N , cfi_c , power, energy and delay estimates
Step 1	: Construct a look up table for (effective switching capacitance, average switching activity) pairs.
Step 2	: Calculate the switching activities at the inputs of each node through behavioral simulation of the DFG.
Step 3	: Find ASAP schedule for the UDFG.
Step 4	: Find ALAP schedule for the UDFG.
Step 5	: Determine the mobility graph of each node.
Step 6	: Modify the mobility graph for MVMC.
Step 7	: Model the ILP formulations of the DFG for MVDFC, MVMC or SVSF scheme using AMPL.
Step 8	: Solve the ILP formulations using LP-Solve.
Step 9	: Find the scheduled DFG.
Step 10	: Determine the cycle frequencies (f_c), f_{base} and cfi_c for MVDFC scheme.
Step 11	: Estimate the power and energy consumptions of the scheduled DFG.

Fig. 1. Scheduling for CPF* minimization

The ILP based scheduler which minimizes the modified cycle power function CPF* of the DFG is outlined in Fig. 1. In step 1, the scheduler constructs a look-up table to store the effective switching capacitance and the average switching activity value pairs. In step 2, the scheduler determines the switching activities at the inputs of each node by using behavioral simulation of DFG. For this purpose, a different set of application specific input vectors (having different correlations) are given at the primary inputs of the DFG and average switching activity at each inputs of other nodes are calculated. It should be noted that if the look-up table (in step 1) does not have the switching capacitance for an average switching activity value (in step 2), then the scheduler uses interpolation techniques to find the same. The third step is to determine the as soon as possible (ASAP) time stamp of each operation. The fourth step is the determination of the as late as possible (ALAP) time stamp of each vertex for the DFG. The ASAP time stamp is the start time and the ALAP time stamp is the finish time of each operation. These two time stamps provide the mobility of an operation and the operation must be scheduled within this mobility range. This mobility graph needs to be modified for the MVMC scheme. The ILP formulations constructed based on the models described in section 5. The scheduler uses the modeling language AMPL to model the ILP formulations [Fourer et al. 2003]. At this step, we calculate the power consumption of the functional units as follows. The operational delay of a functional unit is assumed as

$(d_{FU} + d_{Mux} + d_{Reg} + d_{Conv})$. For the MVMC scheme, the operating frequency depends on the delay of the multiplier unit operating at the highest voltage level allowed. For the MVDFC scheme, the operating frequency of a functional unit is calculated using the formulas for delay given in [Mohanty and Ranganathan 2003a]. We obtain the switching capacitance from steps 1 and 2, and the power values are calculated whenever necessary for different operating voltages and frequencies. The scheduled DFG is obtained after the ILP formulation is solved using LP-Solve. Then, the scheduler determines the f_{base} , cfi_c and cycle frequency (f_c) using the methods proposed in [Mohanty and Ranganathan 2003a] based on the delay of each cycle. Finally, the power consumption, energy consumption and the energy delay product of the scheduled DFG are calculated.

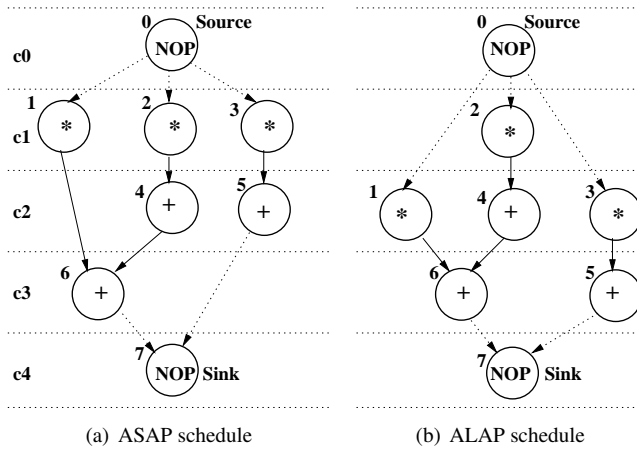


Fig. 2. ASAP and ALAP schedule for example (EXP) DFG

6.1 MVDFC Scheduling Scheme

We illustrate the solution for the ILP formulation in the MVDFC case, with the help of the DFG shown in Fig. 2. The ASAP schedule is shown in Fig. 2(a) and the ALAP schedule is shown in Fig. 2(b). From the ASAP and ALAP schedules, we obtained the mobility graph which is Fig. 3(a). We get the ILP formulations using this mobility graph. We solved the formulation using LP-solve and based on the results, we obtained the scheduled DFG shown in Fig. 3(b) for the resource constraint (RC5), two multipliers at $2.4V$ and one ALU operating at $3.3V$. Similarly, other schedules can be obtained for different resource constraints.

6.2 MVMC Scheduling Scheme

We illustrate the solution for the ILP formulations of the MVMC case, using the DFG shown in Fig. 2. The ASAP schedule is shown in Fig. 2(a) and the ALAP schedule is shown in Fig. 2(b). From the ASAP schedule (Fig. 2(a)) and the ALAP schedule (Fig. 2(b)), we obtained the mobility graph shown in Fig. 4(a). This mobility graph is different from that shown in Fig. 3(a). In the MVMC case, the mobility graph considers the multicycle operations. In this illustration, we assume that we have two operating voltage levels, and when the multipliers are operated at the lower voltage, they take two clock

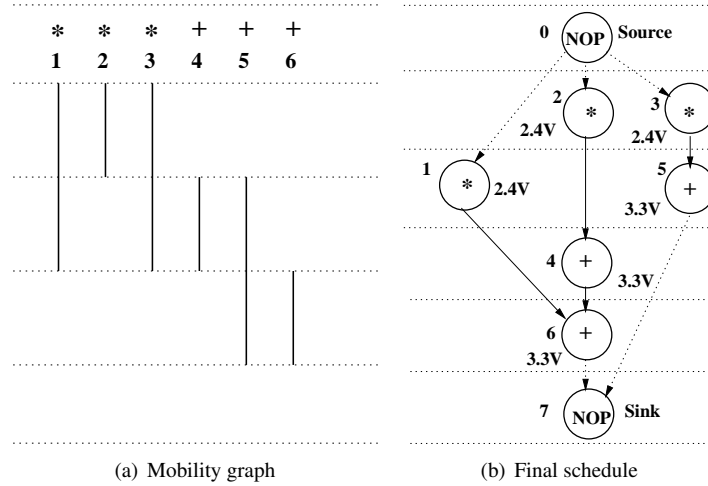


Fig. 3. Mobility graph and final schedule for example DFG for RC5 using MVDFC

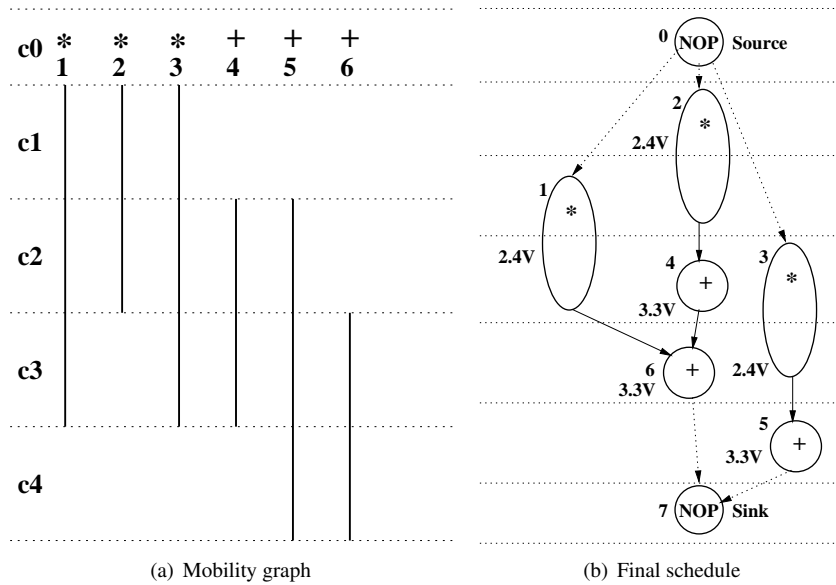


Fig. 4. Mobility graph and final schedule for example DFG for RC5 using MVMC

cycles. It should be noted that the mobility graph will depend on the number of operating voltages and the assumed operating frequency. We solved the ILP formulation using LP-solve and based on the results we obtained the scheduled DFG shown is Fig. 4(b) for the resource constraint (RC5), two multipliers at 2.4V and one ALUs operating at 3.3V.

7. EXPERIMENTAL RESULTS

The following notations are used to express the results :

P_{pS} : the peak power consumption (in mW) SVSF scheme,

P_{pD} : the peak power consumption (in mW) for MVDFC operation,

P_{pM} : the peak power consumption (in mW) for MVMC operation,

P_{mS} : minimum power consumption for any cycle assuming SVSF (in mW)

P_{mD} : minimum power consumption for any cycle for MVDFC (in mW)

T_S : execution time for single frequency

T_D : execution time for dynamic frequency

T_M : execution time for multicycling operation

E_S : total energy consumption (in nano-Joule or nJ) for SVSF scheme,

E_D : total energy consumption (in nJ) for MVDFC operation,

E_M : total energy consumption (in nJ) for MVMC operation,

P_S : average power consumption (in mW) for SVSF scheme, which is calculated as the mean of the cycle power consumptions

P_D : average power consumption (in mW) for MVDFC operation, estimated as the mean of the cycle power

P_M : average power consumption (in mW) for MVDFC operation, calculated as the mean of the cycle power consumptions

EDP_S : energy delay product (in 10^{-15} Joule-sec or fJs) for SVSF operation ($= E_S * T_S$)

EDP_D : energy delay product (in fJs) for MVDFC operation ($= E_D * T_D$)

EDP_M : energy delay product (in fJs) for MVMC operation ($= E_M * T_M$)

ΔP_p : percentage peak power reduction, for MVDFC scheme this is defined as, $\frac{(P_{pS}-P_{pD})}{P_{pS}} * 100$

and for MVMC scheme it is calculated as, $\frac{(P_{pS}-P_{pM})}{P_{pS}} * 100$

ΔDP : percentage peak differential power reduction, which is calculated as

$\frac{(P_{pS}-P_{mS})-(P_{pD}-P_{mD})}{(P_{pS}-P_{mS})} * 100$ for MVDFC scheme and as $\frac{(P_{pS}-P_{mS})-(P_{pM}-P_{mM})}{(P_{pS}-P_{mS})} * 100$

for MVMC scheme

ΔP : percentage average power reduction, for MVDFC scheme it is $\frac{P_S-P_D}{P_S} * 100$ and for MVMC scheme it is $\frac{P_S-P_M}{P_S} * 100$

ΔE : percentage reduction in total energy, is calculated as $\frac{E_S-E_D}{E_S} * 100$ for MVDFC scheme and as $\frac{E_S-E_M}{E_S} * 100$ for MVMC scheme

ΔEDP : percentage EDP reduction, calculated as $\frac{(EDP_S-EDP_D)}{EDP_S} * 100$ for MVDFC scheme and as $\frac{(EDP_S-EDP_M)}{EDP_S} * 100$ for MVMC scheme

The ILP based schedulers were tested with five benchmark circuits :

- (1) Example circuit (EXP) (8 nodes, 3*, 3+, 9 edges),
- (2) FIR filter (11 nodes, 5*, 4+, 19 edges),
- (3) HAL differential equation solver (13 nodes, 6+, 2+, 2-, 1 <, 16 edges),
- (4) IIR filter (11 nodes, 5*, 4+, 19 edges) and
- (5) Auto-Regressive filter (ARF) (15 nodes, 5*, 8+, 19 edges).

We used the look-up table method presented in Section 3 for the average switching capacitance calculation. The look-up table construction consists of two phases, such as input pattern generation and cell characterization. We generate the primary input signals of different correlations using the autoregressive moving average (ARMA) model [Ramprasad

et al. 1997]. We perform the characterization of the physical implementations of the library modules available in [Mohanty and Ranganathan 2003b] by applying the input patterns generated above for some values of $(\alpha_i^{-1}, \alpha_i^2)$ pairs. Whenever necessary, we used interpolation to find the average switching capacitance for any other values of $(\alpha_i^{-1}, \alpha_i^2)$ pairs that do not exist in the look-up table. It should be noted that larger the size of look-up table, better is the accuracy. The above generated signals are propagated through different operators in the DFG and the average switching activities are calculated as described in [Ramprasad et al. 1997].

The scheduling algorithms were tested for five different sets of resource constraints (RC1,RC2,RC3,RC4,RC5):

- (1) multipliers (2 at 2.4V and 1 at 3.3V) and ALUs (1 at 2.4V and 1 at 3.3V),
- (2) multipliers (3 at 2.4V) and ALUs (1 at 2.4V and 1 at 3.3V),
- (3) multipliers (2 at 2.4V) and ALUs (2 at 3.3V),
- (4) multipliers (1 at 2.4V and 1 at 3.3V) and ALUs (1 at 3.3V), and
- (5) multipliers (2 at 2.4V) and ALUs (1 at 3.3V).

The sets of resource constraints were chosen to be a good representation of the different types of resources at different operating voltages. The number of allowable voltage levels is two (2.4V, 3.3V) and maximum number of allowable frequencies being three. The experimental results for various benchmark circuits are reported in Table III for the MVDFC scheduling scheme and in Table IV for the MVMC scheduling scheme. The power/energy estimation include the power consumption of the overheads, such as level converters (data taken from [Mohanty and Ranganathan 2003b]). The results are reported for two supply voltages. In case of MVDFC scheduling the frequencies found out are 4.5MHz, 9MHz, 18MHz. For MVMC scheduling scheme, the operating frequency f_{clk} is 9MHz. The operating voltage and frequency for SVSF scheme is 3.3V and 9MHz, respectively. The tables show the estimates for power, energy and energy delay product for various benchmarks for different resource constraints. The reductions in power values are reported in terms of percentage with respect to single supply voltage and single frequency (SVSF) operation mode. The reductions in peak power, peak power differential and average power are in the range 70 – 76% for MVDFC; on the other hand, the reductions are in the range 0 – 40% for MVMC. The tables do not report the reduction in cycle difference power reduction due to lack of space as the tables became too large to fit the specified margin. Hence, we preferred to report peak power differential, which is a measure of maximum power fluctuation in a DFG. The reduction in the energy delay products for most of the benchmarks indicate that the reduction in power and energy achieved without compromising with the performance. This significance of the proposed scheduling approaches minimizing the new multicost objective function.

We plotted Fig. 5(a) and 5(b) to get a visual picture of the experimental results. The figures show the average reductions for different benchmarks averaged over all resource constraints. It is obvious from the figure that the reductions are significant, which are in the range 44 – 74% for MVDFC for various power and energy. Similarly, for MVMC, the average reductions are in the range 22 – 39%. It may also be noted that for the reductions for MVDFC scheme is better than the MVMC scheme. The MVDFC scheme works effectively for all resource constraints and all benchmarks, where as, the MVMC scheme does not produce good results for ARF benchmark. We did not find any work in the literature that deals with simultaneous reduction of energy and transient power, so we could not

Table III. Power, energy and energy delay product estimates for benchmarks using MVDFC

	P_{PS}	P_{PD}	ΔP	P_{mS}	P_{mD}	ΔDP	P_S	P_D	ΔP	E_S	E_D	ΔE	EDP_S	EDP_D	ΔEDP	
	mW	mW	%	mW	mW	%	mW	mW	%	nJ	nJ	%	fJ_s	fJ_s	%	
(1) E	1	17.28	4.56	73.61	0.46	0.35	74.97	8.87	2.42	72.72	2.96	1.57	46.8	0.99	0.87	11.34
	2	17.28	4.56	73.61	0.46	0.35	74.97	8.87	2.42	72.72	2.96	1.57	46.8	0.99	0.87	11.34
	3	17.28	4.56	73.61	0.46	0.9	78.24	8.87	2.61	70.57	2.96	1.6	46.0	0.99	0.8	18.98
	4	8.87	2.39	73.05	0.45	0.23	77.55	6.67	1.87	71.96	2.96	1.58	46.4	1.31	1.14	12.89
	5	17.28	4.56	73.61	0.23	0.45	75.89	6.65	1.96	70.53	2.96	1.6	45.9	1.31	0.87	32.49
Average values				73.50			76.32			71.70		46.38		1.31	0.87	17.41
(2) F	1	17.51	4.62	73.62	0.23	0.12	73.96	8.82	2.35	73.36	4.9	2.6	47.2	2.7	2.3	15.52
	2	25.92	6.84	73.61	0.23	0.12	73.84	8.82	2.36	73.24	4.9	2.6	47.2	2.7	2.0	26.09
	3	17.51	4.67	73.33	0.23	0.45	75.58	8.82	2.5	71.66	4.9	2.6	46.22	2.7	2.0	24.71
	4	17.28	6.6	61.81	0.23	0.45	63.93	8.82	2.84	67.8	4.9	3.1	36.98	2.7	2.9	NA
	5	17.51	4.67	73.33	0.23	0.45	75.58	8.82	2.5	71.66	4.9	2.6	46.22	2.7	2.0	24.71
Average values				71.14			72.60			71.54		44.76		2.7	2.0	16.21
(3) H	1	17.51	4.62	73.62	0.46	0.35	74.96	13.25	3.55	73.21	5.9	3.12	47.0	2.62	2.43	7.25
	2	26.15	6.9	73.61	0.46	0.35	74.5	13.25	3.55	73.21	5.9	3.12	47.0	2.62	2.43	7.25
	3	17.74	4.78	73.05	0.46	0.9	76.97	13.25	3.73	71.85	5.9	3.17	46.2	2.62	2.23	12.55
	4	17.51	6.71	61.68	0.23	0.45	63.77	10.6	3.73	64.8	5.9	4.07	30.8	3.27	3.85	NA
	5	17.51	4.67	73.33	0.23	0.45	75.6	10.6	2.98	71.9	5.9	3.17	46.2	3.27	2.46	24.66
Average values				71.06			73.16			71.0		43.44		3.27	2.46	10.34
(4) I	1	25.92	8.88	65.74	0.23	0.12	65.9	11.03	3.5	68.36	4.9	3.05	37.7	2.18	2.04	6.57
	2	25.92	6.84	73.61	0.23	0.12	73.84	11.03	2.98	72.98	4.9	2.6	47.96	2.18	1.73	20.44
	3	17.51	4.67	73.34	0.23	0.45	75.58	8.82	2.57	70.86	4.9	2.64	46.22	2.72	2.05	24.71
	4	17.51	6.71	61.68	0.23	0.45	63.77	8.82	3.32	62.86	4.9	3.54	27.73	2.72	2.75	NA
	5	17.51	4.67	73.33	0.23	0.45	75.58	8.82	2.5	71.66	4.9	2.64	46.22	2.72	2.05	24.71
Average values				69.54			71.65			69.34		41.17		2.72	2.05	15.24
(5) A	1	8.87	2.34	73.62	0.23	0.12	74.1	4.5	1.22	72.9	5.0	2.64	47.2	5.56	4.4	20.83
	2	8.87	2.34	73.62	0.23	0.12	74.1	4.5	1.22	72.9	5.0	2.64	47.2	5.56	4.4	20.83
	3	8.87	2.39	73.05	0.23	0.45	77.6	4.5	1.4	68.9	5.0	2.74	45.3	5.56	3.8	31.63
	4	8.87	2.39	73.05	0.23	0.45	77.6	4.5	1.4	68.9	5.0	2.74	45.3	5.56	3.8	31.63
	5	8.87	2.39	73.05	0.23	0.45	77.6	4.5	1.4	68.9	5.0	2.74	45.3	5.56	3.8	31.63
Average values				73.28			76.20			70.5		46.06		5.56	3.8	27.31
Overall average				71.70			74.0			70.82		44.36				17.31

Table IV. Power, energy and energy delay product estimates for benchmarks using MVMC

R	$P_{p,S}$ mW	$P_{p,M}$ mW	ΔP_p %	$P_{m,S}$ mW	$P_{m,M}$ mW	ΔDDP %	P_S mW	P_M mW	ΔP %	E_S nJ	E_M nJ	ΔE %	EDP_S fJs	EDP_M fJs	ΔEDP %
C	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
1	17.28	13.2	23.61	0.46	0.35	23.6	8.87	6.84	22.9	3.0	2.03	31.47	0.99	0.9	8.63
(1)	17.28	13.7	20.83	0.46	0.35	20.8	8.87	6.96	21.53	3.0	1.57	46.8	0.99	0.7	29.07
E	17.28	9.12	47.22	0.46	0.46	48.51	8.87	5.61	36.75	3.0	1.57	46.0	0.99	0.89	9.98
X	8.87	13.43	NA	0.23	0.23	NA	6.67	6.77	NA	3.0	2.5	16.46	1.31	1.11	15.33
P	17.28	9.35	45.9	0.23	0.23	46.51	6.65	5.61	15.64	3.0	1.6	46.0	1.31	0.89	32.5
Average values	17.51	17.76	27.51	0.23	0.23	27.88	8.87	7.67	19.36	4.9	3.09	37.35	2.72	2.06	19.10
(2)	25.92	13.68	47.22	0.23	0.12	47.21	8.82	7.66	13.15	4.9	2.59	47.2	2.72	2.06	24.38
F	17.51	9.35	46.6	0.23	0.23	47.22	8.82	7.75	12.13	4.9	2.64	46.22	2.72	2.05	36.64
I	17.28	13.43	22.28	0.23	0.23	22.58	8.82	7.51	14.85	4.9	4.0	18.5	2.72	2.66	24.71
R	17.51	9.35	46.6	0.23	0.23	47.22	8.82	6.65	24.6	4.9	2.64	46.22	2.72	2.05	2.19
Average values	17.51	17.76	32.54	0.46	0.35	32.85	13.25	9.08	15.55	5.9	4.0	39.03	2.62	2.05	22.53
(3)	26.15	13.8	47.23	0.46	0.35	47.64	13.25	9.24	30.26	5.9	3.2	47.0	2.62	2.08	NA
H	17.74	9.58	46.0	0.46	0.46	47.22	13.25	7.98	39.77	5.9	3.2	46.19	2.62	2.46	20.61
A	17.51	13.43	23.3	0.23	0.23	23.61	10.6	9.0	15.2	5.9	5.0	15.4	3.27	3.32	6.11
L	17.51	9.35	46.6	0.23	0.23	47.22	10.6	6.41	39.53	5.9	3.17	46.18	3.27	2.82	NA
Average values	17.51	17.76	32.63	0.23	0.23	33.14	11.03	8.95	33.14	4.9	3.17	37.27	3.27	2.82	8.10
(4)	25.92	17.76	31.48	0.23	0.12	31.34	11.03	8.95	18.85	4.9	4.0	19.22	2.18	2.2	NA
I	25.92	13.8	46.76	0.23	0.12	46.75	11.03	7.68	30.37	4.9	2.6	47.2	2.18	1.72	20.81
I	17.51	9.12	47.92	0.23	0.23	48.55	8.82	5.82	34.01	4.9	2.6	46.22	2.72	2.34	13.96
I	17.51	13.43	23.3	0.23	0.23	23.61	8.82	7.51	14.85	4.9	3.54	27.73	2.72	2.36	13.28
R	17.51	9.12	47.92	0.23	0.23	48.55	8.82	5.82	34.01	4.9	2.64	46.22	2.72	2.34	16.23
Average values	17.51	17.76	39.48	0.23	0.23	39.76	8.82	7.67	26.42	4.9	2.64	37.32	2.72	2.34	12.76
(5)	8.87	9.24	NA	0.23	0.12	NA	4.5	3.58	20.44	5.0	2.64	47.22	5.56	3.81	31.4
A	8.87	9.24	NA	0.23	0.12	NA	4.5	3.58	20.44	5.0	2.64	47.22	5.56	3.81	31.4
R	8.87	9.35	NA	0.23	0.23	NA	4.5	3.65	18.9	5.0	2.74	45.3	5.56	3.95	28.9
F	8.87	13.43	NA	0.23	0.23	NA	4.5	3.56	20.9	5.0	3.19	36.24	5.56	4.60	17.11
F	8.87	9.35	NA	0.23	0.23	NA	4.5	3.65	18.9	5.0	2.74	45.3	5.56	3.95	28.9
Average values	8.87	9.35	0	0.23	0.23	0	4.5	3.65	19.92	5.0	2.74	44.26	5.56	3.95	27.54
Overall average	17.51	17.76	26.44	0.23	0.23	26.73	8.87	7.67	22.51	4.9	3.09	39.05	2.72	2.06	17.99

provide comparison with any other works.

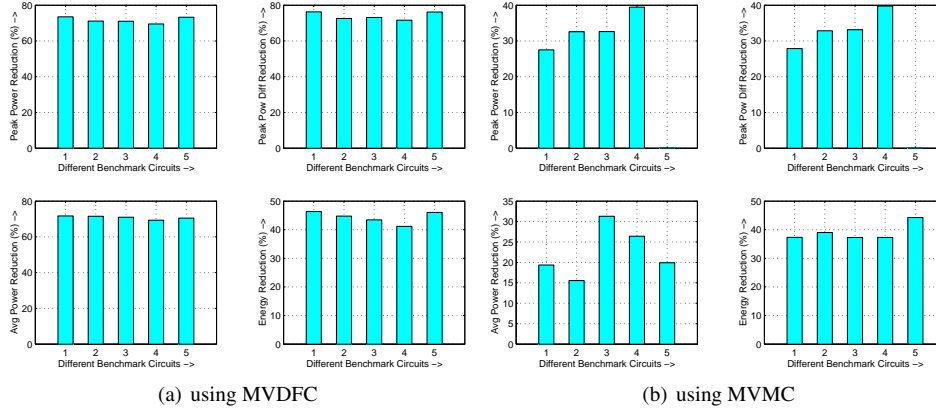


Fig. 5. Average reductions in power or energy for various benchmark circuits

In order to study the power profile, we plotted the cycle power consumption for different benchmarks over all the control steps (clock steps). Fig. 6(a), 6(b), 6(c), 6(d), and 6(e) show power profiles for benchmarks for resource constraints RC1, RC2, RC3, and RC4, respectively. The curves labeled as “SF” correspond to the profile when the schedule is operated at a single frequency (which is the maximum frequency of slower operator, multiplier) and single voltage. The profiles labeled as “DFC” correspond to the case when dynamic clocking and multiple voltage scheme is used. Similarly, the profiles labeled as “MC” are for the MVMC scheme. The effectiveness of the proposed scheduling schemes can be seen from the plots. For MVDFC scheme, the power consumption profile has improved compared to either MVMC or SVSF scheme.

8. CONCLUSIONS

In low power designs for portable applications, the simultaneous minimization of total energy and transient power is essential. The metric CPF* defined and used in this work essentially facilitates such simultaneous optimization using ILP formulations. The optimization is performed using MVDFC scheme and MVMC scheme. The datapath scheduling algorithm described in this paper is particularly useful for synthesizing data intensive application specific integrated circuits. The algorithm attempts to optimize energy and power while maintaining performance. The scheduling algorithm assumes number of different types of resources at each voltage levels (both MVDFC and MVMC) and the number of allowable frequencies (MVDFC scheme) as resource constraints. The energy delay product for both the MVDFC and MVMC scheduling scenario was estimated to keep track of the effect of scheduling algorithms on circuit performance. The MVDFC scheduling resulted in reduction of EDP for all benchmarks and all resource constraints, which shows its effectiveness. On the other hand, the MVMC scheme resulted in improvement in EDP in almost all cases, except for a few cases, where there was no improvement. *The results clearly indicate that the multiple supply voltage and dynamic frequency clocking scheme*

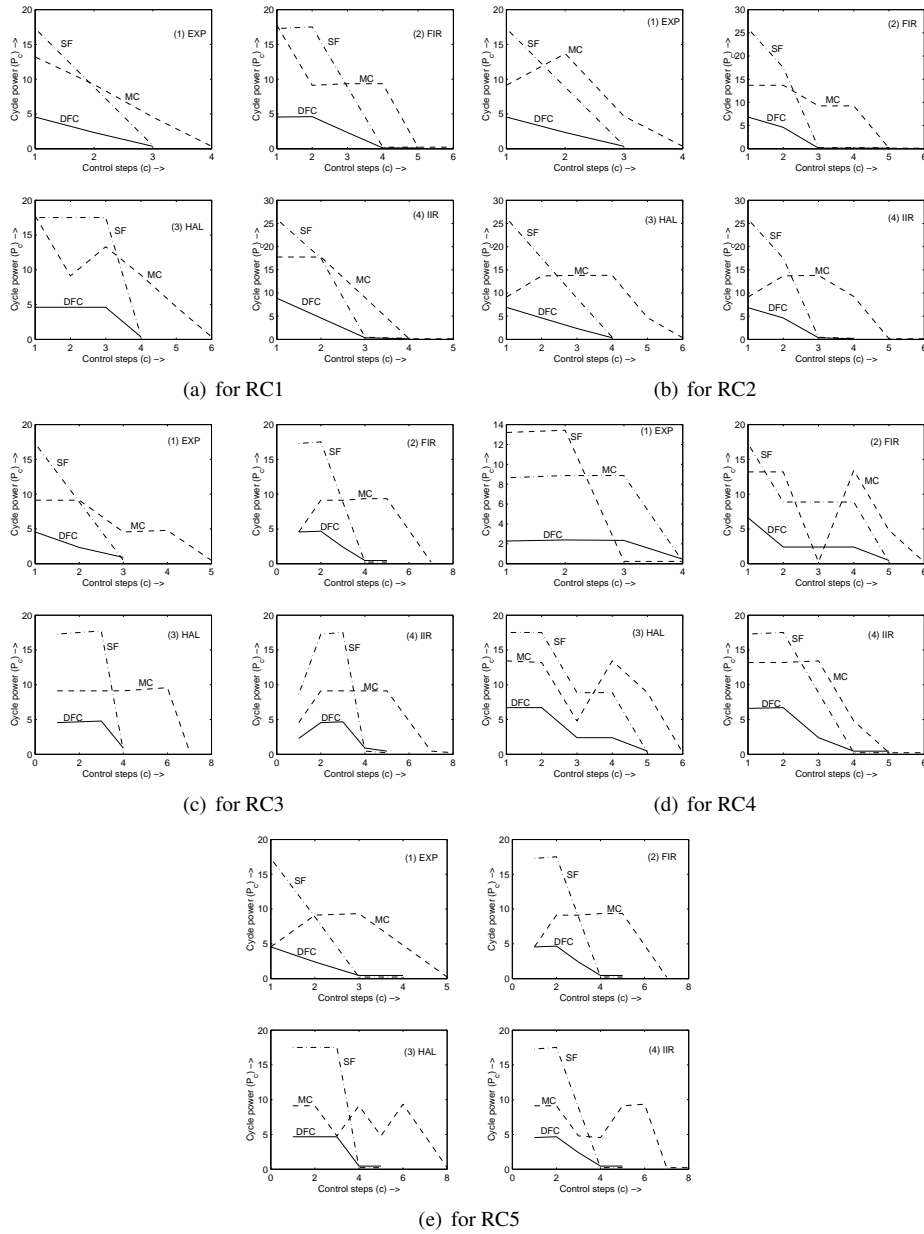


Fig. 6. Power profile for benchmark circuit for different resource constraints

yields better power and energy minimization than the multiple supply voltage and multi-cycling scheme. The effectiveness of the scheduling schemes in the context of pipelined datapaths and also in control intensive applications, still needs to be investigated.

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