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Design metrics for gate oxide leakage characterization in nano-CMOS transistors

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In this paper we propose a set of novel metrics, of primary interest to modeling and design engineers, for characterizing the impact of gate oxide tunneling current in nanoscale CMOS (nano-CMOS) devices. We concentrate on three distinct quantities: (i) steady-state on current (I_{ON}), (ii) steady-state off current (I_{OFF}), and (iii) effective tunneling capacitance during transitions (C_{eff}^{t}). We define C_{eff}^{t} as the change in tunneling current with respect to the rate of change of input voltage, which represents the capacitive load of the transistor due to tunneling. This concisely encapsulates both qualitative as well as quantitative information about the swing in tunneling current during state transitions, while simultaneously accounting for the transition rate. We also investigate, via Monte Carlo simulations, the effect of process and design variations on the metrics. To the best of our knowledge, this is the first ever work that quantifies gate leakage during state transitions through the use of C_{eff}^{t} .

Keywords: Gate tunneling; Direct tunneling; Nanoscale CMOS; Monte Carlo simulations

1. Introduction

As transistor feature sizes shrink with technology scaling, there has been a drastic change in the leakage components of the device in both active as well as passive modes of operation. The leakage current in short channel nanometer transistors has several forms, such as reverse biased diode leakage, subthreshold leakage, gate oxide tunneling current, hot carrier gate current, gate induced drain leakage (GIDL) and channel punch-through current (Roy *et al.* 2003). The reverse biased diode leakage current and gate oxide tunneling current flow during both active and sleep modes of the circuit, whereas other currents flow during the sleep mode only (Mohanty and Kougianos 2006).

According to the Semiconductor Industry Association International Technology Roadmap for Semiconductors (ITRS), high performance CMOS circuits will require very low gate oxide thicknesses due to aggressive technology scaling. Such ultra-thin oxide devices will be susceptible to new leakage mechanisms due to carrier tunneling through the gate oxide layer, which leads to gate oxide current, I_{ox} (Sultania *et al.* 2004). It is projected that the gate oxide tunneling current will be a major component of the static power consumption and hence that of the total power consumption of a low-end nano-CMOS device. Thus, there is a critical need for analysis, explanation, and

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characterization of the various tunneling mechanisms, targeted towards design for manufacturing (DFM) and process variation modeling.

The gate oxide tunneling current is strongly dependent on the supply voltage of the transistor V_{DD} and gate SiO_2 thickness T_{ox}. For given supply voltage V_{DD} and oxide thickness T_{ox}, the tunneling current leakage in a CMOS can be described as (Kim *et al.* 2003, Chandrakasan *et al.* 2001, Mohanty and Kougianos 2006):

$$I_{ox} \propto \left(\frac{V_{DD}}{T_{ox}}\right)^2 \exp\left(-\gamma \frac{T_{ox}}{V_{DD}}\right), \quad (1)$$

where γ is an experimentally derived factor. This explains the fact that a small change in T_{ox} can have a tremendous impact on gate oxide current. Moreover, it is a fact that when T_{ox} is ultra thin, it is extremely difficult to maintain a constant T_{ox} for devices in a chip due to variations in nano-CMOS process technology. During the fabrication process a displacement of very few SiO_2 molecules can cause a significant variation in T_{ox}. This leads to a difference between the desired value of T_{ox} and the actual T_{ox} value obtained after fabrication. Additionally, a change in on-chip power supply voltage can cause variation in the gate oxide tunneling current. Thus, it is necessary to study the impact of both process and design parameter variation on the tunneling current of a CMOS device.

We have performed our analysis and characterization on both NMOS and PMOS devices. For brevity, we present the results for an NMOS transistor only. The analysis procedure for both NMOS and PMOS is similar. It may be noted that as far as SiO_2 technology is concerned the PMOS tunneling current is small compared to an NMOS, but it becomes an issue in high-κ dielectrics.

The contributions of this paper are as follows:

- We analyze in detail the behavior of a nano-CMOS device during an entire cycle of its operation.
- Guided by the results of the previous analysis and using additional simulations, we define three novel metrics, I_{ON}, I_{OFF} and C_{eff}^t, appropriate for a complete characterization of the gate oxide tunneling current of a CMOS transistor and its impact on device operation as far as leakage and capacitive effects are concerned.
- We evaluate the statistical dependence of the proposed metrics on process parameter gate oxide thickness (T_{ox}) and design parameter power supply (V_{DD}) variations.

The rest of the paper is organized as follows. In section 2 we review prior works focused on gate tunneling current. In section 3 we study the dynamics of the gate tunneling current mechanism during the operation of an NMOS and define appropriate metrics. In

section 4 we model the statistical effects of process and power supply variations and study their impact on the proposed metrics in section 5. Finally, we conclude in section 6 with suggestions on the utility of these metrics in design and synthesis.

2. Related Work

There are several research works available in the current literature that model as well as characterize the gate oxide leakage current. This leakage current may be due to two phenomena, Fowler-Nordheim tunneling or direct tunneling (Roy *et al.* 2003). For sub-65 nm CMOS technologies, direct tunneling is the predominant mechanism. In this section, we discuss in brief some of the works that examine these tunneling phenomena and their implications for nano-CMOS technology. While the modeling works provide analytical methods for calculating the gate tunneling current, the characterization works provide statistical and Monte Carlo approaches.

Lo *et al.* (1999) provide quantum mechanical models for direct tunneling current through the ultrathin oxide of a MOS transistor. Choi *et al.* (1999) discuss a surface potential model and compact quantum mechanical models to predict direct tunneling through thin oxide. Statistical distributions of direct tunneling current and the projected limits of oxide thickness are provided by Hirose *et al.* (2000). Hou *et al.* (2001) provide a direct tunneling current calculation for holes using a modified WKB (Wentzel-Kramers-Brillouin) approximation. Choi *et al.* (2001) provide simulation based studies for gate direct tunneling including edge-direct tunneling (EDT). Maitra and Bhat (2003) propose analytical schemes to combine the channel component and the edge component of gate oxide direct tunneling current. Lee *et al.* (2004) propose a total leakage analysis method that includes gate tunneling current as well.

We observe that the above mentioned works do not consider the effect of both on and off states on gate oxide tunneling current. We will demonstrate that for low-end nano-CMOS technology both currents are comparable and one component cannot be ignored in favor of the other. In addition, the previous mentioned works investigate only steady-state conditions and do not take into account transient effects. In other words, they do not address the effect of gate tunneling current on the device power and performance when it is changing states from on to off or off to on. Finally, they do not model or characterize the gate oxide tunneling current with respect to process and design parameters or study the impact of their variation.

3. Dynamics of gate oxide tunneling

In this section we discuss the physical mechanism of gate oxide tunneling with the help of an NMOS transistor for low-end (i.e. sub-65 nm) nano-CMOS technology. We study the behavior of the tunneling current with respect to the supply voltage V_{DD}, and gate oxide thickness T_{ox}.

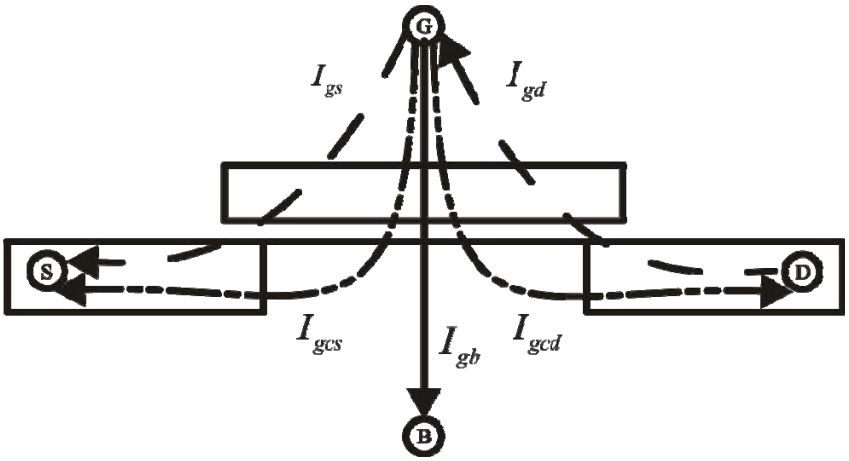


Figure 1. Gate oxide tunneling current (I_{ox}) components in the BSIM 4.5.0 model. I_{gs} and I_{gd} are the components due to the overlap of gate and diffusions, I_{gcs} and I_{gcd} are the components due to tunneling from the gate to the diffusions via the channel and I_{gb} is the component due to tunneling from the gate to the bulk via the channel. It may be noted that these components vary in magnitude as well as direction based on biasing and operating conditions of the transistor.

3.1 *Tunneling current SPICE modeling*

Figure 1 shows and identifies the various components of the gate oxide tunneling current, such as gate-to-diffusion, gate-to-channel and gate-to-substrate currents as proposed in the BSIM 4.5.0 model. Since the objective of this work is to analyze the effect of these currents in future nano-CMOS technologies, especially in the 65 nm, 45 nm and beyond range, no commercially available process data could be used. It is, however, expected that the Predictive Technology Model (PTM) accounts for these effects (Zhao and Cao 2006) correctly and has been used throughout this work. The BSIM model is used today almost exclusively for nanometer CMOS designs and its validity is widely accepted. The methodology we present in this work for the establishment and calculation of the relevant metrics is, however, model-independent. Any alternative model which accounts for gate oxide tunneling can be used and the same methodology followed.

The PTM model used in this work is for a 45 nm NMOS device with nominal $T_{ox} = 1.4$ nm and threshold voltage $V_{th} = 0.22$ V. The process is bulk CMOS with substrate tied to ground and NWELL tied to V_{DD}. Other processes such as SOI can be also characterized using this approach provided the SPICE models account for the gate tunneling mechanisms appropriate in each case. The effect of varying oxide thickness (T_{ox}) was incorporated by varying the parameter TOXE in the SPICE model deck directly. The width of the device was chosen to be very large ($W = 1$ μm), to eliminate any width-modulation effects in the following analysis. Such effects can be easily incorporated in the analysis, provided the underlying SPICE model properly accounts for them. Since we concentrate on the behavior of a single device and not a logic gate, no

capacitive or resistive load was connected to the output. In a more complex situation, where gate-level blocks would be characterized, an appropriately chosen slew rate and load would be used. In simulation tests performed using an inverter comprised of an NMOS and a PMOS, it was found that for the particular technology used in this work, a slew rate of 7×10^{-10} V/sec or higher eliminates any dependence of the calculated currents on slew rate. A purely capacitive load will have no effect on the slew rate but a mixed RC loading circuit will. Due to lack of physical data on typical interconnect resistivity at the 45 nm technology node, we chose to characterize the device without load. In addition, gate depletion and activation effects are not taken into account due to the fact that BSIM4 does not model them.

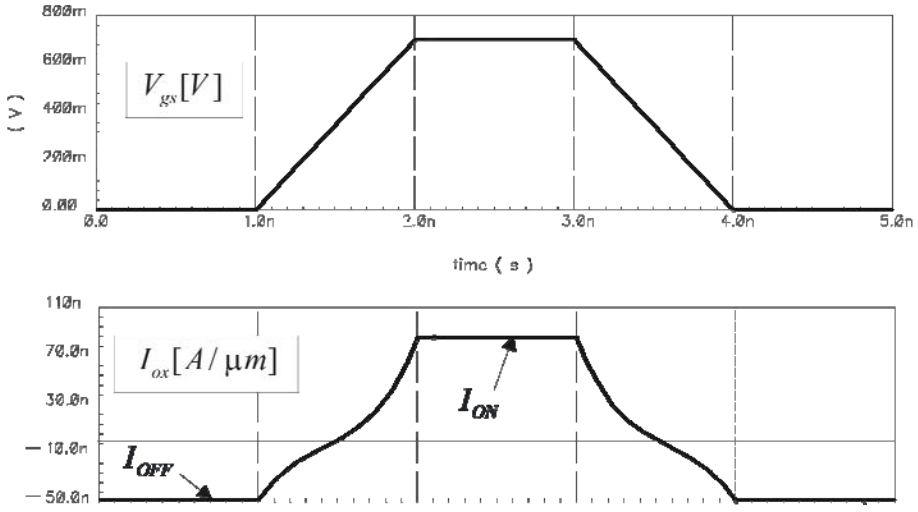


Figure 2. Gate oxide tunneling current (I_{ox}) calculated using the BSIM 4.5.0 model for a test input pulse. Indicated are the steady-state on and off currents (I_{ON}, I_{OFF}). The rise and fall times of the input pulse are $t_r = t_f = 1$ ns.

Cadence Design Systems' Analog Design Environment and Spectre circuit simulator were used for the analog simulations in this work. The supply voltage is initially held at $V_{DD} = 0.7$ V. We characterized the gate direct tunneling current by evaluating all components (source, drain and bulk, as shown in figure 1) from the BSIM 4.5.0 model during the switching operation of the transistor from the off to the on state and then back to the off state. The results, shown in figure 2, clearly demonstrate that gate leakage currents in both on and off states are quantitatively comparable and there is significant leakage during state transitions.

3.2 *Tunneling current physical mechanism in steady-state and during state transitions*

We now study the physical mechanism of the gate oxide tunneling in a nano-CMOS transistor. We identify the regions of operations of a MOS device distinguishing its

transition and steady states. From figure 2, we can identify four distinct regions of operation of the transistor during a typical switching cycle as listed below:

- Steady-state off region (OFF)
- Steady-state on region (ON)
- Low-to-High transition region (LH)
- High-to-Low transition region (HL)

In order to obtain a better picture of the different tunneling current components and their relative contributions to the overall gate tunneling current, we used the BSIM 4.5.0 model to evaluate them. The results are shown in figure 3 for various operating regions of the device during a complete switching cycle.

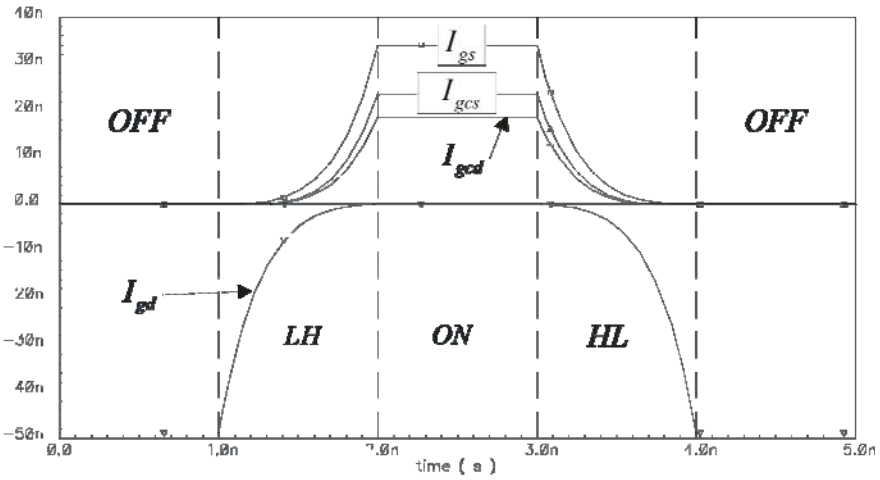


Figure 3. Gate tunneling current components calculated in the BSIM 4.5.0 model. The gate-to-source diffusion (I_{gs}) and gate-to-channel (I_{gcs} and I_{gcd}) components are positive, i.e., from the gate. The gate-to-drain diffusion component (I_{gd}) is negative, i.e., towards the gate. The gate to bulk tunneling current (I_{gb}) is negligible compared to the other currents and is not shown.

The first observation is that the gate to bulk component (I_{gb}) is negligible throughout all regions of operation and will be ignored for the remainder of this discussion. It is also clear that different mechanisms contribute to the overall current during different phases of the switching cycle. In the following discussion we refer to figure 4 which identifies the various components active during each region of operation for the NMOS device.

- *OFF region*: In the steady-state off region (figure 4(a)), both gate and source are at ground while the drain is at high (V_{DD}) voltage. Since no channel is formed in

this condition, the only active component is I_{gd}, due to the overlap of the drain diffusion and the gate.

- *ON region*: In the steady-state on region (figure 4(b)), both gate and drain are held at high with the source being grounded. A well-formed channel exists in this case and three separate components are active: (i) I_{gs} due to the overlap of the source diffusion with the gate, (ii) I_{gcs} due to the flow of current from gate to the inversion layer in the channel and subsequently to the source, and (iii) I_{gcd} due to the flow of current from gate to the channel and subsequent collection at the drain.

- *Low-to-High (LH) or High-to-Low (HL) transition region*: Finally, during the LH and HL transitions, all four components become active as evident from figures 3 and 4(c). In this case the source is at ground, the drain is at V_{DD}, and the gate is switched from low to high or high to low. In the LH transition, the channel gradually forms from source to drain and the components I_{gs}, I_{gcs} and I_{gcd} start becoming significant, in that order. Conversely, as the field across the oxide region over the drain is reduced, I_{gd} is decreasing to almost total extinction. The situation is reversed in the HL transition.

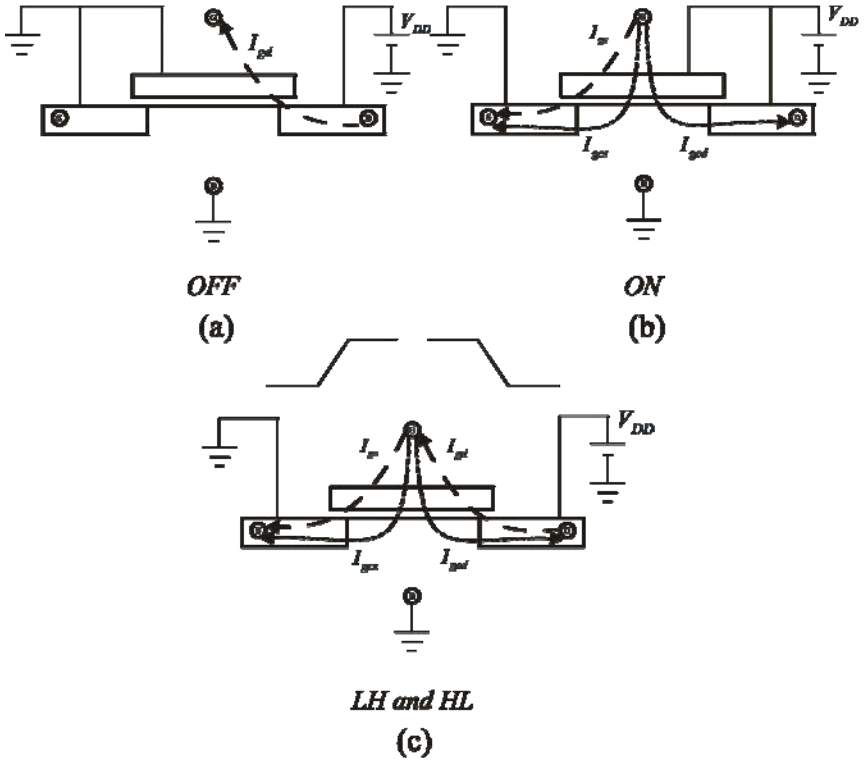


Figure 4. Gate tunneling current component flow in the various states of operation of an NMOS transistor. The gate to bulk tunneling current component (I_{gb}) is negligible compared to the other components and not shown in the figure.

3.3 *The three metrics for tunneling current*

Based on the results presented in the previous sections, it is apparent that the behavior of the device in terms of gate tunneling leakage current must be characterized not only during the on state but also during the off and LH and HL transitions as well. In particular, the off state current is comparable in magnitude to the on state current and hence a major source of leakage which needs to be accounted for in any characterization effort.

The situation is more complex during the LH and HL transitions. In order to provide a meaningful metric during this transition period, we need to account for the change in magnitude and direction of the total gate leakage current and also consider the time in which this transition takes effect. We arrive, therefore, to the following expression:

$$C_{eff}^{t} = \left| \frac{I_{ON} - I_{OFF}}{dV_g / dt} \right|, \tag{2}$$

where V_g is the voltage applied on the gate. For simplicity we will assume that the rise (t_r) and fall (t_f) times of the gate input voltage are equal, which makes the two transition regions symmetric with respect to their behavior during switching. In this case, equation (2) simplifies to:

$$C_{eff}^{t} = \left| \frac{I_{ON} - I_{OFF}}{V_{DD}} \right| t_r \, . \tag{3}$$

The three metrics presented here (I_{ON}, I_{OFF}, and C_{eff}^{t}) provide a concise and complete mechanism for characterizing the gate oxide leakage during the entire operational cycle of an NMOS. Similar metrics can be defined, of course, for PMOS devices as well as logic gates. I_{ON} has been recognized in prior works as a significant contributor to gate leakage but I_{OFF} has not received the attention it deserves as its magnitude is comparable to I_{ON}. C_{eff}^{t} is novel, proposed for the first time in this paper, and can be considered as representing the effort needed to overcome the gate leakage current for a transition from the on to the off state or vice versa. It also allows the designer to quantify the tunneling loading effect at all levels of design abstraction, from transistor to architectural block. In addition, we believe that C_{eff}^{t} contains valuable information not only for the switching operation of the device but for reliability studies since it can be directly related to transient charge flow through the gate oxide. A design engineer can use C_{eff}^{t} to calculate

the average amount of charge through the gate oxide due to tunneling and hence its impact on device lifetime. Thus, an early characterization which delivers information on these three metrics provides invaluable information to the designers in order to accurately estimate power and performance losses due to gate tunneling leakage.

Which particular metric will be used at a given situation will depend on the particular aspect of gate leakage the design engineer is interested in exploring. For active leakage I_{ON} would be appropriate while for off state leakage I_{OFF} would be utilized, in addition to subthreshold leakage. C_{eff}^{t} will have an additive effect to the net switching capacitance and, consequently, to the dynamic power dissipation.

Finally, we should point out that these three metrics, at the device level, can be used in a transistor macromodel to ease the amount of computational time in large designs in which gate leakage is anticipated to have a significant impact. While BSIM4 calculates the gate leakage currents directly, it is considerably more intensive on computational resources than BSIM3. BSIM3 does not include gate tunneling mechanisms. A macromodel consisting of a BSIM3 device, a voltage controlled current source (modeling I_{ON} and I_{OFF}) and a capacitance (C_{eff}^{t}) can model the leakage effects in a fraction of the simulation time used by a full BSIM4 model.

4. Modeling of process and power supply variation

In this section, we studied the effect of gate oxide thickness (T_{ox}) and power supply variation (V_{DD}) on the proposed metrics. To further elucidate the behavior of the total gate leakage current due to tunneling and in order to arrive at physically meaningful metrics to characterize these effects, we also performed a least squares fit of the data obtained to functional equations in order to quantify this information. The results are shown in table 1.

4.1 *Modeling for T_{ox} variation*

Initially, we held the power supply fixed at $V_{DD} = 0.7\,\mathrm{V}$ and varied the oxide thickness from $T_{ox} = 1\,\mathrm{nm}$ to $T_{ox} = 2\,\mathrm{nm}$. The simulation results are shown in figure 5(a). In the same figure we also display the dependence on T_{ox} of the calculated quantity C_{eff}^{t} (effective tunneling capacitance).

From the first three rows of table 1, we observe that all three metrics obey equation (1) extremely well as evidenced by the high correlation coefficients of the fit (99.9% or better). In addition, the exponential fitting factor β is identical in all three metrics, as expected from the theoretical analysis (Kim *et al.* 2003, Chandrakasan *et al.* 2001) leading to equation (1) and the definition of C_{eff}^{t}, equation (2).

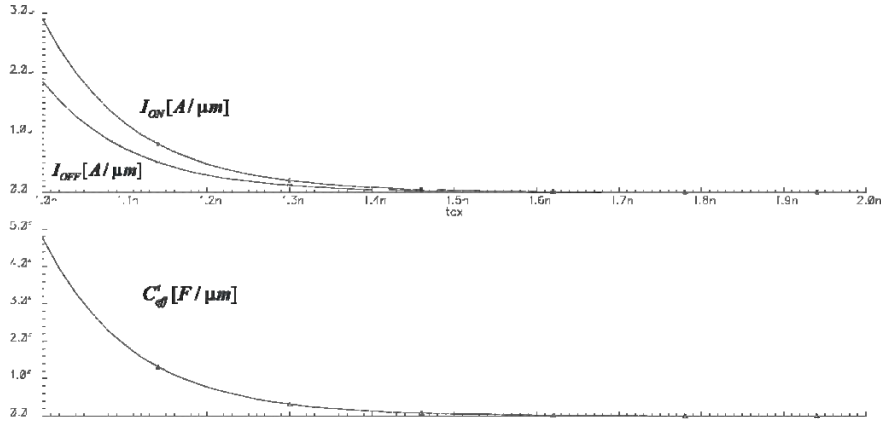
Table 1. Curve fitting using different functions.

Variation	Metrics	Fitting functions	Function parameters	Correlation coefficients
Process Parameter (T_{ox})	I_{ON} vs. T_{ox}	$I_{ON} = \left(\frac{\alpha}{T_{ox}^2}\right)\exp(-\beta T_{ox})$	$\alpha = 3.89\times10^{-21}$ $\beta = 7.2\times10^{9}$	99.9%
	I_{OFF} vs. T_{ox}	$I_{OFF} = \left(\frac{\alpha}{T_{ox}^2}\right)\exp(-\beta T_{ox})$	$\alpha = 2.55\times10^{-21}$ $\beta = 7.2\times10^{9}$	99.9%
	C_{eff}^{t} vs. T_{ox}	$C_{eff}^{t} = \left(\frac{\alpha}{T_{ox}^2}\right)\exp(-\beta T_{ox})$	$\alpha = 6.86\times10^{-30}$ $\beta = 7.2\times10^{9}$	100%
Design Parameter (V_{DD})	I_{ON} vs. V_{DD}	$I_{ON} = (\alpha V_{DD})\exp\left(\frac{-\beta}{V_{DD}}\right)$	$\alpha = 1.19\times10^{-6}$ $\beta = 1.29$	99.5%
	I_{OFF} vs. V_{DD}	$I_{OFF} = (\alpha V_{DD})\exp\left(\frac{-\beta}{V_{DD}}\right)$	$\alpha = 6.43\times10^{-7}$ $\beta = 1.29$	99.5%
	C_{eff}^{t} vs. V_{DD}	$C_{eff}^{t} = (\alpha V_{DD})\exp\left(\frac{-\beta}{V_{DD}}\right)$	$\alpha = 1.78\times10^{-15}$ $\beta = 1.29$	100%

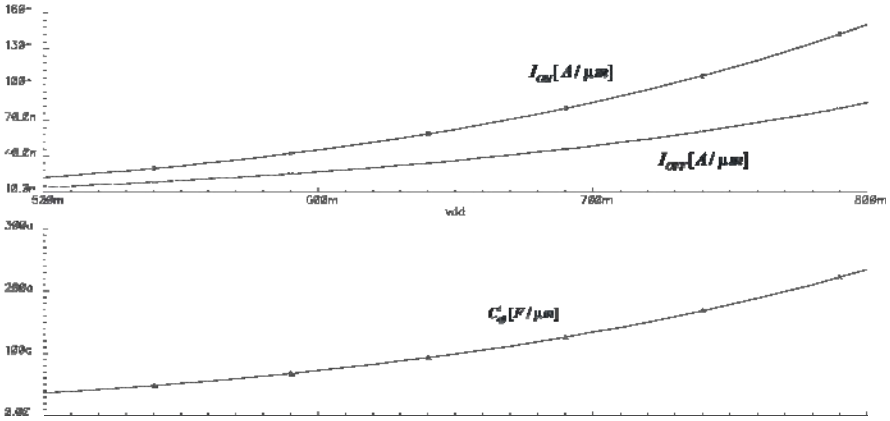
4.2 *Modeling for V_{DD} variation*

We held T_{ox} to a nominal value of 1.4 nm, and investigated the dependence of the currents and C_{eff}^{t} on power supply variation. At supply voltages below 1.0 V, on-chip supply variation is expected to be significant, which makes a study of the variation of the metrics with respect to V_{DD} important. The results are shown in figure 5(b).

Similarly, the last three rows of table 1 indicate an almost perfect fit of the metrics to equation 1 and an identical exponential fitting factor β. It may be pointed out that the fitting factors α and β for a given metric are different for the T_{ox} and V_{DD} fits. The reason for this is that we look at two separate curve fitting procedures: one keeping V_{DD} constant and the other keeping T_{ox} constant. We believe that this is more flexible than performing a simultaneous T_{ox}, and V_{DD} fit as we can isolate the effects of each factor separately.



(a) Dependence on T_{ox}. The power supply is held fixed at $V_{DD} = 0.7\,\text{V}$.



(b) Dependence on V_{DD}. The oxide thickness is held fixed at $T_{ox} = 1.4\,\text{nm}$.

Figure 5. Dependence of steady-state on current (I_{ON}), steady-state off current (I_{OFF}) and effective tunneling capacitance (C_{eff}^{t}), on oxide thickness (T_{ox}) and power supply (V_{DD}). It is evident that the dependence is exponential.

5. Statistical distribution of the proposed metrics

Our ultimate objective in determining a functional relationship between the metrics and T_{ox} and V_{DD} is to translate statistical information for the distributions of T_{ox} and V_{DD} to statistical information about the metrics themselves. In order to obtain this distribution analytically, the equation relating the metrics to the variables must be invertible. Since this is not feasible in our case due to the complex functional dependence on the process and design parameters, we perform a statistical characterization of the devices using a Monte Carlo approach.

In the Monte Carlo method followed here, we assume that the statistical distribution of process (T_{ox}) and on-chip power supply factors (V_{DD}) is known. A similar procedure can be followed for any of the parameters in the design, process or BSIM 4.5.0 model. For both variables we use a normal distribution with standard deviation (σ) equal to 10% of the mean (μ). The mean value for T_{ox} was 1.4 nm and for V_{DD} was 0.7 V.

Using these distributions, a statistical sample of N (T_{ox},V_{DD}) pairs was generated and N simulations were performed with each pair being used only once. These simulations resulted in N triplets of (I_{ON}, I_{OFF}, C_{eff}^{t}) metrics which were subsequently processed to generate frequency plots. These results indicate that even though approximately 65% of the metrics follow the mean very closely, a significant number of them fall within the range from 2 σ to 3 σ of the mean. In addition, the distribution is lognormal, as expected in view of equation (1), and σ is almost 1.8 times the value of the mean. The results and least square fit estimates of the mean and σ for $N=1000$ simulations are shown in figure 6.

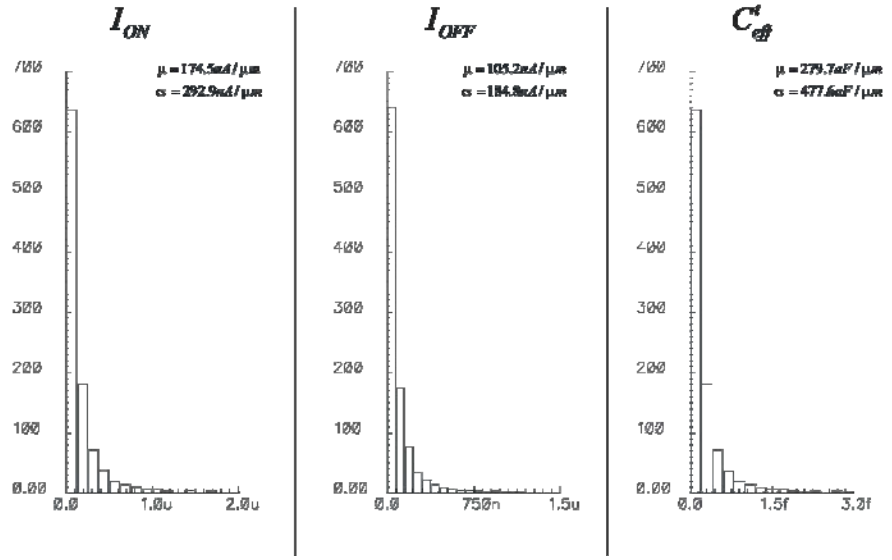


Figure 6. Monte Carlo simulation results for I_{ON}, I_{OFF} and C_{eff}^{t}. A total of $N=1000$ simulations were performed. The vertical axis corresponds to the number of runs falling within a certain bin. The numbers at the top right corner of each graph correspond to the mean and standard deviation of the best fit lognormal distribution.

In summary, a small (10%) variation in process and supply parameters can influence the gate oxide tunneling current metrics significantly. This influence can be manifested by metrics that are two or more times the mean value. Clearly this wide distribution must be taken into account in the design and synthesis of next generation integrated circuits.

7. Conclusions

We presented a comprehensive analysis of the various gate oxide tunneling current components present during the entire switching cycle of an NMOS for a realistic 45 nm model and used this information to identify metrics for the characterization of the tunneling effect.

A study of these metrics reveals that not only the on cycle but the off as well as switching cycles must be accounted for, and towards this objective, we introduced the metrics I_{ON}, I_{OFF}, *and* C_{eff}^{t}.

Further analysis of the dependence of these metrics on gate oxide thickness and power supply variation reveals that the BSIM 4.5.0 equations correctly predict the qualitative and quantitative behavior of these metrics. This methodology can provide valuable information and estimates for the effect of gate tunneling leakage on power consumption and delay which can then be used to characterize entire cells and libraries leading ultimately to optimized synthesis algorithms for nano-CMOS circuit design.

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