

# Design of Parasitic and Process-Variation Aware Nano-CMOS RF Circuits: A VCO Case Study

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**Abstract**—This paper proposes a novel flow for parasitic and process-variation aware design of radio-frequency integrated circuits (RFICs). A nano-CMOS current-starved voltage controlled oscillator (VCO) circuit has been designed using this flow as a case study. The oscillation frequency is considered as the objective optimization function with the area overhead as constraint. Extensive Monte Carlo simulations have been carried out on the parasitic extracted netlist of the VCO to study the effect of process variation on the oscillation frequency. In the design cycle, a performance degradation of 43.5% is observed when the parasitic extracted netlist is subjected to worst-case process variation. The proposed design flow could bring the oscillation frequency within 4.5% of the target, leading to convergence of the complete design in only one design iteration. To the best of the authors' knowledge, this paper presents the first work focussed on a current starved VCO in which the combined effect of parasitics and process variations has been considered.

**Index Terms**—Nano-CMOS, Process Variation, Monte Carlo

## I. INTRODUCTION AND MOTIVATION

The fluctuation of device characteristics caused by process variation has considerably increased in the nanoscale regime. Process variations can be classified into inter-die and intra-die [1]. Inter-die variation, which comes from lot-to-lot, wafer-to-wafer, and within wafer, affects every device on a single chip equally. Intra-die variation refers to device characteristics such as device geometry change, dopant density change, threshold voltage, gate-oxide thickness and circuit timing change that vary from device to device within the same die. Capturing and modeling the intra-die process variation becomes essential to device and interconnect extraction tools for accurate timing and power analysis. The circuit's parasitics also cause degradation in performance. In other words, parasitics along with process variation can lead to severe degradation in circuit performance. The design cycle must include process variations along with parasitics to produce variation-tolerant circuits.

When RFIC components are designed assuming ideal components, it is observed that parasitics have serious degrading effects at high frequencies. The only way to overcome these effects is to consider parasitics as an integral part of the circuit. This motivates the essential need for parasitic-aware design and optimization. If parasitics have an acute effect on the design, as in a VCO, an early layout needs to be created so

that the parasitics can be extracted and their effect estimated. Without that early layout-parasitic information, designers rely mostly on experience. If a design is understood well enough to know the sensitive nodes, dummy elements can be placed on those nodes to mimic the effect that real parasitics will have. This process is tedious and error-prone. Therefore a methodology is required which can achieve the required performance while accounting for the parasitics.

The aim of this paper is to present a design methodology accounting for parasitics and process variation of general RFIC components, using a VCO as a case study. The oscillation frequency of VCOs is one of the most critical performance parameters and hence considered as the optimization objective.

Different oscillator topologies have been examined in [2]. The authors in [3] have studied high performance designs using CMOS processes. The design issues faced by low-power VCOs have been addressed in [4]. Issues related to parasitic aware design to overcome degradations due to device and package parasitics have been addressed in [5]. Simulated annealing heuristics have been used to implement a parasitic-aware optimization technique for CMOS RF circuits [6], [7]. In [8], an LC VCO is subjected to parasitic-aware synthesis.

## II. THE PROPOSED NOVEL RFIC DESIGN FLOW

The logical design of a 90nm nano-CMOS VCO has been done and its frequency-voltage characteristics are recorded. The physical design of this VCO follows and its frequency-voltage characteristics are recorded. Due to parasitics, the frequency-voltage characteristics of the physical design show a large discrepancy compared to the logical design (Fig. 1). Monte Carlo simulations on the parasitic extracted netlist of the VCO determines the effect of process variations on its oscillation frequency. The bottom-most curve in Fig. 1 shows further increase in the discrepancy between the logical and physical design.

In a standard RFIC design flow, multiple iterations between the front-end circuit design and back-end layout are required to achieve parasitic closure. Such a manual approach requires X number of iterations, where X is a natural number. To have a process-variation robust design accounting for parasitics, we propose a “new parasitic and process-variation aware RFIC design flow” shown in Fig. 2. The goal of the proposed design flow is to reduce the number of manual iterations to 1, by performing the X number of iterations on a parasitic parameterized netlist instead of the layout. The parasitic-parameterized netlist refers to the netlist derived from the

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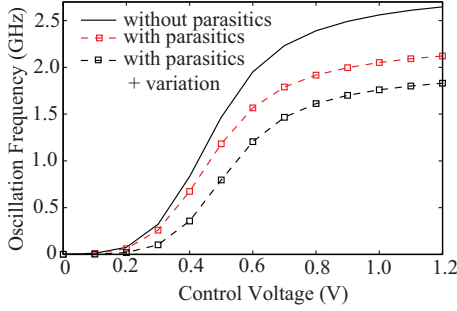


Fig. 1. Comparison of unoptimized frequency-voltage characteristics for: (1) the logical design, (2) parasitic extracted physical design, and (3) parasitic extracted physical design subjected to worst-case process variation.

initial physical design and then parameterized for optimization in  $X$  automatic iterations. The final physical design is done using the parameters obtained from the netlist optimized for a worst case process variation. This constitutes 1 iteration. Hence, the *novel flow reduces the  $X$  number of manual iterations required for parasitic closure, to 1 manual iteration.* This flow ensures that the final physical design is not only resistant to parasitic effects, but also process-variation tolerant.

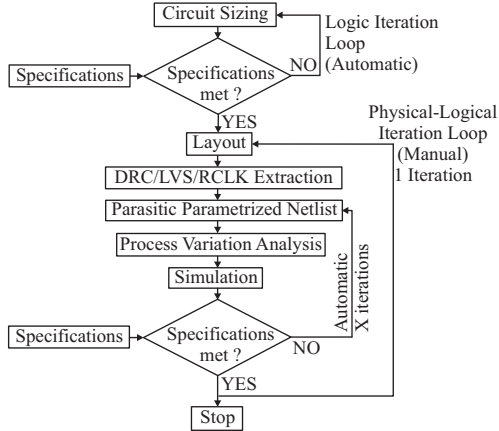


Fig. 2. Proposed parasitic and process-variation aware RFIC design flow.

This is a novel methodology for the physical design of Nano-CMOS RF components to meet required design specifications. In this procedure, a 1 iteration approach is followed, in which the layout has to be done manually only twice. Once before the optimization, and once, with minor modifications, after the optimization. The fully extracted physical design consisting of resistors ( $R$ ), capacitors ( $C$ ), inductors ( $L$ ), and mutual inductors ( $K$ ) is optimized to meet the target specification.

### III. VCO CASE STUDY

#### A. Logical Design of the VCO

We consider the current starved type of VCO, as other designs require large resistors and capacitors consuming large silicon area. The circuit consists of two input stage transistors with high impedance, an odd numbered chain of inverters

along with two current source transistors per inverter, which limit (starve) the current flow to the inverter [9].

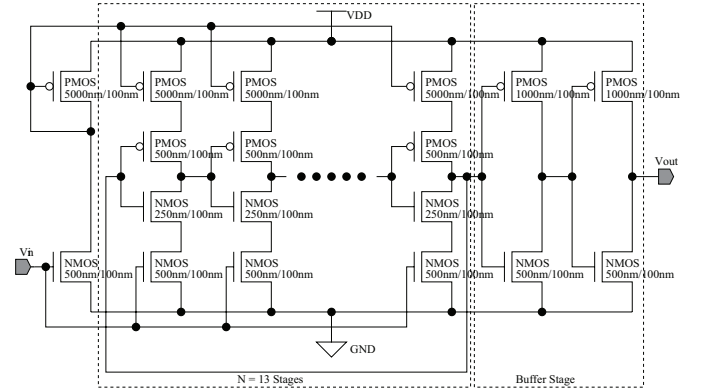


Fig. 3. Nominal case logical design of the voltage controlled oscillator.

For determination of the oscillation frequency, we calculate the total capacitance ( $C_{TOT}$ ) on the drain of the inverter [10]:

$$C_{TOT} = C_{out} + C_{in} = \left(\frac{5}{2}\right) \times C_{ox} \times (W_p L_p + W_n L_n), \quad (1)$$

where  $C_{ox}$  is the gate oxide capacitance per unit area,  $W_n$  and  $W_p$  are the widths and  $L_n$  and  $L_p$  are the lengths of the inverter NMOS and PMOS transistors, respectively. The gate oxide capacitance per unit area  $C_{ox}$  is calculated as  $(\epsilon_{ox}/T_{ox})$  with gate-oxide thickness  $T_{ox}$ . The total time required to charge and discharge the capacitance of an inverter stage is:

$$T = C_{TOT} \times \left(\frac{V_{DD}}{I_D}\right). \quad (2)$$

The operating frequency of the VCO can be determined using this simple capacitance charging estimate [10]:

$$f_0 = \left(\frac{1}{N \times T}\right) = \left(\frac{I_D}{N \times C_{TOT} \times V_{DD}}\right), \quad (3)$$

where  $V_{DD}$  is the supply voltage,  $I_D$  is the current flowing through the inverter, and  $N$  is the odd number of inverters in the VCO circuit. Hence, the oscillation frequency is determined by the number of inverters, size of the transistors in the circuit, and the current flowing through the inverter ( $I_D$ ), which is determined by the input voltage to the VCO.

The oscillation frequency is the functional specification for the design. The target oscillation frequency is kept at  $2GHz$  for this design. To meet high frequency requirements and an area optimal design, the number of stages ( $N$ ) is fixed to 13. Minimum sized transistors have been used to design the inverters. The length is kept constant for all devices. Hence, the drawn lengths and widths are  $L_n = L_p = 100nm$ ,  $W_n = 250nm$  and  $W_p = 2 \times W_n = 500nm$ . Choosing minimum width transistors also ensures an area optimal design.  $C_{TOT}$  is calculated using these values. The  $I_D$  requirement is calculated for the desired  $f_0$  and the current starved NMOS and PMOS devices are sized to provide this required  $I_D$ . Thus, we obtained  $L_{ncs} = L_{pcs} = 100nm$ , and  $W_{ncs} = 500nm$  and  $W_{pcs} = 10 \times W_{ncs} = 5\mu m$ , where  $W_{ncs}$  and  $W_{pcs}$  are the widths and  $L_{ncs}$  and  $L_{pcs}$  are the lengths of the current-starved NMOS and PMOS transistors,

respectively. The minimum sizes of transistors needed for successful operation are obtained using Eqns. (1) - (3).

### B. Performance Optimization of the VCO

1) *Variability Analysis*: The oscillation frequency shows strong dependence on  $V_{DD}$ , threshold voltage of the CMOS  $V_T$  (as  $I_D$  depends on  $V_T$ ), and gate oxide thickness  $T_{ox}$ . Hence any variation in these process ( $V_T$ ,  $T_{ox}$ ) parameters and supply ( $V_{DD}$ ), would lead to a degradation in the oscillation frequency.

For the VCO, the parameters identified for variation are: supply voltage ( $V_{DD}$ ), threshold voltage of NMOS transistors ( $V_{T_{nm}}$ ), threshold voltage of PMOS transistors ( $V_{T_{pm}}$ ), gate-oxide thickness of NMOS transistors ( $T_{ox_{nm}}$ ), and gate-oxide thickness of PMOS transistors ( $T_{ox_{pm}}$ ). Statistical variations in the device parameters, each assumed to be Gaussian (with a mean  $\mu$  as nominal technology-driven value and a standard deviation  $\sigma$  as 10%), are explicitly taken into account by using Monte Carlo simulations. The effects on  $f_0$  are observed for 5 cases: (a) only  $V_{DD}$  variation, (b) only  $V_{T_{nm}}$  variation, (c) only  $V_{T_{pm}}$  variation. (d) simultaneous  $T_{ox_{nm}}$  and  $T_{ox_{pm}}$  variation, and (e) simultaneous  $V_{DD}$ ,  $V_{T_{nm}}$ ,  $V_{T_{pm}}$ ,  $T_{ox_{nm}}$  and  $T_{ox_{pm}}$  variation.

For cases (a)-(c), Gaussian statistical distributions with standard deviation  $\sigma = 10\%$  of the mean are considered for the parameters. 100 Monte-carlo runs are performed per experiment. In each case, the oscillation frequency followed a Gaussian distribution as shown in Fig. 4(a), 4(b), and 4(c). For case (d), we have considered simultaneous variation of  $T_{ox_{nm}}$  and  $T_{ox_{pm}}$  with a correlation coefficient of 0.9 and a Gaussian distribution for both with  $\sigma = 10\%$ . This is due to that fact that in a typical CMOS process, the gate oxides of NMOS and PMOS transistors are grown together [10]. 100 Monte Carlo runs are considered and the oscillation frequency follows a Gaussian distribution as shown in Fig. 4(d). For case (e), a total of 1000 Monte Carlo runs are considered for simultaneous variation of all 5 parameters with  $\sigma = 10\%$ . The resulting Gaussian distribution of  $f_0$  is shown in Fig. 4(e). The value of mean ( $\mu$ ) and standard deviation ( $\sigma$ ) of the oscillation frequency for all 5 cases has been presented in Table I. It can be seen that  $f_0$  shows greater dependence on  $V_{DD}$  and  $V_{T_{nm}}$  (value of  $\sigma$  is greater), as compared to  $V_{T_{pm}}$ ,  $T_{ox_{nm}}$  and  $T_{ox_{pm}}$ .

TABLE I

EFFECT OF PROCESS VARIATIONS ON OSCILLATION FREQUENCY ( $f_0$ )

Parameter	Mean ( $\mu$ )	Standard Deviation ( $\sigma$ )
$V_{DD}$	1.54GHz	77.9MHz
$V_{T_{nm}}$	1.57GHz	68.2MHz
$V_{T_{pm}}$	1.56GHz	19.7MHz
$T_{ox_{nm}} + T_{ox_{pm}}$ (cc = 0.9)	1.56GHz	20.8MHz
The 5 parameters together	1.54GHz	103.5MHz

#### 2) Parasitic and process variation aware optimization:

A 22% discrepancy in the oscillation frequency has been observed between the logical and fully-extracted (RCLK)

physical design. The parasitic parameterized netlist derived from this initial physical design is then subjected to process and supply variation where  $V_{DD}$ ,  $V_{T_{nm}}$ ,  $V_{T_{pm}}$ ,  $T_{ox_{nm}}$ , and  $T_{ox_{pm}}$  are varied by  $\pm 10\%$  from their nominal values. The worst case is identified as the one in which  $V_{DD}$  is reduced by 10%, and all the process parameters are increased by 10%. In this case, a 43.5% discrepancy was observed in the oscillation frequency of the logical and physical designs. The results are summarized in Table II for worst-case process variations.

TABLE II

FREQUENCY DISCREPANCY FOR A TARGET FREQUENCY  $\geq 2GHz$ 

Parameter	Unoptimized Physical Design	Unoptimized Physical Design, Process Variation	Optimized Physical Design, Process Variation
Frequency	1.56GHz	1.13GHz	1.91GHz
Discrepancy	22%	43.5%	4.5%
$V_{DD}$	1.2V (nominal)	1.08V (-10%)	1.08V
$V_{T_{nm}}$	0.1692662V (nominal)	0.186193V (+10%)	0.186193V
$V_{T_{pm}}$	-0.1359511V (nominal)	-0.149546V (+10%)	-0.149546V
$T_{ox_{nm}}$	2.33nm (nominal)	2.563nm (+10%)	2.563nm
$T_{ox_{pm}}$	2.48nm (nominal)	2.728nm (+10%)	2.728nm

The *initial values* of various attributes are: (i) Target oscillation frequency  $f_0^i = 2GHz$ . (ii) Logical design oscillation frequency  $f_{0,logical}^i = 1.95GHz$ . (iii) Physical design oscillation frequency  $f_{0,physical-nominal}^i = 1.56GHz$ . (iv) Physical design oscillation frequency in a worst case process variation environment  $f_{0,physical-variations}^i = 1.13GHz$ .

The objective is to achieve an oscillation frequency of 2GHz with a minimum number of layout iterations. The parasitic parameterized netlist generated from the first layout step is subjected to conjugate gradient optimization [11] where the design variables are varied to achieve the required oscillation frequency in a worst case process variation scenario. The design variables are the constraints for the methodology. The set of design variables used for optimization are: (i) Widths of NMOS devices in the inverter ( $W_n$ ). (ii) Widths of PMOS devices in the inverter ( $W_p$ ). (iii) Widths of NMOS devices in the current-starved circuitry ( $W_{ncs}$ ). (iv) Widths of PMOS devices in the current-starved circuitry ( $W_{pcs}$ ). (v) Lengths of all devices ( $L_n = L_p = L_{ncs} = L_{pcs} = L$ ).

The *final-optimal values* obtained for the design variables are recorded in Table III. The physical design of the VCO is then realized using these parameter values, and the following results are obtained: (i) Target oscillation frequency  $f_0 = 2GHz$ . (ii) Logical design oscillation frequency  $f_{0,logical} = 1.95GHz$ . (iii) Parasitic and process-variation aware physical design oscillation frequency in a nominal case process environment  $f_{0,physical-nominal} = 2.54GHz$ . (iv) Parasitic and process variation aware physical design oscillation frequency in a worst case process variation environment  $f_{0,physical-variations} = 1.91GHz$ . Fig. 5 shows the frequency-voltage transfer curves for the logical and physical designs

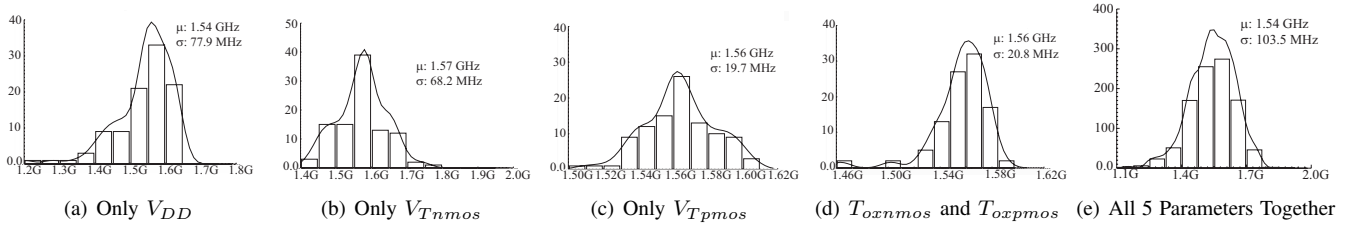


Fig. 4. Impact of statistical variations of different device parameters ( $V_{DD}$ ,  $V_{Tnmos}$ ,  $V_{Tpms}$ ,  $T_{oxnmos}$ , and  $T_{oxpms}$ ) on oscillating frequency.

after parasitic and process variation aware optimization.

TABLE III

OPTIMAL VALUES OF THE DESIGN VARIABLES OF THE VCO

Parameters	Varied from	Varied to	Optimal values
$W_n$	200nm	500nm	415nm
$W_p$	400nm	1 $\mu$ m	665nm
$W_{ncs}$	1 $\mu$ m	5 $\mu$ m	4 $\mu$ m
$W_{pcs}$	5 $\mu$ m	20 $\mu$ m	19 $\mu$ m
$L$	100nm	110nm	100nm

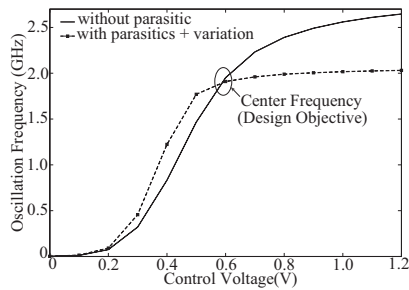


Fig. 5. Frequency-voltage transfer characteristics of the VCO optimized for design flow accounting for parasitics and process variation

3) *Physical Design of the Optimal VCO*: The physical design of the VCO is performed using a generic 90nm Salicide 1.2V/2.5V 1 Poly 9 Metal process. The final layout for the VCO is shown in Fig. 6. Multi-fingered transistors are used to minimize the area overhead. The performance summary of the VCO is given in Table IV.

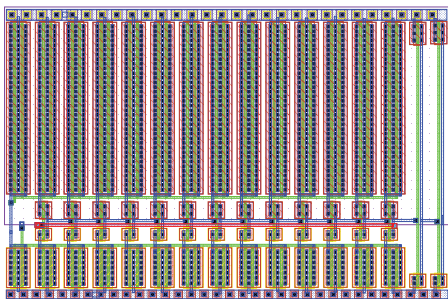


Fig. 6. Final layout of the VCO optimized using new design flow.

#### IV. CONCLUSIONS AND FUTURE WORKS

A high frequency current-starved VCO has been used as a case study for parasitic and variation aware RFIC design

TABLE IV

PERFORMANCE SUMMARY OF THE FINAL OPTIMAL VCO

Parameter	Value
Technology	90nm CMOS 1P 9M
Supply Voltage ( $V_{DD}$ )	1.2V
Nominal Oscillation Freq.	2.54GHz
Process/Supply Variations	$V_{DD}(-10\%)$ , $V_T(+10\%)$ , $T_{ox}(+10\%)$
Worst-Case Oscillation Freq.	1.91GHz
The Design Variables	5 ( $W_n$ , $W_p$ , $W_{ncs}$ , $W_{pcs}$ , $L$ )
Number of Objectives	1 ( $f_0 \geq 2GHz$ )

flow. The degradation of the oscillation frequency due to parasitic and process variation effects has been narrowed down from 43.5% to 4.5% in only one iteration of the physical design. This work may be extended for optimization of other attributes, like response linearity and phase noise. The work presented here will be beneficial for statistically robust analog design, with minimal physical redesign, thus reducing time-to-market, essential in this highly competitive age.

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