

ULS: A Dual- V_{th} /High- κ Nano-CMOS Universal Level Shifter for System-Level Power Management

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Power dissipation is a major bottleneck for emerging applications, such as implantable systems, digital cameras, and multimedia processors. Each of these applications is essentially designed as an analog/mixed-signal system-on-a-chip (AMS-SoC). These AMS-SoCs are typically operated from a single power-supply source which is a battery providing a constant supply voltage. In order to reduce power dissipation of the AMS-SoCs multiple-supply voltage and/or variable-supply voltage is used as an attractive low-power design approach. In the multiple-/variable-supply voltage AMS-SoCs the use of DC to DC voltage-level shifter is critical. The voltage-level shifter is an overhead when its own power dissipation is high. In this paper a new DC to DC voltage-level shifter is introduced that performs level-up shifting, level-down shifting, and blocking of voltages and is called Universal Level Shifter (ULS). The ULS is a unique component that reduces dynamic power and leakage of the AMS-SoCs while facilitating their reconfigurability. The system-level architectures for three AMS-SoCs, such as Drug Delivery Nano-Electro-Mechanical-System (DDNEMS), Secure Digital Camera (SDC), and Net-Centric Multimedia Processor (NMP) are introduced to demonstrate the use the ULS for system-level power management. The paper presents a design flow and an algorithm for optimal design of the ULS using dual- V_{th} high- κ technique for efficient realization of ULS. A prototype ULS is presented for 32nm nano-CMOS technology node. The robustness of the ULS design is examined by performing three types of analysis, such as, parametric, load, and power. It is observed that the ULS produces a stable output for voltages as low as 0.35V and loads varying from 50fF to 120fF. The average power dissipation of the ULS with a 82fF capacitive load is 5 μ W.

Categories and Subject Descriptors: B.7.1 [Integrated Circuits]: VLSI (very large scale integration), Advanced technologies; C.5.4 [Computer Systems Organization]: VLSI Systems

General Terms: Power Management, Analog/Mixed-Signal System-on-a-chip (AMS-SoC), Low-Power Design, Nanoscale CMOS

Additional Key Words and Phrases: System-Level Power Management, DC to DC Voltage-Level Shifter, Low-Power Design, Dual-Threshold Voltage, High- κ /Metal-Gate Nano-CMOS

1. INTRODUCTION

Real-life emerging applications including implantable systems, digital cameras, and multimedia processors are essentially designed as analog/mixed-signal system-on-chips (AMS-SoCs). Particular example of such AMS-SoCs are Drug-Delivery Nano-Electro-Mechanical Systems (DDNEMS) [Mohanty et al. 2009], Secure Digital Camera (SDC) [Mohanty et al. 2007; Mohanty et al. 2005], and Net-Centric Multimedia Processor (NMP) [Mohanty et al. 2009]. These AMS-SoCs are typically operated from a single power-supply source which is a battery providing a constant supply voltage. In order to be effective, these AMS-SoCs must have the following desired attributes: (1) low power dissipation, (2) fault tolerance, and (3) reconfigurability and field upgradability. This paper discusses the system-level power management to address low-power dissipation aspects of the AMS-SoCs.

High power dissipation is the primary bottleneck for the AMS-SoCs targeted for the portable applications. It has many side effects, such as reduction in battery life time, in-

crease in operating temperature of the system which will then require a heat transfer mechanism. In the DDNEMS, higher power dissipation has many side effects, such as reduction in battery life which may lead to frequent operating by the doctors, increase in operating temperature of the system which will then require a heat transfer mechanism affecting the portion of the body where it is implanted. Power dissipation is also important issue for the design of the NMP. In particular, when the NMP would be integrated in portable devices like mobile phones, power dissipation becomes a paramount issue. In a mobile phone, running mobile TV, the battery is the primary system constraint. Battery life is critical for the success of mobile TV. Similarly, power dissipation is an important constraint for SDC when deployed in critical applications like video surveillance in remote places.

There is need for devising integrated power management methods to reduce power consumption in these AMS-SoCs. When the AMS-SoCs are realized using nano-CMOS technology, the major components of total power dissipation are: gate-oxide leakage, sub-threshold leakage, and dynamic power [Mohanty and Kougiianos 2007; Kougiianos and Mohanty 2009; Ghai et al. 2008]. These power dissipation sources depend on supply voltage, either linearly or quadratically. Dynamic power management techniques with variable-supply voltage (variable- V_{DD}) are used for system level power reduction and multiple-supply voltage (multi- V_{DD}) is a static solution for switching power reduction in application-specific integrated circuits (ASICs).

A typical portable system is realized as a AMS-SoC while supplied with power from a single battery source. This paper discusses a special type of DC to DC level shifter, called ULS. The ULS suitable for power management and field programmability of such AMS-SoCs and can also be used as a standard cell in low-power design of ASICs. Efficient design of ULS is critical to reduce the overhead on the circuits that they are designed to serve. This paper discusses using cutting-edge technology, high- κ /metal-gate nano-CMOS for the design of the ULS. The high- κ is used to contain the gate leakage which is assisted by the use of dual- V_{th} technology to contain the subthreshold leakage. The use of high- κ serves the dual purpose of scaling of the device as well as reducing of gate leakage. Hence high- κ /metal-gate transistors serve as a good alternative to classical transistors at nano-CMOS technologies [Chau and et. al. 2000; Choi and et. al. 2002; Ghai et al. 2009].

The salient features of this paper are as follows:

- (1) Three representative reconfigurable applications are introduced, each of which can be realized as multiple supply voltage based multicore analog/mixed-signal system-on-a-chip (AMS-SoC). The key components of these representative multiple-supply voltage based AMS-SoCs are identified.
- (2) In order to serve the most pressing challenge, the power dissipation, the universal DC to DC voltage-level shifter (ULS) is introduced.
- (3) A novel design flow for energy-efficient design of a ULS circuit is proposed.
- (4) An algorithm is presented for the simultaneous power, leakage, and delay optimization of the ULS circuits.
- (5) A dual- V_{th} technique is applied to the high- κ /metal-gate the ULS circuit for its power and delay optimization.
- (6) A $32nm$ high- κ /metal-gate CMOS ULS is realized and thoroughly characterized for power dissipation, delay, and load.

The rest of this paper is organized as follows: Section 2 introduces the architecture

of representative systems along with the concept of ULS where low-power dissipation and programmability are required. Section 3 discusses the design of the ULS using high- κ /metal-gate nano-CMOS technology. Section 4 presents the optimization algorithm used for efficient design of ULS. Section 5 discusses the functional simulation and characterization of the ULS. Section 7 presents conclusions and directions for future research.

2. REPRESENTATIVE EXAMPLES OF EMERGING SYSTEMS

In this section three representative emerging systems are introduced each one of them use the ULS for power management. Each system needs different supply voltages for operation of individual components while supplied constant voltage from a battery.

2.1 Drug-Delivery Nano-Electro-Mechanical Systems (DDNEMS)

Strong interest in improving the quality of human life catalyzes research in the area of self-health management. Typical conventional drug delivery schemes suffer from many drawbacks that seriously limit their effectiveness for self-health management. NEMS are a technological solution for building miniature systems which can be beneficial in terms of safety, efficacy, or convenience [Wolbring ; Staples et al. 2006]. The goal of NEMS based drug delivery is to administer drugs in pre-determined targets and doses using implantable chips which are controlled or programmed externally through a radio frequency interface. Fig. 1 presents an architecture for the DDNEMS, the typical components of which are now discussed [Mohanty et al. 2009].

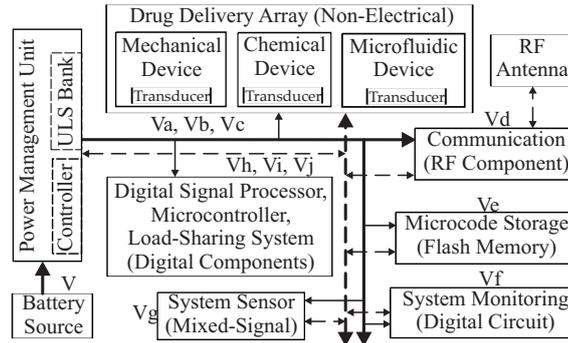


Fig. 1. The system architecture of a DDNEMS. The solid-lines represent the power buses and the dotted line the data and control buses. The modules are digital, mixed-signal, RF or non-electrical. The battery provides a constant supply voltage of V , whereas the system needs different discrete voltage levels V_a, \dots, V_j . The individual components, e.g. the digital circuits are intrinsically designed as a multiple-voltage based circuit.

Power management unit (PMU) is one of the important components of the entire DDNEMS. It manages the power distribution to the various subsystems to reduce energy consumption using the control signals from the digital signal processor (DSP) and the stored microcode. It has built-in timers that put the system to “sleep” or “wake-up” mode and can be induced to activate the system via external signals received by the RF subsystem (to force an emergency drug delivery, for example). *The heart of PMU is a ULS bank.* An ULS sends different operating voltages to various subsystems of DDNEMS each of which operate at different voltages from a single battery and facilitates reconfigurability.

The key component of the DDNEMS is the drug delivery subsystem, which is typically non-electrical in nature. To allow for redundancy, fault tolerance, load sharing and multiple drugs, the subsystem itself needs to be designed as an array. The array is expected to be heterogeneous, i.e. the elements of the array are quite diverse. The different array elements in the DDNEMS include micropumps, microfluidic devices, stents, and microneedles. The array elements have appropriate transducers to facilitate their control and interfacing to the electrical portions of the DDNEMS.

The data processing, controlling and interfacing functions of the DDNEMS are handled by electrical subsystems, which are analog, digital or mixed-signal circuits. The monitoring and control of the drug array is performed by the sensor subsystem which communicates through the transducers. Its front-end (transducer side) is analog but the back-end, interfacing to the DSP is digital. The DSP subsystem analyzes the on-line data generated by the sensors and using the program stored in the flash memory subsystem, generates control signals for drug delivery, facilitate fault tolerance, load sharing, and drug mixing. The system monitoring subsystem continually polls the various electrical subsystems and transducers to obtain a snapshot of the DDNEMS's functionalities. It alerts the DSP to initiate appropriate actions upon the discovery of faults or errors.

The RF subsystem which is comprising of an antenna and transmitter/receiver is built using RFID principles for the shape and placement of the antenna and communication protocol. Its function is to facilitate non-invasive maintenance of the system (e.g. modification of the microcode stored in the flash memory), remote collection of data (e.g. amount of drug remaining in the reservoir, drug array element failures, or battery status), and emergency drug delivery or system deactivation.

2.2 Secure Digital Camera (SDC)

Digital media transmitted or displayed through digital TV broadcast, compact disc (CD), digital-video disc (DVD), personal computers, smart phones, personal digital assistants (PDAs) offer several distinct advantages over analog media, including high-visual quality and easy processing. The ease by which a digital media is tampered give rise to the need for digital rights management (DRM) [Memon and Wong 1998; Eskicioglu and Delp 2001; Cox and Miller 2002]. Digital watermarking is used along with encryption to provide dual layer copyright protection through DRM [Eskicioglu and Delp 2001; Macq and Quisquater 1995]. Watermarking embeds extra information called a watermark into a multimedia (e.g. image, audio, video) such that the watermark can later be used to make an assertion about the host. Many software-based systems of the DRM algorithms are available, but very few attempts are made for hardware-based DRM. Hardware-based DRM is absolutely necessary for low power, real-time performance, high reliability, low cost applications, and also for easy integrability with existing consumer-electronic applications [Mathai et al. 2003; Mathai et al. 2003; Kougianos et al. 2009]. For example, DRM chips can be integrated with any digital camera [Mohanty et al. 2007; Adamo 2006; Adamo et al. 2006; Mohanty et al. 2004]. The hardware modules can also be integrated with a JPEG-codec [Mohanty et al. 2003], which can be a part of a scanner, a digital camera, or any multimedia device so that the multimedia are secured right during capture-time at the source. The high-level system architecture of the Secure Digital Camera (SDC) and its main components are shown in Fig. 2 [Mohanty et al. 2007; Adamo et al. 2006; Adamo et al. 2006; Mohanty et al. 2005].

In the SDC, the image is captured by an image sensor (aka active pixel sensor, APS) and converted to a digital signal by the analog-to-digital converter (ADC). A CMOS image

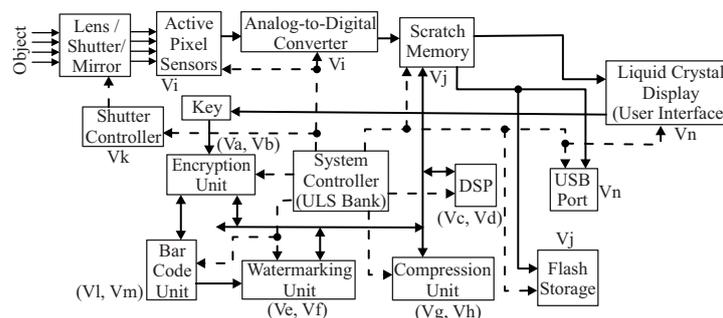


Fig. 2. System architecture of the the Secure Digital Camera (SDC). The individual units are designed to operate at discrete supply voltages V_a, V_b, \dots, V_n . The digital units are designed to operate at two discrete supply voltages. The smart controller provides the different supply voltages using the ULS bank. The solid lines represent data lines and dashed lines represent control lines.

sensor that has an embedded ADC can also be used (aka digital pixel sensor, DPS). The captured image is stored temporarily in the scratch memory, after which it is displayed on the LCD panel using the controller. The purpose of the LCD panel is to enable the user to see the image before it is processed by the watermarking or encryption units and stored in the camera, which can then be further transmitted over the network, or transferred to flash memory, computer hard drive or optical discs. The controller is responsible for co-ordinating the entire sequence of events. Both the invisible-robust and visible watermarking algorithms are used along with encryption and data compression (which is image compression unit such as JPEG). The choice of the operations performed on the image is dependent on the user of the camera. The security of image in the SDC is dependent on the encryption unit, e.g. based on the advanced encryption standards (AES) algorithm.

One of the specific application of the SDC is electronic passport [Mohanty et al. 2007; Adamo et al. 2006; Adamo et al. 2006; Adamo 2006]. The SDC can invisibly watermark biometric information, such as “iris image”, “handwritten signature”, “fingerprint” into an individual’s image, which can then be added to the passport. The watermarking is key-based and this key is encrypted and then embedded as a visible watermark in the form of a barcode on the picture image. The robustness of the invisible watermark and the authenticity of the picture image is based on the secret key. The biometric data cannot be accessed and extracted unless the secret key is known. At the same time, the secret key for the invisible watermarking process cannot be known unless it is decrypted. Hence, SDC offers double protection to the biometric data embedded into the picture image. The SDC also ensures the privacy issues pertaining to the owners of the biometric data.

Several attempts have been made for realization of different components of SDC. The trustworthy camera for restoring credibility to photographic images using encryption is presented in [Friedman 1993]. This camera produces two output files representing the captured image and the “digital signature” of the captured image. A Biometric Authentication System (BAS) in the framework of a SDC is presented in [Blythe and Fridrich 2004]; however hardware architectures are not proposed. Design for a CMOS active pixel sensor (APS) with pseudo-random number generation capability which is needed for watermarking is presented in [Nelson et al. 2005]. Industries have produced cameras with watermarking capabilities; however these camera were discontinued for unknown reasons,

e.g. Epson released the PhotoPC 3000Z and 800Z model and Kodak manufactured the DC-200 and DC-260 [Blythe and Fridrich 2004].

2.3 Net-Centric Multimedia Processor (NMP)

Information in the form of video is preferred over other forms of multimedia for combined audio-visual effects which is well supported by the significant growth of the Internet and high-bandwidth communications [Emmanuel and Kankanhalli 2003; Cherry 2005]. Video is the hardest multimedia information to deal with because it has the extensive memory and computational requirements as it is a three-dimensional signal. Video is made available and transmitted by using many video compression standards, such as MPEG-4 [Bhargava et al. 2004; Richardson 2003; Sikora 1997], H.264 [Richardson 2003], and VC-1. Thus, there is a need for a system for integrated video compression, encryption, and watermarking, which will work well with these video coding standards. Net-centric Multimedia Processor (NMP) is such a system [Mohanty et al. 2009; Tarigopula 2008]. The architecture the NMP is shown in Fig. 3 [Mohanty et al. 2009; Tarigopula 2008]. NMP has built-in facilities for real-time multimedia information security or DRM. An NMP can be integrated in any multimedia processing networked equipment (e.g., mobile phones or sensor networks) to facilitate Internet protocol (IP) packet processing and multimedia information processing without the use of a main central processing unit (CPU). NMP will be very much useful for several critical applications, like video surveillance, video over IP, and IP-TV [Cherry 2005; Jain 2005; Alfonsi 2005].

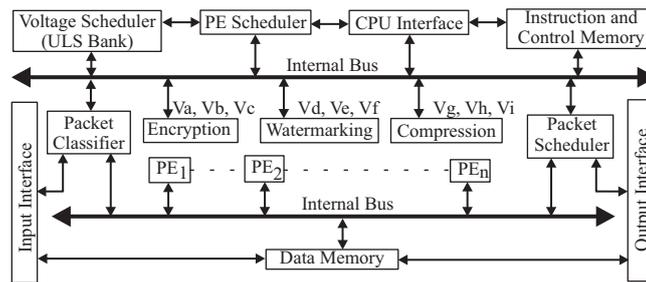


Fig. 3. High-level representation of the architecture of the NMP. PE scheduler and voltage schedulers work in coordination for reconfiguration and power management. The individual units are designed to operate at discrete supply voltages V_a, V_b, \dots, V_i .

The system of NMP consists of several processing elements (PEs), each PE with dedicated functionalities and all PEs connected through an internal bus. This bus forms the physical communication channel among the PEs as well as other components of the NMP. Packet classification is an intensive task which is carried out by the packet classifier in NMP. The packet classifier reads the header of an incoming packet, determines the stream to which the packet belongs, selects the outgoing interface, and passes the packet to the appropriate PE for further processing. The outgoing packet is dynamically buffered by the packet scheduler until it is sent to the outgoing link. The instruction and control memory is used to store the instructions corresponding to the functions that will be executed using the NMP. The data memory is used to buffer the data, and an appropriate mechanism is

needed to avoid data conflict among the PEs. Input and output interfaces are ports through which the NMP will communicate with other systems or CPU.

Real time packet classification is needed for the NMP. Design of packet classifier exploits structure and characteristics of packet classification rules [Kounavis and et al. 2003; Nourani and Faезipour 2006]. The packet scheduler is needed to control different traffic streams and to determine the streams quality [Zhang and et al. 2000]. Wide ranges of scheduling algorithms whose hardware implementation is needed for the NMP are described in [Xu and Lipton 2002]. Each PE in NMP needs can be designed to operate at a finite set of supply voltages in the range of V_1 to V_m , where m is a natural number, and V_m is the maximum supply voltage, for low power dissipation [Mohanty et al. 2006]. The PE scheduler activates and deactivates each PE, depending on the application of NMP. The inactive PEs will be shut off with a switching mechanism to reduce leakage power [Hu et al. 2004]. The ULS is specifically useful for reducing dynamic power as well as standby leakage. The voltage scheduler dynamically assigns the operating voltage of each PE depending on the traffic load and application requirements so that power and delay specifications are met. These units together form the set of units to provide real-time DRM facility in the NMP. The sequence in which they will be used depends on the application and location of the NMP in the IP network cloud. Compression unit performs one of the video compression standards such as H.264, MPEG-4, or VC-1.

2.4 Use of the ULS for Reconfiguration and Power Management

In the multi- V_{DD} AMS-SoC design, once individual units and processing elements are designed, the next issue is integrating them. The ULS is used for such integration in static or dynamic fashion. The high-level representation of the ULS is shown in Fig. 4 [Mohanty et al. 2009; Ghai et al. 2008; Mohanty et al. 2007; Vadlamudi 2007]. It has an input voltage signal called V_{in} , two control signals S1 and S0, two supply voltages V_{DDh} and V_{DDl} , and an output voltage signal V_{out} . The control signals decide which functionality is to be performed by the ULS. Depending on the control signal, the input voltage V_{in} is transformed to the output voltage V_{out} . Table I presents the truth table which defines the functionality of the ULS and can be used for programming the ULS.

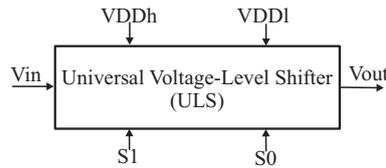


Fig. 4. High-Level Representation of the Universal Level Shifter (ULS).

Table I. Control signals for programmability or reconfiguration

Select Signal (S1, S0)	Functionality
0 0	Signal-Blocking
0 1	Level-Down Shifting
1 0	Level-Up Shifting
1 1	Signal-Passing

The ULS is capable of performing four types of operations on the voltage signal: (1) level-up shifting, (2) level-down shifting, (3) signal-passing (no shifting), and (3) signal-blocking as needed for power management in AMS-SoCs. Voltage-level up-shifting is stated as shifting of a low-voltage signal to a high-voltage level. While in contrast, voltage-level down-shifting is defined as shifting of a high-voltage signal into a low-voltage. Passing of the signal indicate bypassing the signal to the other side of the network without doing any operation on the signal. Blocking indicates completely stopping the input signal from appearing at the other side. The ULS is programmed for any of these four functionalities depending on the type of requirement.

The type of functionality to be performed is selected using the two control signals. Level-down shifting is used to provide supply to the blocks of the sub-systems which operate at lower than battery voltage. Level-up shifting is applied as an interface where lower-supply voltage cells are driving higher-supply voltage cells or to provide supply to sub-systems operating at higher than the battery voltage. The blocking feature of the ULS is used to shut-off the unused blocks of a circuit in the standby mode, thereby reducing standby leakage. The ULS is programmed according to different requirements, however, all the supporting operations may not be needed every time. A combination of two operations, for example, block and step-down is needed for dynamic power management. For static power management one operation is performed at a time where ULS is used as a single standard cell, in which case pass-signal operation is not needed. AMS-SoCs may use level-up shifting with blocking features to reduce short-circuit power and leakage power. AMS-SoC may also use level-down shifting with the blocking features to minimize switching power, in addition to standby leakage.

Fig. 5 illustrates the logical configuration using two PEs while they are operating at two different supply voltages. The explanation is logical representation of the use of ULS for multiple-supply voltage AMS-SoCs. The ULS is used for two different locations; one at the power-supply and other interfacing different voltage operating islands. The actual scenario may be different for (semi)-custom design and field-programmable-gate-array (FPGA) based design. The switch in real-life AMS-SoCs may be firmware or just control signals. The working principle of configurable architecture shown in Fig. 5 can be analyzed as follows. There are two different processing elements PE_1 and PE_2 . Each PE can be operated at any of the two different discrete voltages, V and V^- , where V is the supply voltage. In this scenario the following four configuration modes possible are as follows : (a) PE_1 operating at voltage V^- driving PE_2 operating at V , (b) PE_2 operating at voltage V^- driving PE_1 operating at V , (c) PE_1 operating at voltage V driving PE_2 operating at V^- , and (d) PE_2 operating at voltage V driving PE_1 operating at V^- . In particular, for example case (a) in Fig. 5(a), supply voltage to PE_1 comes through supply voltage level by step-down level shifting. Since PE_1 is operating at V^- and PE_2 is operating at V , step-up level shifting is needed between the two. Similarly, the case (b) in Fig. 5(b) can be analyzed in which step-down shifting provides power supply to PE_2 and step-up level shifting connects between PE_2 and PE_1 . Similarly, configurations for case (c) and case (d) can be discussed in which step-down level shifting would be necessary from the ULS. When both PE_1 and PE_2 are operated at same voltage, either both at V^- or both at V , in such case ULS does not need to perform level-shifting. The block signal unit of the ULS will be used to disconnect PE_1 and PE_2 from each other.

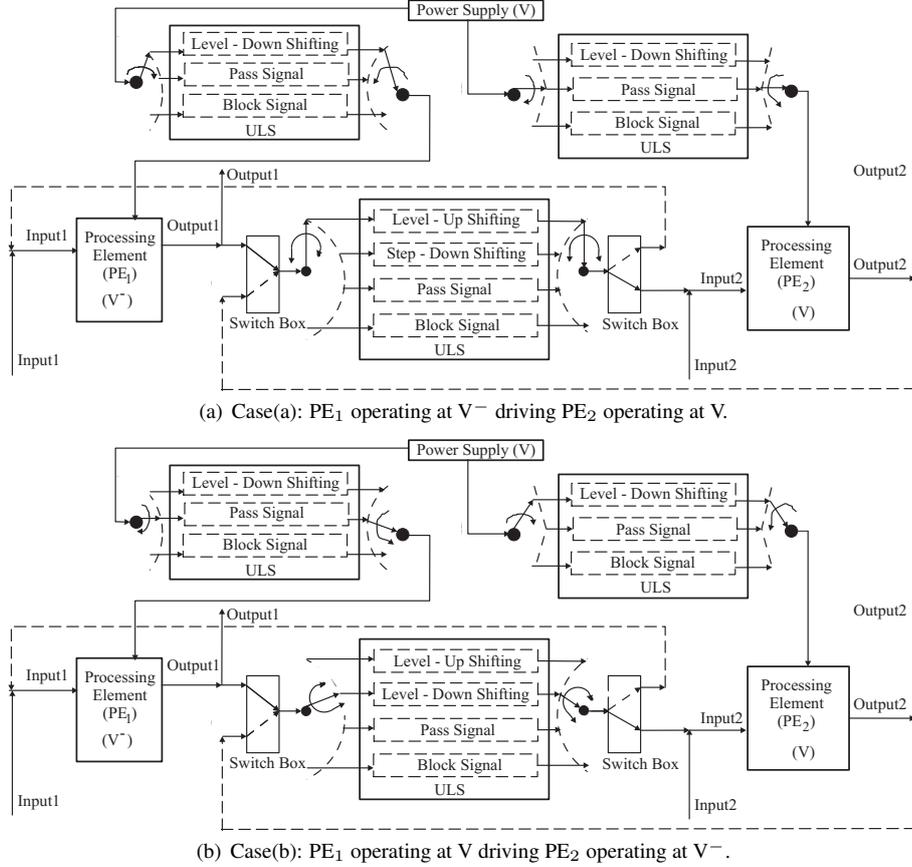


Fig. 5. System configuration for two supply voltage scenario. There are several possible cases for configurability as explained in the text. Two cases are represented, Case(a) and Case(b). In Case(a), PE₁ operating at voltage V^- driving PE₂ operating at V . In Case(b), PE₁ operating at V driving PE₂ operating at V^- . Similar configurations can be shown for all other cases of configurability. The pass-signal unit would transfer the signal without changing the voltage level, and the block-signal unit will completely disconnect signal from the PE which helps in reducing static power consumption. The solid arrow indicates signal flow and dashed arrow indicate non-flow.

3. DESIGN OF ULS USING HIGH- κ /METAL-GATE NANO-CMOS

This section discusses flow for ULS design using high- κ /metal-gate nano-CMOS technology [Mohanty et al. 2009; Ghai et al. 2008; Mohanty et al. 2007; Vadlamudi 2007].

3.1 Models for Power, and Delay Calculation of the ULS

3.1.1 Power and Leakage Models. The total power of a nano-CMOS circuit is calculated as the summation of major components, like dynamic power, subthreshold leakage, and gate leakage. The use of high- κ /metal-gate nano-CMOS transistors as technology for our design eliminates gate leakage. Thus, the power dissipation of the ULS circuit is calculated by the following expression:

$$P_{ULS} = P_{dynamic} + P_{subthreshold}. \quad (1)$$

The dynamic power dissipation of the circuit, which depends on loading conditions, is calculated as follows [Rabaey et al. 2003; Mohanty et al. 2008]:

$$P_{dynamic} = \alpha \times C_L \times V_{DD}^2 \times f, \quad (2)$$

where the α term is the activity factor, C_L is the total switched capacitive load, V_{DD} is the supply voltage and f is the clock frequency. This term is derived from the equations for energy consumed in charging and discharging a capacitor. This power dissipation depends on loading condition and not the device features.

The subthreshold leakage of a nano-CMOS device is calculated by the following expression [Sill et al. 2007]:

$$I_{sub} = \mu_0 \left(\frac{\epsilon_{gate} W_{eff}}{T_{gate} L_{eff}} \right) \times v_{therm}^2 e^{1.8} \times \exp \left(\frac{V_{gs} - V_{th}}{S \times v_{therm}} \right) \times \left(1 - \exp \left(\frac{-V_{ds}}{v_{therm}} \right) \right).$$

μ_0 is the zero bias mobility, ϵ_{gate} dielectric constant of the gate dielectric, L_{eff} is the effective channel length, V_{th} is the threshold voltage, v_{therm} is the thermal voltage, S is the subthreshold swing factor, V_{gs} is gate-to-source voltage, and V_{ds} is the drain-to-source voltage. From the above expression it is clear that if T_{gate} is increased, the length (L_{eff}) is increased, and/or the width (W_{eff}) of the transistors is reduced, there will be a reduction in the subthreshold current. This leakage current is exponentially dependent on V_{th} , and increasing V_{th} will decrease the leakage current substantially.

3.1.2 Delay Model. The delay of a CMOS circuit is approximately calculated using the follow expression [Sill et al. 2007]:

$$D = \gamma \times \left(\frac{C_L \times V_{DD}}{\mu \times \left(\frac{\epsilon_{gate}}{T_{gate}} \right) \times \left(\frac{W_{eff}}{L_{eff}} \right) \times (V_{DD} - V_{th})^\alpha} \right), \quad (3)$$

where γ is a technology dependant constant, μ is the electron surface mobility and α is the velocity saturation index, which varies from 1.4 to 2 for nano-CMOS, ϵ_{gate} dielectric constant of the gate oxide, L_{eff} is the effective channel length, and W_{eff} is the effective width of the transistors. Since in a ULS both level-up shifting and level-down shifting takes place, the average propagation delay of the ULS (D_{ULS}) is defined as follows:

$$D_{ULS} = \left(\frac{D_{up} + D_{down}}{2} \right), \quad (4)$$

assuming an equal number of level-up shifting and level-down shifting operations. D_{up} and D_{down} are the level-up-shifting and level-down-shifting delays, respectively. The delay of the ULS circuit is calculated from the 50% level of the input swing to 50% level of the output swing.

3.2 High- κ Nano-CMOS Modeling

For the design and simulation of the ULS using high- κ /metal-gate selection of appropriate transistor model is critical. It is difficult to get access to industrial standard models at this point of time. In the absence of such models, Predictive Technology Model (PTM) is used for design and simulation of the ULS [Zhao and Cao 2006]. The PTM is well established and is able to predict the general trend of device attributes and captures the physics of the devices accurately. In the absence of published data and other device models, PTM provides a timely and effective analysis approach. The simulation results obtained are highly

accurate and the calculated data are of comparable accuracy to technology-computer-aided design (technology CAD or TCAD) simulations which are typically time and computation intensive. For PTM-based BSIM4 models, either of the two methods are used [Mukherjee et al. 2005]: (1) The parameter (EPSROX) in the model card that denotes relative permittivity is changed and (2) The equivalent oxide thickness (EOT) for the dielectric under consideration is calculated. The EOT is calculated so as to keep the ratio of relative permittivity over dielectric thickness constant using the following expression:

$$T_{ox}^* = \left(\frac{\epsilon_{SiO_2}}{\epsilon_{gate}} \right) \times T_{gate}, \quad (5)$$

where ϵ_{gate} is the relative permittivity and T_{gate} is the thickness of the gate dielectric material other than SiO_2 , while ϵ_{SiO_2} is the dielectric constant of SiO_2 (= 3.9). In this paper, ϵ_{gate} is taken as 21 to emulate a HfO_2 based dielectric. The EOT is calculated to be $5nm$ for $32nm$ node.

3.3 The Design Flow Using Dual- V_{th} Based High- κ Nano-CMOS Technology

Algorithm 1 presents a design flow or optimal design of ULS using dual- V_{th} based high- κ /metal-gate technology. It may be noted that in SiO_2 based nano-CMOS technologies (particularly for sub- $65nm$ node), gate-oxide leakage is a major contributor to power during ON, OFF, and transient states of a circuit [Mohanty and Kougianos 2007]. This is overcome using the dual oxide technique, as proposed in [Ghai et al. 2008]. This is a viable solution above the $45nm$ CMOS technology node. However, at sub- $45nm$ technologies (e.g., $32nm$ in this paper), this technique is not viable, and hence bulk-CMOS must be replaced by high- κ /metal-gate CMOS. This motivates the use of the high- κ /metal-gate nano-CMOS for the design of the ULS to eliminate gate-oxide leakage.

One prominent component of the total power dissipation in the ULS circuit is the subthreshold leakage. A dual- V_{th} is adopted to reduce subthreshold leakage [Wei and et al. 1999]. A higher V_{th} in a transistor leads to lower subthreshold current, but increases the propagation delay. Hence a dual- V_{th} technique is presented for the minimization of the subthreshold leakage in the ULS circuit. The power-hungry transistors are assigned a higher- V_{th} value in this technique leaving the other transistor at nominal- V_{th} . It may be noted that while dual- V_{th} technique is well-proven in digital circuits, its use in analog circuits like ULS is distinct in this design.

The total power dissipation accounting the subthreshold leakage and delay of the entire ULS circuit are optimized using the optimization methodology; an algorithm for which is presented in Section 4. Hence, as the end result of this design flow, a thorough optimization of the ULS circuit is obtained for the use in a multi- V_{DD} circuits and systems environment.

3.4 Circuit-Level Design of the ULS

For level-up shifting, a cross coupled level converter (CCLC) shown in Fig. 6 is used. In this sub-circuit, there are two cross-coupled PMOS transistors to form the circuit load. The cross-coupled PMOS transistors act as a differential pair [Ishihara and Sheikh 2004]. Thus, when the output at one side is pulled low, the opposite PMOS transistor will be turned on and the output on that side will be pulled high. Below the PMOS load, there are two NMOS transistors that are controlled by the input signal V_{in} . The CCLC is an asynchronous level shifter. In other words, it can be inserted anywhere in the circuit wherever voltage-level shifting is necessary. Because of this flexibility, CCLC is one of the most commonly used

Algorithm 1 Power-Delay Optimal ULS Design Methodology

- 1: Design and simulate level-up shifting sub-circuit of the ULS.
- 2: Design and simulate level-down shifting sub-circuit of the ULS.
- 3: Design and simulate pass/block sub-circuit of the ULS.
- 4: Stitch the partial circuit circuits to design the complete ULS circuit.
- 5: Eliminate gate leakage power by using high- κ /metal-gate nano-CMOS technology.
- 6: Perform functional simulation of the ULS to test different functionality and programmability using different input control signals.
- 7: Perform reduce transistor design of the ULS by eliminating any redundancy in the circuit and perform functional simulations of the new circuit.
- 8: Obtain netlist of the ULS and parameterize the netlist for transistor width.
- 9: Rank the individual transistors of the ULS circuit in the order of total power dissipation accounting the subthreshold leakage.
- 10: Identify the power-hungry transistors which collectively dissipate the designer-defined percentage of total power.
- 11: Call the conjugate gradient algorithm to select optimal width for all the transistors.
- 12: Assign high- V_{th} to the power-hungry transistors to reduce the subthreshold leakage power dissipation.
- 13: Assign the new width to all the transistors of the ULS circuit.
- 14: Perform the parametric, power, and load characterization of the final ULS circuit.
- 15: Perform the process variation analysis to study robustness of final ULS circuit.

designs to suppress the DC current [Ishihara and Sheikh 2004]. This is most suitable to be used as a standard cell for multi- V_{DD} based circuit design [Mohanty et al. 2006].

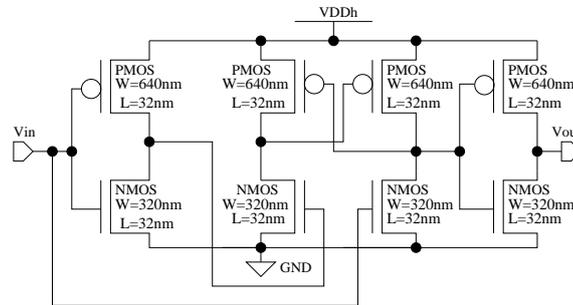


Fig. 6. Level-Up Shifting Sub-Circuit Showing Baseline Sizes for 32nm.

A differential input level shifter sub-circuit as shown in Fig. 7 is used for voltage-level down shifting. The circuit consists of a cross-coupled PMOS pair. It is similar to the voltage-level up shifting circuit. It has a differential input, which enables a stable operation at low voltage and high speed use [Kanno et al. 2000]. The differential input also offers immunity against power supply bouncing [Sanchez et al. 1999] to ensure supply of constant voltages even in tougher conditions.

The blocking circuit completely stops any voltage signal at the input side from appearing at the output side. This feature is crucial in the cases when total isolation from the input-

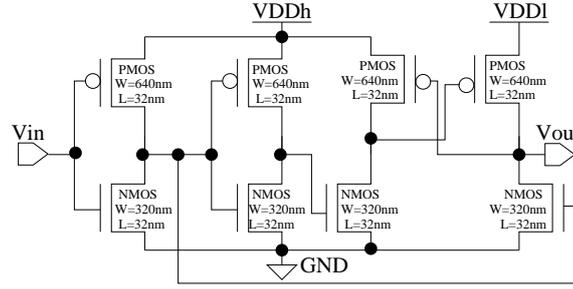


Fig. 7. Level-Down Shifting Sub-Circuit Showing Baseline Sizes for 32nm.

voltage signal is required for reduction of standby leakage power. The blocking circuit is designed by using a tristate-buffer circuit which makes use of a transmission gate [Mohanty et al. 2007; Vadlamudi 2007]. The tristate buffer circuit acts as a high impedance circuit when it is in “not enabled” mode. The state of high impedance is defined as state of the output circuit which is not driven by the circuit. The function of passing circuit is to bypass the input signal as it is to the other side of the circuit. In other words it acts as a buffer between the input and output. The passing circuit is designed with the use of a transmission gate [Mohanty et al. 2007; Vadlamudi 2007].

Fig. 8 shows a transistor-level circuit design of the ULS. This is achieved by stitching the individual sub-circuits which perform step-up shifting, step-down shifting, and pass/blocking functionalities. To achieve programmability multiplexers are used wherever necessary. For circuit optimization, instead of using a 4:1 multiplexer or three 2:1 multiplexers, the functionalities are achieved by using two 2:1 multiplexers. They are controlled by the control signals S1 and S0. In the baseline circuit design transistor sizes, such as, $W = 320nm$, $L = 32nm$ for NMOS devices, and $W = 640nm$, $L = 32nm$ for the PMOS devices are chosen, respectively to achieve correct functionality of the ULS. By eliminating the redundant transistors a reduced transistor ULS circuit is constructed which is shown in Fig. 9. A further reduced transistor ULS circuit design is shown in Fig. 10. In this design, a switch constructed using transmission gates is attached in front of the level-up shifting circuit and level-down shifting circuit. The output of the ULS is controlled by the switches. The number of transistors was reduced to 24, eliminating 8 transistors from the baseline design. The 24-transistor ULS (Fig. 9) has two output nodes instead of one as in the case of 28-transistor design (Fig. 10). The choice of their use depends on the application. The single-output 28-transistor ULS has more flexible programmability, but has more area and power dissipation and is more suitable for FPGA environments. On the other hand, the two-output 24-transistor is less flexible programmability, but has lesser area and power dissipation, and is more suitable for application-specific integrated circuits (ASICs).

Each of the above sub-circuits of the ULS as well as the three variants of the ULS presented above are thoroughly tested and characterized through parametric, load, and power analysis. For power-delay optimization point-view, each of the above variants of ULS circuit (i.e. Fig. 8, Fig. 9, and Fig. 10) can be subjected to optimization using the algorithm presented in the following Section.

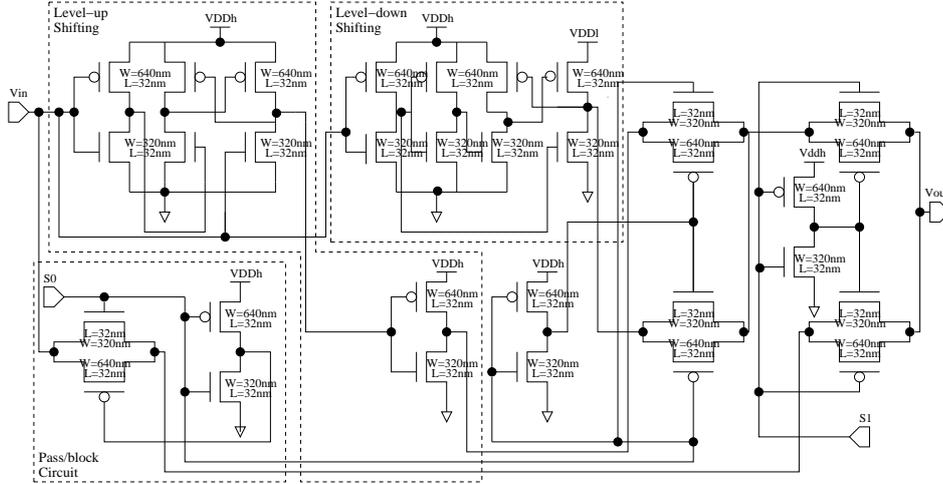


Fig. 8. Transistor level circuit of the baseline ULS with 32 transistors.

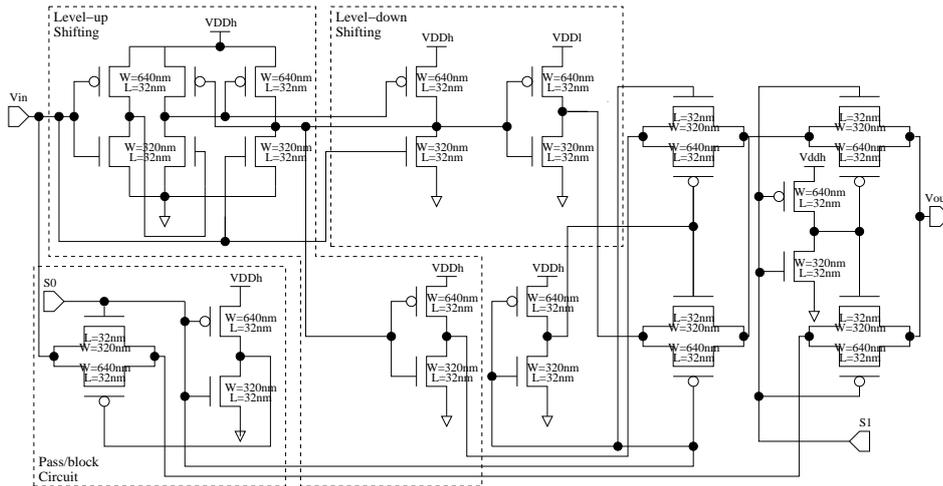


Fig. 9. Transistor level circuit of the ULS with 28 transistors.

4. DTCMOS BASED OPTIMIZATION IN HIGH- κ NANO-CMOS ULS

The dual V_{th} technique [Mohanty and Kougiianos 2007; Wei and et. al. 1999] is used along with transistor sizing to achieve a power-delay optimized ULS. In the optimization algorithm, power consumption dissipation of ULS is the target objective function and a propagation delay of ULS is the constraint. Any one of the three variants of ULS circuit can be subjected to optimization, however for brevity the rest of the discussions in this paper is for the 3rd circuit alternative with 24 transistors in Fig. 10.

First, the power-hungry transistors of the ULS circuit are identified and are assigned

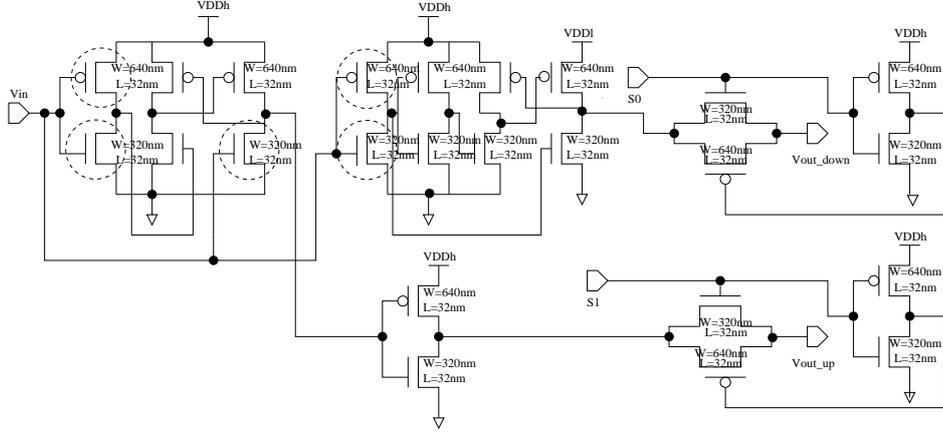


Fig. 10. Transistor level circuit of the optimal design of the ULS with 24 transistors. The circled transistors are identified as power-hungry and subjected to dual- V_{th} technique.

higher V_{th} values. Power-hungry NMOS are assigned 20% higher V_{th} and power hungry PMOS are assigned 50% higher V_{th} as compared to the nominal values specified for the technology node [Mohanty et al. 2010]. Those transistors are marked as dashed-circles in Fig. 10. This reduces the power consumption considerably, but increases the delay (Eqn. 3). Hence the transistor geometry is also explored, where the widths of all the transistors in the level-up and level-down shifting sub-circuits were considered. In general, sizing of parameters, such as, L , W , and finding appropriate value of V_{th} can be considered during optimization [Ghai et al. 2008; 2009]. However, for simplicity, sizing on W will be presented in this paper keeping other parameters at a technology defined nominal value for L and experimentally selected value of V_{th} .

Algorithm 2 is used for the power dissipation (accounting leakage) and delay optimization of the ULS circuit. The algorithm is based on conjugate-gradient method [Hager and Zhang 2006; Ghai et al. 2009]. The conjugate-gradient method is an algorithm for the numerical solution of systems of linear equations whose matrix is symmetric and positive-definite. The main advantages of the conjugate gradient method are its low memory requirements, and its convergence speed. This is based upon the Feasible Sequential Quadratic Programming. This is advantageous for analog circuits like ULS with complex netlist to be optimized.

The inputs to the proposed algorithm comprise of the circuit netlist, the objective set \hat{F} (P_{ULS} , D_{ULS}) with its stopping criteria S (e. g., 1 – 5%), and the design variable set \hat{D} with its lower constraint C_{lower} and upper design constraint C_{upper} . The lower design constraint C_{lower} is $(\hat{D} - \Delta\hat{D})$ i.e. $(W - \Delta W)$. The upper design constraint C_{upper} is $(\hat{D} + \Delta\hat{D})$ i.e. $(W + \Delta W)$.

The design variable set \hat{D} in this paper comprises of the followings: (1) W_{PMOSup} : width of PMOS transistors in level-up shifting sub-circuit, (2) W_{NMOSup} : width of NMOS transistors in level-up shifting sub-circuit, (3) $W_{PMOSdown}$: width of PMOS transistors in level-down shifting sub-circuit, and (4) $W_{NMOSdown}$: width of NMOS transistors in level-down shifting sub-circuit. The outputs of the algorithm are the optimized objective

Algorithm 2 The power-delay optimization algorithm for ULS circuit.

- 1: **Input:** Circuit netlist; Objective set $\hat{F} = [f_1, f_2 \dots f_n]$, i.e. $[P_{ULS}, D_{ULS}]$; Stopping criteria S , design variable set $\hat{D} = [d_1, d_2 \dots d_n]$, i.e. $[W_{PMOSup}, W_{NMOSup}, W_{PMOSdown}, W_{NMOSdown}]$; Lower design constraints on \hat{D} C_{lower} and Upper design constraints on \hat{D} C_{upper} .
 - 2: **Output:** $\hat{F}_{optimal}, \hat{D}_{optimal}$ for $S = \pm\sigma$, and optimal ULS circuit. {Where $1\% \leq \sigma \leq 5\%$ is designer defined error margin.}
 - 3: Perform the initial simulation in order to obtain feasible values of design variables for the given objective set.
 - 4: **while** ($C_{lower} < \hat{D} < C_{upper}$) **do**
 - 5: Use finite difference perturbation to generate new set of design variables $\hat{D}' = \hat{D} + \delta\hat{D}$ for design space exploration.
 - 6: Compute the new objective set $\hat{F}(\hat{D}') = [P_{ULS}, D_{ULS}]$.
 - 7: **if** ($S == \pm\sigma$) **then**
 - 8: i.e. Stopping criteria is in the error margin.
 - 9: **return** $\hat{D}_{optimal} = \hat{D}'$, where $\hat{D}' = [W_{PMOSdown}, W_{PMOSup}, W_{NMOSdown}, W_{NMOSup}]$.
 - 10: **end if**
 - 11: **end while**
 - 12: Obtain optimal values for design variable set $\hat{D}_{optimal}$.
 - 13: Redesign the ULS circuit with new variables.
 - 14: Compute optimized Objective set $\hat{F}_{optimal}$ for the ULS.
-

set $\hat{F}_{optimal}$ satisfying the stopping criteria S and the optimal values of the design variable set $\hat{D}_{optimal}$ within C_{lower} and C_{upper} .

During optimization, a simulation is performed using the initial values of \hat{D} and the value of \hat{F} are calculated, to determine whether the initial values are feasible for the given $\hat{F}_{optimal}$. In the next iteration, the design variable set (\hat{D}) values are changed accordingly to traverse towards the required $\hat{F}_{optimal}$. This is called finite difference perturbation. The ULS circuit is simulated again using this new design variable set. This process continues till $\hat{F}_{optimal}$ meets with stopping criteria S . The optimized objective set $\hat{F}_{optimal}$ is presented in Table II, and the $\hat{D}_{optimal}$ values are presented in Table III.

Table II. Optimized values of objective set $\hat{F}_{optimal}$.

Objective	Value
P_{ULS}	$5\mu W$
D_{ULS}	$1.6ns$

5. CHARACTERIZATION OF THE ULS CIRCUIT

This section discusses the functional simulation and characterization of ULS circuit. The ULS circuit is characterized using three types of analysis: parametric, load, and power analysis to check the robustness of the design. The functional simulation is same for all

Table III. Design variable values \hat{D} for optimal power and delay.

\hat{D}	C_{lower}	C_{upper}	$\hat{D}_{optimal}$
W_{PMOSup}	64nm	640nm	64nm
W_{NMOSup}	64nm	640nm	640nm
$W_{PMOSdown}$	64nm	640nm	64nm
$W_{NMOSdown}$	64nm	640nm	640nm

three alternative ULS circuits, whereas characterization results are different. For brevity, the characterization of 24-transistor ULS of Fig. 10 is discussed in this Section.

5.1 ULS Functional Simulation

Before constructing the overall ULS circuits the functional simulations of each sub-circuits responsible for level-up shifting, level-down shifting, and pass/block were performed [Mohanty et al. 2007; Vadlamudi 2007; Mohanty et al. 2009]. The functional simulation of the ULS is shown in Fig. 11. When the control signals S1 and S0 are “00”, the input signal V_{in} is blocked. When the control signals S1 and S0 are in the “01” state, V_{in} is $0.7V (V_{dd})$, and V_{out} is $0.595V (V_{ddl})$, i.e., level-down shifting of the input voltage signal is performed. When the control signals S1 and S0 are in the “10” state, V_{in} is $0.595V (V_{ddl} = 85\% \text{ of } V_{dd})$, and V_{out} is $0.7V (V_{dd})$, i.e., level-up shifting is performed. It is observed that the three functions, level-up shifting, level-down shifting, and blocking are performed depending on values of S1 and S0. This is verified from Table I. Thus, the ULS can be programmed, for example, by external stimuli through the radio-frequency (RF) interface of DDNEMS.

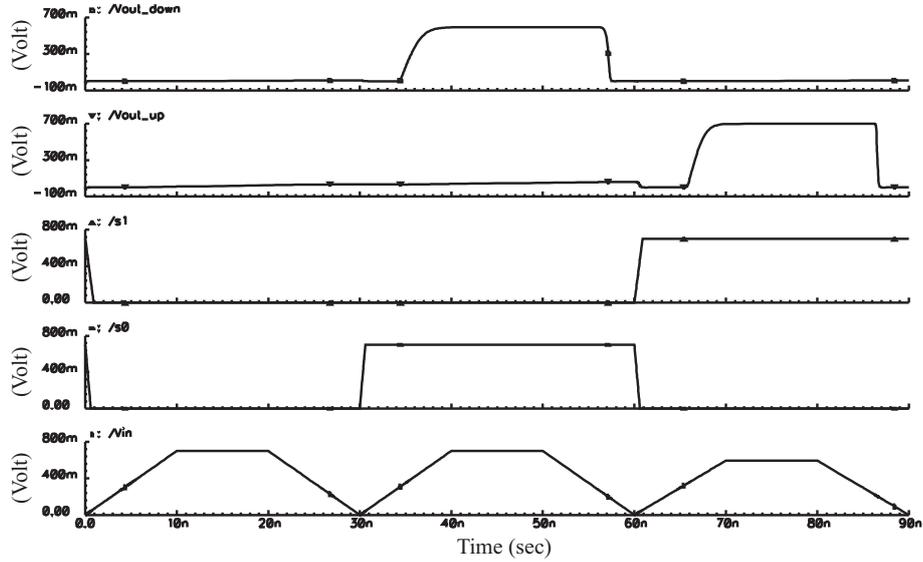


Fig. 11. Functional simulation of the ULS circuit. It verifies the truth table given in Table I, demonstrating its programmability capability of the ULS. The bottom-most curve is the input, the 2 top-most curves are the outputs, and the middle 2 signals are control signals. The sequence of operations is block, step-down, and step-up.

5.2 ULS Characterization

The ULS characterization for three types of analysis, such as, parametric analysis, load analysis and power analysis is now presented. It is observed that the ULS circuit is stable under varying operating conditions and hence the design is robust.

5.2.1 Parametric Analysis. The parametric analysis involves testing of the level-up shifting and level-down shifting of the ULS circuit. For the level-up shifting, V_{in} is varied from $0.1V$ to $0.595V$ in steps of $0.05V$ and the output of ULS is observed. As shown in Fig. 12(a), a stable level-up shifting is performed for voltages as low as $0.35V$ (50% of V_{DD}). For the level-down shifting, V_{in} is varied from $0.1V$ to $0.7V$ in steps of $0.05V$. The output in Fig. 12(b) shows that stable level-down shifting is performed for voltages greater than $0.35V$.

5.2.2 Load Analysis. Load analysis is used to determine the excess load the ULS can drive. The ULS can be placed in any portion of a target circuit; thus is it important that ULS operates under varying loading conditions. The value of nominal load capacitance (C_L) is taken as 10 times the gate capacitance of the PMOS transistors (C_{gg}) in the ULC [Mukherjee et al. 2005]. Thus the following expression is used for calculation of load capacitance for high- κ nano-CMOS technology:

$$C_L = 10 \times \left(\frac{\epsilon_{gate} \times W_{pmos} \times L_{pmos}}{T_{gate}} \right). \quad (6)$$

The nominal value of C_L is calculated as $82fF$. For the load analysis, the load capacitance is varied from $50fF$ to $120fF$ in steps of $10fF$. These values of load capacitance represent realistic loads [Yu et al. 2001]. The experimental results as shown in Fig. 13(a) and Fig. 13(b) demonstrates that the ULS circuit produces a stable and expected output voltage under varying load conditions.

5.2.3 Power Analysis. The power analysis of the ULS circuit is performed for three different capacitive loading conditions, such as $50fF$, $82fF$, and $120fF$. Table IV shows the values obtained from analog simulations. The input rise or fall times and switching frequency are also recorded. It is evident that there is not much difference in the power consumption with varying loads. The power measurement includes the dynamic power and subthreshold leakage in the ULS circuit. The gate leakage is measured to be negligible as expected due to the use of high- κ nano-CMOS.

Table IV. Power consumption of the 24-transistor ULS

Rise or Fall Time (ns)	Switching Frequency (MHz)	Capacitive Load (fF)	Power Dissipation (μW)
10	33.33	50	4.988
10	33.33	82	5
10	33.33	120	5.8

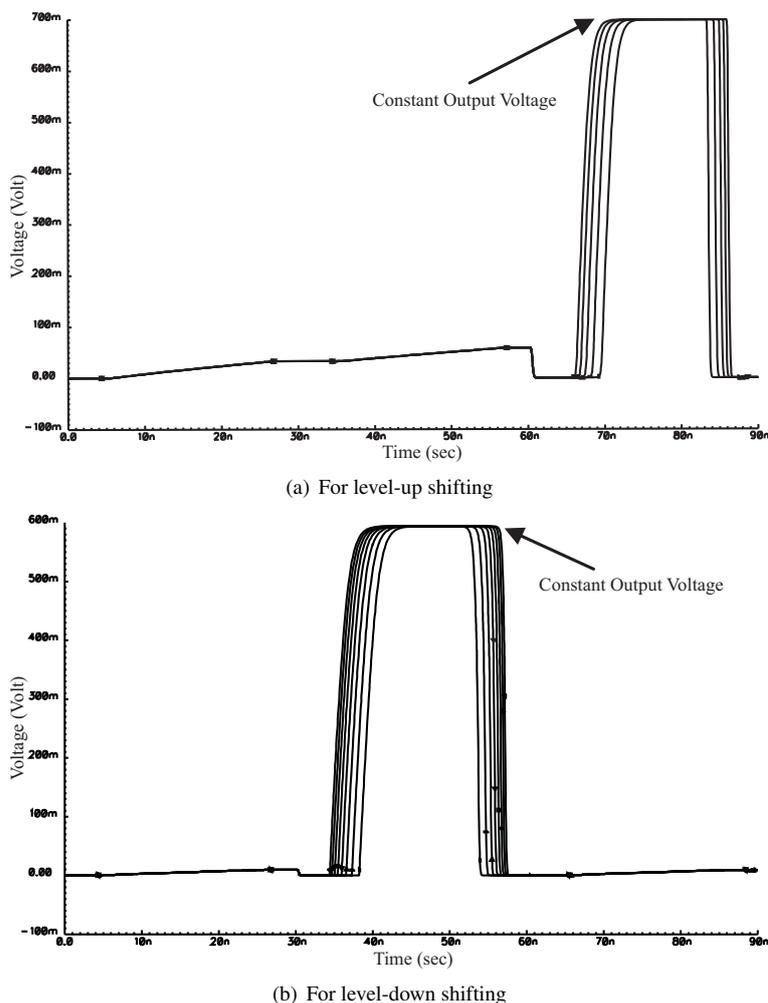
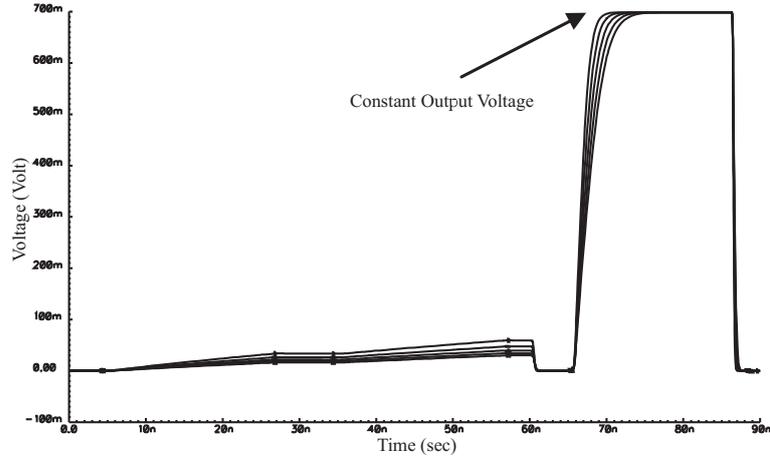


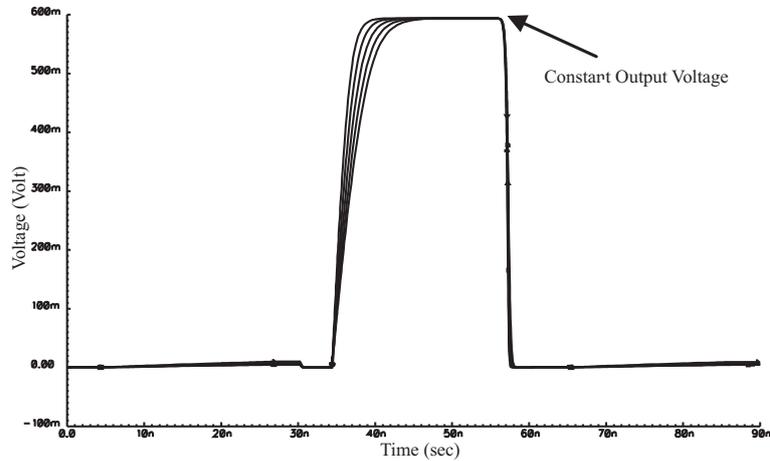
Fig. 12. Parametric analysis of the ULS showing the output (V_{out}) waveforms. It is evident that the ULS could produce constant output voltage even for varying input voltages.

6. RELATED PRIOR RESEARCH ON LEVEL SHIFTER CIRCUIT DESIGN

A comparative perspective of selected related prior research on DC to DC voltage-level shifters is presented in Table V. These existing research are diverse in terms of functionality, CMOS technology node, and circuit features. Thus, these existing research are discussed with a broad perspective without direct comparison. A level-down shifter with differential input pair operation is presented in [Kanno et al. 2000]. In [Yu et al. 2001], a symmetrical dual cascode voltage switch (SDCVS) is proposed which achieves 50% reduction in short-circuit power and 60% speed increase. In [Kulkarni and Sylvester 2003], new level converting circuits that consume 8 – 50% less energy compared to traditional techniques are proposed. In [Ishihara and Sheikh 2004], up-shifters and down-shifters have been used to minimize energy and delay. A level-up shifter using Dual Cascode Voltage



(a) For level-up shifting



(b) For level-down shifting

Fig. 13. Output under varying load conditions ($C_L = 50fF$ to $120fF$). ULS provides stable output voltage even though the loading condition changes.

Switch (DCVS) is presented in [Yuan and Chen 2005]. In [Sadeghi et al. 2006], only the issue of short-circuit power dissipation is handled. In [Ghai et al. 2008], a universal level converter performing the functionalities of the ULS presented in this paper is proposed for $90nm$ dual-oxide thickness technology.

The average power consumption of the ULS is $5\mu W$ making it the lowest power design reported. It is evident that this is the first ever reported level converter implemented using $32nm$ high- κ /metal-gate nano-CMOS technology. The proposed ULS consumes the least power compared to other level shifters presented. It can also be observed from the table that existing circuits perform a specific task, either up or down shifting, and are not programmable, unlike the ULS which can perform multiple tasks and programmable.

This archival journal paper is based on preliminary idea presented in [Mohanty et al.

Table V. Research on DC to DC Voltage-Level Shifters.

Research	Tech.	Power	Delay	Shifting Type
[Kanno et al. 2000]	140nm	–	5ns	Down
[Yu et al. 2001]	350nm	220.57 μ W	–	Up
[Kulkarni and Sylvester 2003]	130nm	–	–	Up
[Ishihara and Sheikh 2004]	130nm	–	127ps	Up/Down
[Yuan and Chen 2005]	180nm	–	–	Up
[Sadeghi et al. 2006]	100nm	10 μ W	1ns	Up
[Mohanty et al. 2007]	90nm	27.1 μ W	–	Up/Down/Block
[Ghai et al. 2008]	90nm	12.26 μ W	111.3ps	Up/Down/Block
This Paper	32nm	5 μ W	1.6ns	Up/Down/Block

2009]. In the current paper, system-level energy management aspects as well as energy-efficient design of the ULS are presented. Three representative systems, such as DDNEMS, SDC, NMP are discussed, which are needed in critical applications like health care, DRM, and video broadcasting over IP. Formal representation of the design flow of the ULS is presented for high- κ /metal-gate nano-CMOS technology. The optimization algorithm for energy-efficient design of ULS using dual- V_{th} technology is thoroughly discussed. In the previous publication [Mohanty et al. 2007], the general idea of universal level shifter was introduced whereas, in [Ghai et al. 2008] dual- T_{ox} technology is used for energy-efficient design of the ULS.

7. SUMMARY, CONCLUSIONS, AND FUTURE RESEARCH

In this paper, a new circuit called ULS is presented for the static as well as dynamic power management in multiple-supply voltage (V_{DD}) based AMS-SoC architecture. The ULS is applicable for scenarios where different supply voltage are needed from a single power supply. The ULS is capable of performing three types of distinct level converting operations on the input signal: up-shifting, down-shifting, and blocking. This makes the proposed ULS highly suitable for use in the context of dynamic power management in a multi- V_{dd} AMS-SoC. The ULS can be used for static power management (i.e. low-power design) in multi- V_{dd} based circuits to connect islands operated at different voltage levels. ULS can also be used to disconnect power supply when a portion of the circuit is not used.

As a specific realization, an 32nm high- κ /metal-gate based design of the ULS is presented. The ULS circuit is subjected to further power minimization by applying a dual- V_{th} technique. Finally, an algorithm is introduced and applied for the power and delay optimization of the entire ULS circuit. The robustness of the ULS circuit is tested using parametric, load and power analysis. It is observed that a stable output is obtained for voltages as low as 0.35V and capacitive loads varying from 50fF to 120fF.

A complementary of this research is an array of batteries (called IntellBatt) which are scheduled using novel switching mechanism to provide voltage levels needed [Mandal et al. 2008]. Such battery scheduling also attractive for system-level power management which extends the battery life by 22%. Thus, a combined ULS and IntellBatt can be immensely useful for system-level power management particularly in portable applications.

Based on the ULS idea, future research will include considering gate-induced junction leakage (GIDL) in the optimization process. Physical design for 32nm high- κ technol-

ogy will be performed. As part of future research, it is planned to design the ULS using other nanoscale technologies, such as double gate FET (DGFET), Carbon Nano-Tube FET (CNTFET), etc., and analyze the effects on the performance metrics.

8. ACKNOWLEDGMENT

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