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Special Issue on Nanoelectronic Circuit and System Design Methods for the Mobile Computing Era

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Guest Editorial

Special Issue on Nanoelectronic Circuit and System Design Methods for Mobile Computing Era

This special issue on nanoelectronic circuit and system design method for mobile computing era covers a wide range of design challenges and solutions facing current designers for fast performing and energy efficient computing platforms. The papers presented in this issue span through various design challenges from devices, circuits and architecture to address some of the most imminent issues for low power computing. It is well known that the use of smart mobile phones, tablets, and notebooks, which are different forms of mobile computing platform, defines the present age social life style. Such heavy demand for ever smaller, portable, low-energy, high-performance, and secure electronic systems has been the primary driver for recent VLSI technology scaling. To continue coping with this trend, and to address new massive markets of the Internet of Things (IoT), high performance with energy constraints, low leakage dissipation, fast sleep and wake-up transitions, as well as reliability and security still remain significant challenges to address in future integrated circuits. In recent years, as the device sizes have reduced below 10nm, the challenges of design and manufacturing engineers have increased multifold. One example is leakage current, which because transistors are so small, now represents a significant proportion of the power consumption. Imagine, battery life of a smartwatch is matter of 24 hours only! Thus, at device level alternate device architecture, e.g. thin film devices like FinFET or FDSOI, nanowires or 3-D transistor are introduced and proposed for the next nodes. Simultaneously alternative to Flash memory are explored. Most of the proposals are based on resistive devices, e.g. MRAM, PCRAM, ReRAM. Designers have to assess the benefits of these new devices as well as to innovate by exploiting their unique capabilities. Better system level architectures are also required for high-performance at minimum energy, and reliability. Finally, circuit- and system-level solutions are needed to improve security of the information being processed by the hardware. This special issue describes six articles covering topics from emerging technologies for devices and memories, architecture to processor design for energy efficiency and high performance. We briefly introduce them in the rest of the guest editorial.

Sartor et al., present several design techniques for very long instruction word (VLIW) processors to mitigate soft errors introduced due to technology scaling. The proposed fault tolerance techniques based on 1) phase-configurable duplication, 2) adaptive duplication and 3) adaptive with ILP reduction provide fault tolerance at a minimum cost, by using idle resources of the VLIW processor with low area and power overhead. For the first two methods, the area overhead is less than 4% with no performance degradation. The third method based on ILP reduction has shown effective to improve fault tolerance with the cost of 14% area overhead and up to 27% of performance degradation. This is seminal work on exploiting the idle cycles of processor for improving its reliability and fault tolerance.

Fault tolerance is further investigated by *Mohammadi et al.* on arithmetic logic build based on controllable-polarity transistors. Such devices are very promising for implementing compact logic elements due to their enhanced functionalities such as they can be electrostatically configured to be either n- or p-type device. Authors present fault models and analysis unique for controllable polarity transistors in order to forecast the behavior of more complex circuits composed of such devices. Experimental results on a adder architecture indicate that the proposed fault tolerant design is able to tolerate all possible single faults and up to 99.5% of double faults with minimal impact on area, performance and leakage power. Such large fault tolerance further motivates design of complex arithmetic logic at reduced implementation cost.

Fang et al., present a paper on exploring oscillator based computing systems with emerging nano-devices that can be exploitable for computer vision and pattern recognition applications. Inspired by

the interactions between neural oscillations that occur on biological systems, recent advancements on spin torque oscillators, resonate body transistor oscillators and vanadium oxide oscillators have enabled building complex systems that can become the next generation computing structures used for intelligent information processing. Authors present an in-depth look into the challenges on building complex, energy efficient and fast-performing systems based on oscillator devices. They provide models and analysis to understand how to build complex oscillator systems and address some of their fundamental issues such as synchronization/de-synchronization, prediction of oscillator frequencies and their relation to the degree of match function for pattern matching.

In *Moreira et al.*, a new computing system based on digitally controlled delay elements is explored that yields low power and moderate delay quantization error under process, voltage and temperature variations. They proposed a novel generic delay shift block using the 28nm FD-SOI technology. Authors show from the obtained results that process variations impact on performance can be alleviated and fine-tuned by using the proposed digitally controlled elements indicating the promise of building larger and more complex system based on such elements.

Exploring non-volatile memory for novel computing paradigms such as normally-off computing is the scope of the paper from *Senni et al.*. The paper explores the opportunity of having a non-volatile memory as reconfigurable logic devices, processor and data storage by the integration of MRAM as register and main memory levels. Investigation on use of MRAM to design non-volatile processor is studied and analyzed the backup/restore performance and power consumption.

In *Rakshit et al.*, monolayer heterojunction FETs based on vertical transition metal dichalcogenides (TMDCFETs) and planar black phosphorus FETs (BPFETs) have been explored to design energy-efficient and denser SRAM. The approach relies on an atomistic self-consistent device modeling with SRAM circuit design and simulation. The SRAM has lower static power, smaller read/write delay and high dynamic read/write noise margin at the low operating voltages.

In *Kim et al.* layouts and parasitic capacitances and resistances have been analyzed for the asymmetric heterojunction vertical tunnel FET (HVTFETs). It is found out that the HVTFETs have smaller foot prints as compared to FinFET due to their vertical structure for small fan-in cells. However, for high fan-in cells, this paper demonstrated that HVTFETs exhibit larger area-overheads.

Finally, the guest-editors sincerely hope that this special issue will be a great read for contemporary researchers worldwide. The guest editors would like to sincerely acknowledge the Editor-in-Chief of ACM Journal on Emerging Technologies in Computing Systems (JETC) Dr. Krishendu Chakrabarty and Dr. Yuan Xie. The guest editors are extremely thankful to the reviewers for their timely reviews. A majority of the reviewers represent experts in their fields who provided high quality reviews for the papers. We thank the authors for their patience and dedication at all stages of the review process. Each manuscript was assigned at least to three reviewers and has undergone multiple rounds of peer-review process.

- Guest Editors
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Dr. Aida Todri-Sanial (<http://www.lirmm.fr/~todri>) received the B.S. degree in electrical engineering from Bradley University, IL in 2001, M.S. degree in electrical engineering from Long Beach State University, CA, in 2003 and Ph.D. degree in electrical and computer engineering from the University of California, Santa Barbara, in 2009. She is currently a Research Scientist for French National Council of Scientific Research (CNRS) attached to Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier (LIRMM). Previously, she was an R&D Engineer for Fermi National Accelerator Laboratory, IL. She has also

held summer and visiting research positions at Mentor Graphics, Cadence Design Systems, STMicroelectronics and IBM TJ Watson Research Center. Her present research interests focus on nanometer-scale issues in high performance VLSI design with emphasis on power, thermal, signal integrity and reliability issues as well as on circuits and systems for emerging technologies. Dr. Todri-Sanial was a recipient of CNRS Medaille de Bronze 2016, John Bardeen Fellow in Engineering in 2009 and CNRS Prime d'Excellence Scientifique in 2012. She serves as Technical Program Committee member for ISVLSI, NEWCAS, GLSVLSI, ISQED, EDSSC and DATE.



Saraju P. Mohanty is a Professor at the Department of Computer Science and Engineering (CSE), University of North Texas (UNT), where he directs the NanoSystem Design Laboratory (NSDL). He obtained a Ph.D. in Computer Engineering from the University of South Florida (USF) in 2003, a Master's degree in Systems Science and Automation (SSA) from the Indian Institute of Science (IISc), Bangalore, India in 1999, and a Bachelor's degree (Honors) in Electrical Engineering from Orissa University of Agriculture and Technology (OUAT), Bhubaneswar, India in 1995. Prof. Mohanty's research is in "Energy-Efficient High-Performance Secure Electronic Systems". Prof. Mohanty's research has been funded

by National Science Foundation (NSF), Semiconductor Research Corporation (SRC), and Air Force. Dr. Mohanty is an inventor of 4 US patents. Prof. Mohanty is an author of 220 peer-reviewed research articles, and 3 books. The publications are well-received by the world-wide peers with a total of 2900 citations leading to an h-index of 27 and i10-index of 76 (from Google Scholar). His latest book titled Nanoelectronic Mixed-Signal System Design is published by McGraw-Hill in 2015 is a best seller. This book received 2016 PROSE Award for best Textbook in Physical Sciences & Mathematics from the Association of American Publishers (AAP). Prof. Mohanty has been serving on the editorial board of several peer-reviewed international journals or transactions. He currently serves on the editorial board of 6 peer-reviewed international journals, including IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), ACM Journal on Emerging Technologies in Computing Systems (JETC), and IET Circuits, Devices & Systems Journal (CDS). He is the Editor-in-Chief of the IEEE Consumer Electronics Magazine. He serves as a founding Editor-in-Chief (EiC) of the VLSI Circuits and Systems Letter (VCAL). He has been serving as a guest editor for many prestigious journals including ACM Journal on Emerging Technologies in Computing Systems (JETC) and IEEE Transactions on Emerging Topics in Computing (TETC). Prof. Mohanty currently serves as the Chair of Technical Committee on Very Large Scale Integration (TCVLSI), IEEE Computer Society (IEEE-CS) to oversee a dozen of IEEE conferences. He serves on the steering, organizing, and program committees of several international conferences. He is the founding steering committee chair for the IEEE International Symposium on Nanoelectronic and Information Systems (iNIS) and steering committee vice-chair of the IEEE-CS Symposium on VLSI (ISVLSI). Prof. Mohanty is a senior member of IEEE and ACM. Prof. Mohanty has supervised 8 Ph.D. dissertations and 25 M.S. theses; seven of these advisees have received outstanding student awards at UNT. He has received Honors Day recognition as an inspirational faculty at the UNT for multiple years. He has also received UNT Provost's Thank a Teacher recognition for multiple years. More about his biography, research, education, and outreach activities can be obtained from his website: <http://www.smohanty.org>.



Mariane Comte received her Master of Engineering and Master of Sciences degrees in Microelectronics Engineering at the INPG, Grenoble, France in 2000. She carried out her Ph.D. studies at Laboratory of Computer Science, Robotics and Microelectronics of Montpellier (LIRMM), Montpellier, France working on Analog-to-Digital Converter testing. She received the Ph.D. degree in Microelectronics from the University of Montpellier in 2003. She is currently an Associate Professor in the Microelectronics department at LIRMM. Her main research interests concern fault modeling of CMOS, emerging technologies and devices, test of mixed-signal and RF integrated circuits and

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Marc Belleville received a Ph.D. degree from the Grenoble National Polytechnic Institute in 1980. Since then, he has been involved in circuit design spending the first 6 years in industrial companies. He joined CEA-LETI in 1985, and occupied several positions of team leader. He is now research director and chief scientist of the Architecture, IC Design and Embedded Software division in the Center for Innovation in micro & nanotechnology (MINATEC). Marc Belleville background is mostly focused on the interactions between design and advanced technologies (SOI, heterogeneous or 3D design for instance). He is author or co-author of 21 patents and 85 international communications or publications. He is IEEE Senior Member.