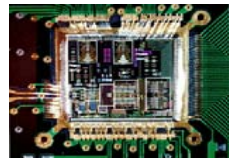
Lecture 1: Introduction

CSCE 5730
Digital CMOS VLSI Design

Instructor: Saraju P. Mohanty, Ph. D.

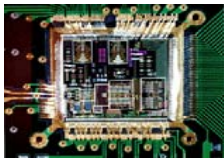
NOTE: The figures, text etc included in slides are borrowed from various books, websites, authors pages, and other sources for academic purpose only. The instructor does not claim any originality.



Lecture Outline

- First day administrative stuff:

  Instructor, student, class

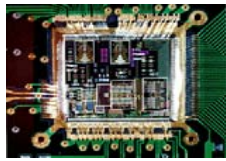


Class Time and Venue

- **Course Homepage:**
  http://www.cse.unt.edu/~smohanty/teaching/CMOSVLSIFall08

- **Class Timing and Venue:**
  MW -- 5:00PM-6:20PM, NTRP B192

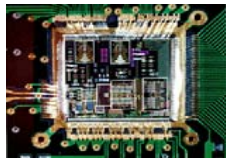
- **Instructor's Office:**
  Office Hours: MW -- 3:30-4:30PM (any other time possible by appointment through email)
  Room: NTRP F247
  Email: saraju.mohanty@unt.edu
  Homepage URL: http://www.cse.unt.edu/~smohanty/



Course Syllabus and Description

Course objectives:

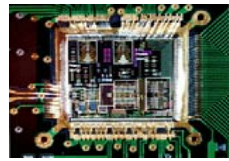
To understand theory and to learn design of digital systems at transistor level. The course will involve design, layout and simulation of digital VLSI circuits using various CAD tools.



Course Syllabus and Description ….

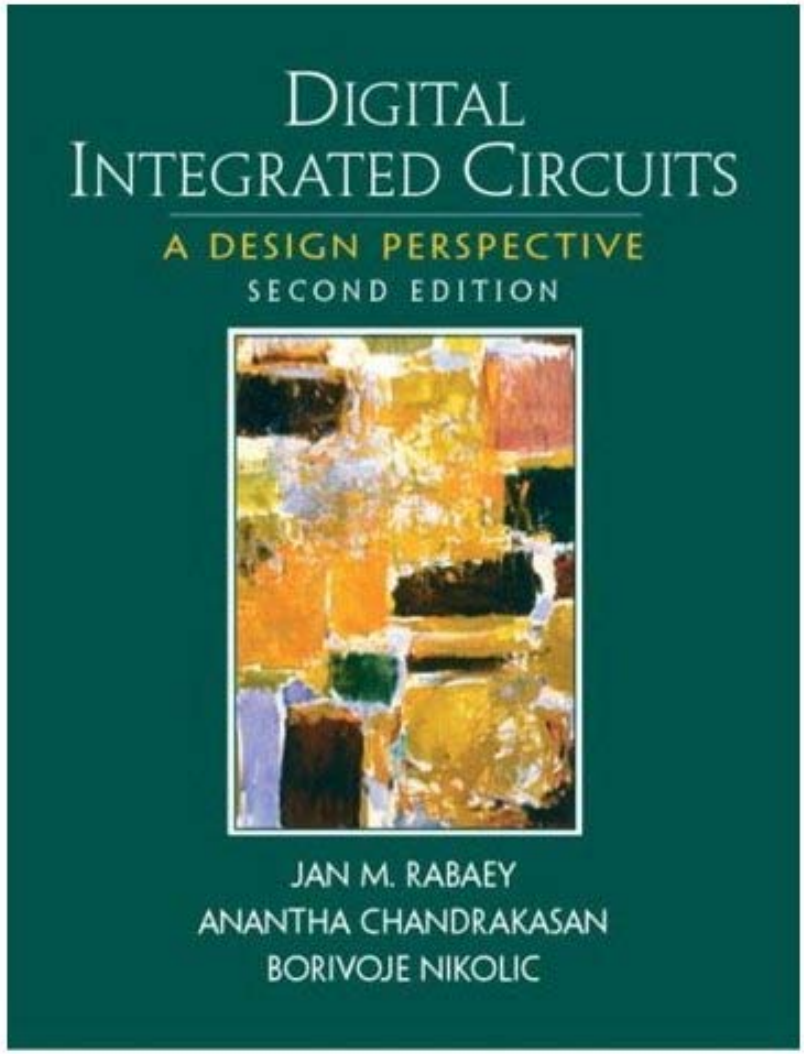
- **Prerequisites:** Minimal knowledge of computer logic design, semiconductor physics.

- **Level of the Course:** The course is designed for first year graduate students and advanced undergraduate students.



Course Syllabus and Description ….

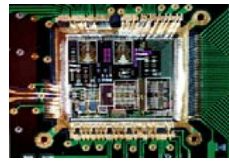
Digital Integrated Circuits (2nd Edition) by Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, Prentice Hall.



Course Syllabus and Description ….

Selected Topics (Tentative):

- MOS transistor theory
- CMOS processing technology
- Circuit Characterization
- Power Dissipation
- Clocking Strategies
- Design methods and tools
- CMOS testing
- System Design Examples



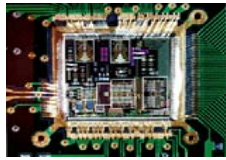
Course policy

- **Attendance for this course is mandatory** . In the case of absence due to unavoidable reasons, substantial documented evidence must be provided.

- Several **assignments** including exercise problems and design works will be given. The written or typed solutions for exercise problems and reports for design works must be submitted in the class **at the beginning of lecture** of the announced deadline, else **there will be late penalty of 20%** . Under no circumstances late assignment will be accepted two days after deadline and score for such assignment will be zero.

- Several surprise **quizzes** will be given in the class. There will be no make up quiz for any student under any circumstances.

- **There will be three tests of equal weightage.** There will be no final test. The tests will be approximately evenly spaced throughout the semester. The tests will be conducted in the same lecture room. The dates of the tests will be announced right on the 1st lecture, and the test dates will not be changed under any circumstances.



Course policy …..

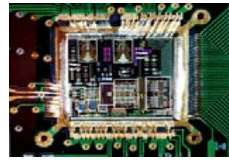
- Any makeup test will not be given unless substantial documented evidence is provided for a reasonable excuse of absence. In the absence of the documented evidence the score for the test will be zero.

- Any questions regarding the test grades should be clarified **a week of returning the test**. If no complaint is formulated within one week after the grades are posted on the course web page, **it will be considered that the student accepted the grade and the corresponding grades are considered definite** .

- No student shall be compelled to attend class or sit for a test on a day or time prohibited by his or her religious belief.

- Dishonesty in this class will be handled as per the University of North Texas policy (http://www.unt.edu/csrr).

- If a students needs any special accommodations according to the American Disability Act, he or she should let the instructor know.

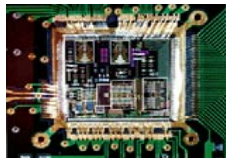


Tests Dates

Test No.	Date	% of Final Grade (for CSCE 5730)	% of Final Grade (for EENG 4710)
Test 1	29 Sep 08 (Mon)	20	25
Test 2	29 Oct 08 (Wed)	20	25
Test 3	24 Nov 08 (Mon)	20	25

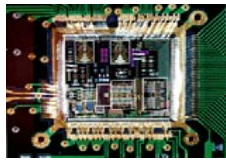
NOTE:

- Tests will be closed book and closed notes.
- Test dates will not be changes under any circumstances.



Grading Procedure

Items	% of Final Grade (CSCE 5730)	% of Final Grade (EENG 4710)
Tests	60	75
Assignments	10	10
Quizzes	10	10
Project/ Survey	15 (Abstract + Report + Presentation - 3+8+4) Deadlines: 1. Abstract: 6 Oct 08 (Mon) 2. Report: 26 Nov 08 (Wed) 3. Presentation: 26 Nov 08 (Wed), 01 Dec 08 (Mon), 03 Dec 08 (Wed)	NA
Discretion	5	5

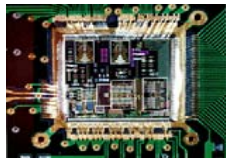


Grading Policy

A >= 90
90 > B >= 80
80 > C >= 70
70 > D >= 60
60 > F

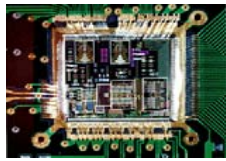
NOTE: (i) Grading policy may change if University or Dept. decide so.

(ii) There will be no border grade concessions.



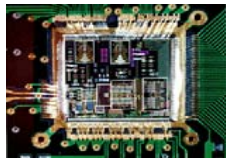
Course Software

- Students should have access to a computer to do the assignments and projects.
- The computer may be either one's own Workstation/PC/laptop or a Workstation/PC in general access laboratory.
- Students are free to choose anyone of them.
- Students can use various tools, such as microwind-DSCH/LT-SPICE/Cadence, etc.



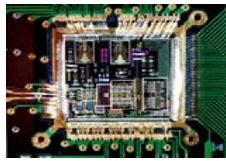
Assignments: Exercises

- Exercise problems from text book and other sources and Circuit Design/Simulation.



Projects

- All projects are individual projects.
- Any topic can be chosen by a student and can be assigned by instructor.
- Important: Start from the first day of class ☺



Survey

- Intended to make the student learn a particular area of current research.
- Needs to be done individually.
- Any topic can be chosen by a student and can be assigned by instructor.
- Important: Start from the first day of class ☺