Lecture 6: Energy Reduction

CSCE 6730
Advanced VLSI Systems

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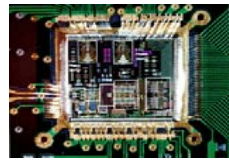
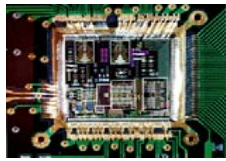
NOTE: The figures, text etc included in slides are borrowed from various books, websites, authors pages, and other sources for academic purpose only. The instructor does not claim any originality.



Outline of the Talk

- Why frequency variations ?
- What is dynamic frequency clocking (DFC) ?
- TC-DFC scheduling scheme
- RC-DFC scheduling scheme
- Experimental results
- Related Research
- Conclusions

Source: S. P. Mohanty and N. Ranganathan, "Energy Efficient Datapath Scheduling using Multiple Voltages and Dynamic Clocking", *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 10, No. 2, April 2005, pp. 330-353.



Why Frequency Variations?

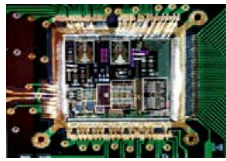
1. Energy dissipation per operation, $E = C_{eff} * V_{dd}^2$

2. Power dissipation per operation, $P = C_{eff} * V_{dd}^2 * f$

3. Delay that determines maximum frequency,

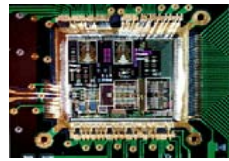
   $t_d = k * V_{dd} / (V_{dd} - V_T)^{\alpha}$

   where, α is a technology dependent factor, k is a constant and $1/ t_d = f_{max}$



What we deduce from the equations ?

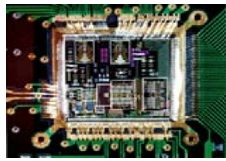
1. If we reduce supply voltage (V_{dd}), delay increases and performance degrades.
2. If we reduce clock frequency (f), we save only power, but do not save energy.
3. If we reduce switching activity, we reduce the effect of (C_{eff}) as well as correlations to an extent. – this needs to be done irrespective of 1 and 2 above.



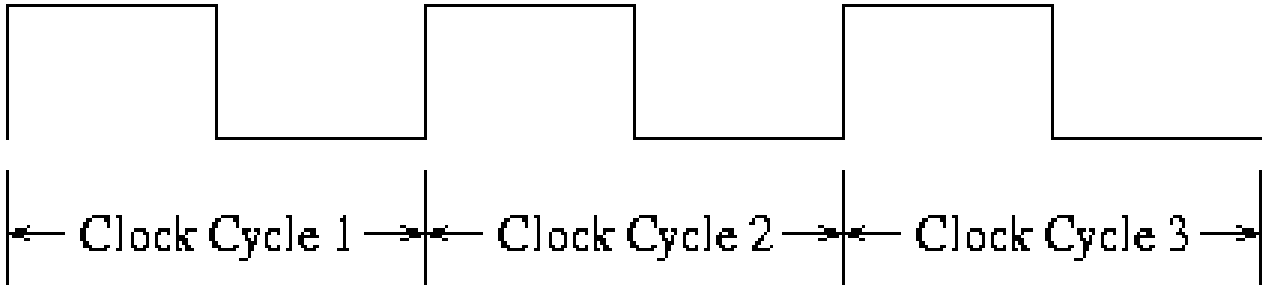
Our Approach

Adjust the processor's frequency and reduce the supply voltage together during scheduling

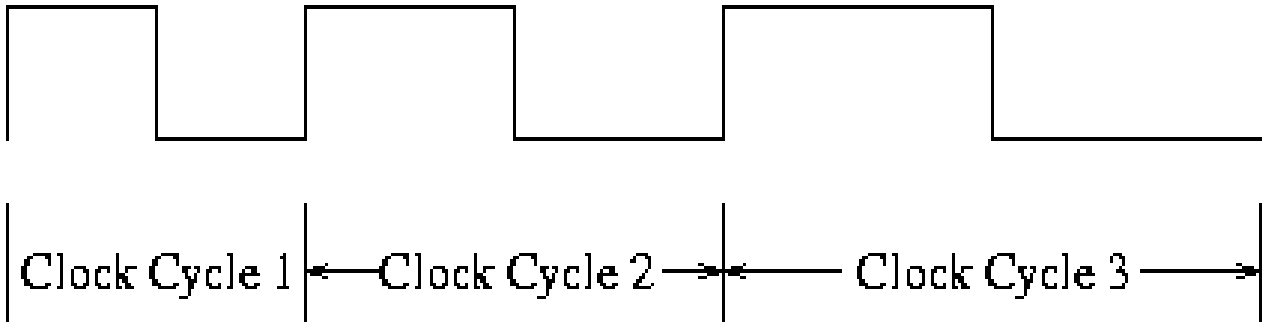
By doing that we reduce energy while maintaining performance or even improve performance if possible!



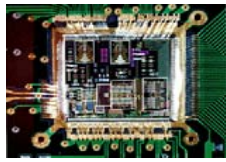
Dynamic Frequency Clocking (DFC)



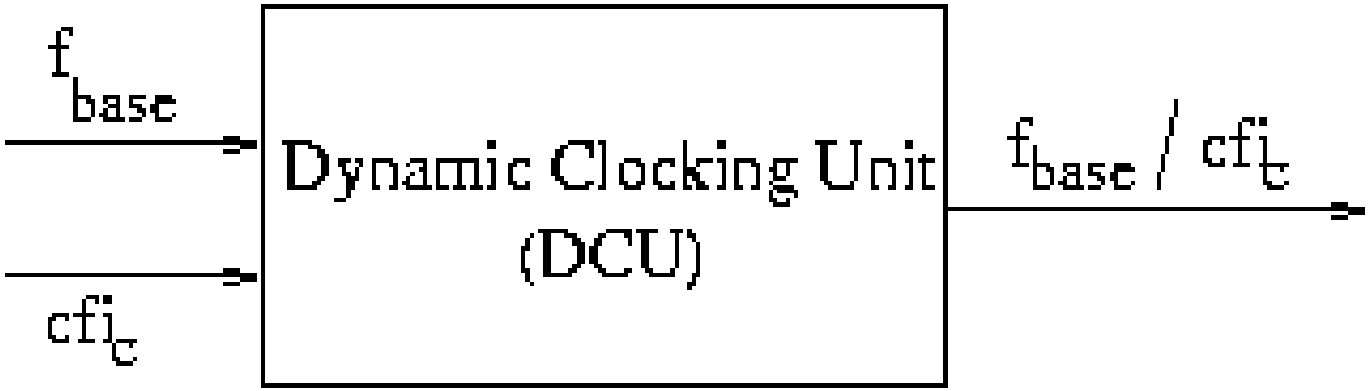
(a) Clock Cycle 1 = Clock Cycle 2 = Clock Cycle 3



(b) Clock Cycle 1 ≠ Clock Cycle 2 ≠ Clock Cycle 3



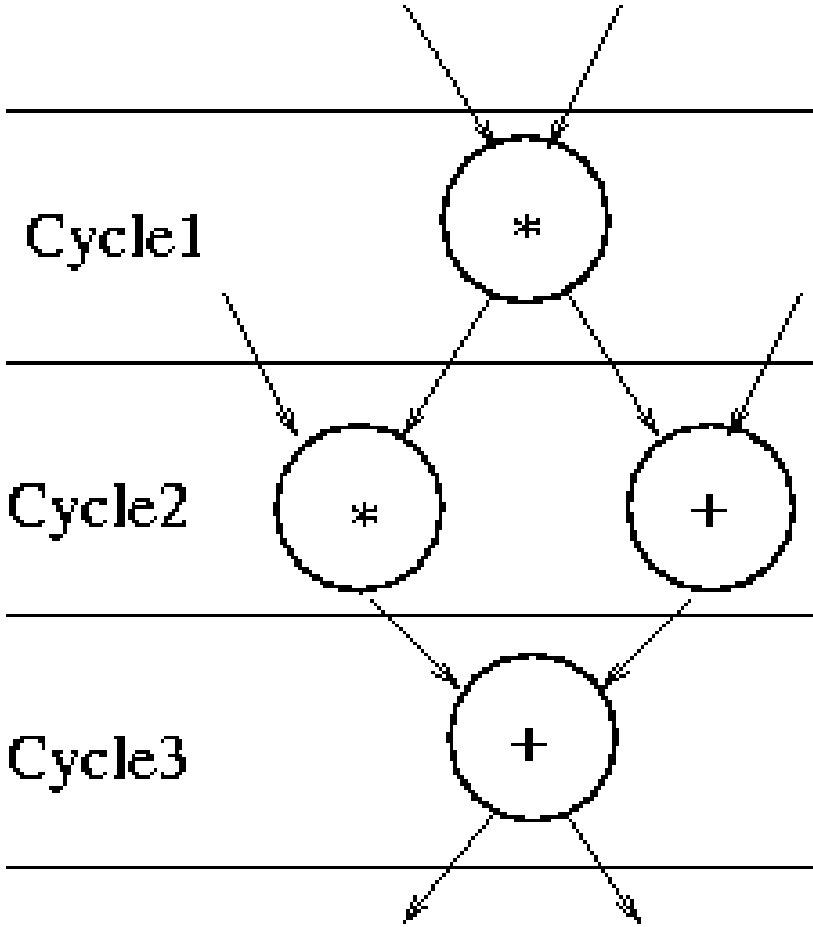
Dynamic Clocking Unit (DCU)



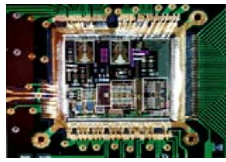
DCU uses clock divider strategy.

More details : Ranganathan [12]

DFC for energy savings and performance



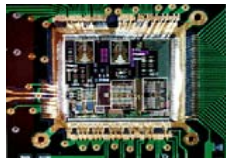
	Single Frequency				Dynamic Frequency			
Cycle1	t_m	V	E_m		t_m^+	V^-	E_m^-	
Cycle2	t_m	V V	E_m E_a		t_m	V V^-	E_m E_a^-	
Cycle3	t_m	V	E_a		t_a	V	E_a	
	(a)	(b)	(c)		(d)	(e)	(f)	



TC-DFC/RC-DFC Schedulers

What they do ?

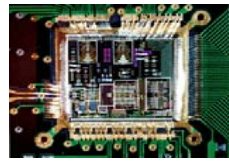
Attempts to operate high energy units (multipliers) at lower frequencies (voltages) and low energy units (ALUs) at higher frequencies (voltages) to save energy without loosing performance as much as possible



TC-DFC Algorithm

Input: Unscheduled DFG, time constraint (execution time for critical path), operating frequencies and voltages

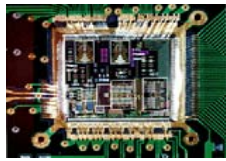
Output: Scheduled DFG with frequency assignment for each control step (cycle) and voltage assignment for each vertex (operation)



TC-DFC Algorithm

Vertex priority list: the vertices from source to sink in DFG are reordered such that the multipliers are grouped with higher priority than adders and among the multipliers (and adders) the precedence in DFG is maintained. (used to ensure precedence by time-stamping)

Cycle priority list: the control steps or the cycles are reordered in this list such that the cycles with more simultaneous operations (consuming more energy) get higher priority. (used for low frequency assignment in the algorithm)



TC-DFC: Scheduling Algorithm

Step 1: ASAP schedule of the sequencing UDFG

Step 2: create vertex priority list of vertices in DFG

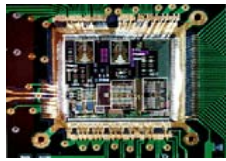
Step 3: assign control steps to the operators such that precedence is satisfied and that multiply and add operators are not scheduled in the same cycle - yields an intermediate schedule

Step 4: create a cycle priority list using the intermediate schedule

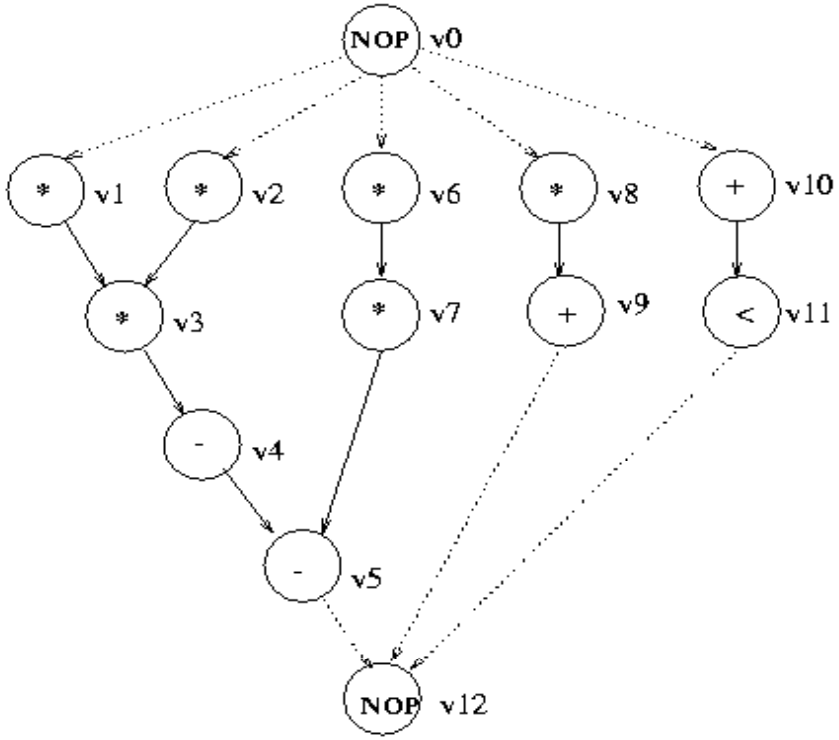
Step 5: assign frequency to each control step using cycle priority list – assign higher frequency to lower priority steps

Step 6: If execution time not close to time constraint, then eliminate the control step that has minimal number of ALU operations also adjusting all its predecessors to get a new intermediate schedule. Go to Step 3.

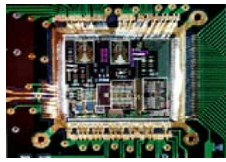
Step 7: To the schedule with frequency assignment for each control step, perform voltage assignment for each operation



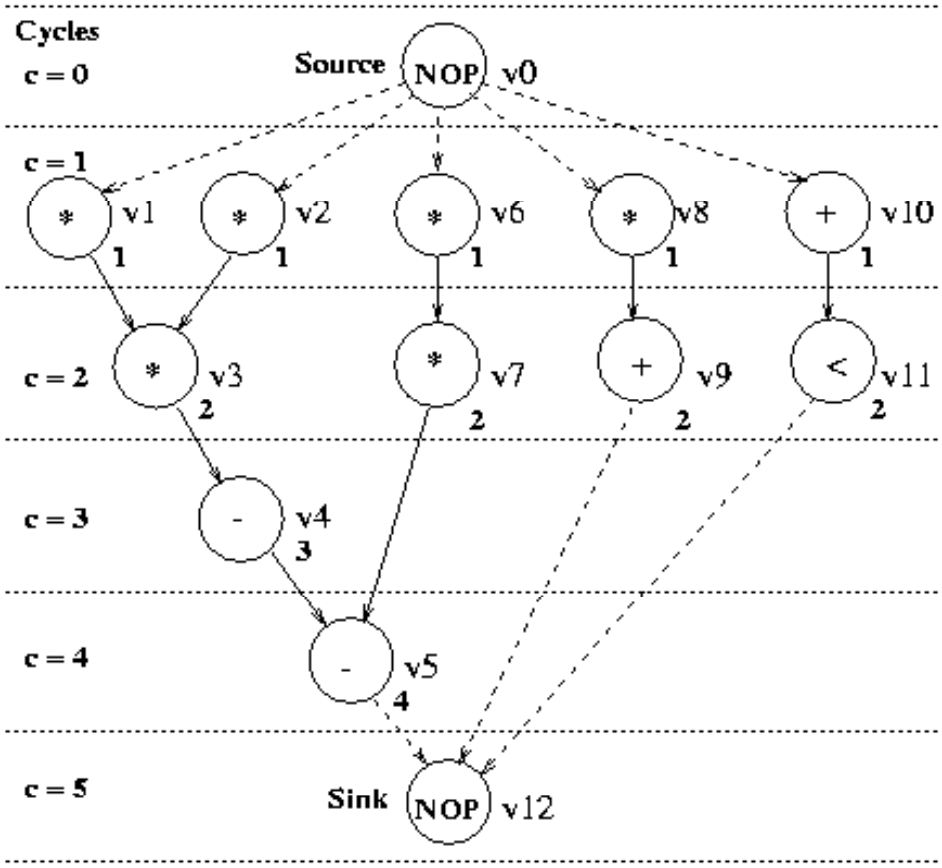
Example to illustrate TC-DFC

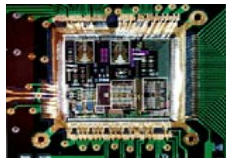


(HAL Differential Equation Solver)



Example TC-DFC : ASAP Time stamp





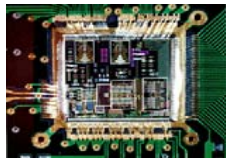
TC-DFC : Freq. Selection & Vertex Priority

	$MULT_{Low}$	$MULT_{Med}$	$MULT_{Med}$	ALU_{High}
Frequency	4.5 MHz	9 MHz	18 MHz	36 MHz
cfi_c	8	4	2	1

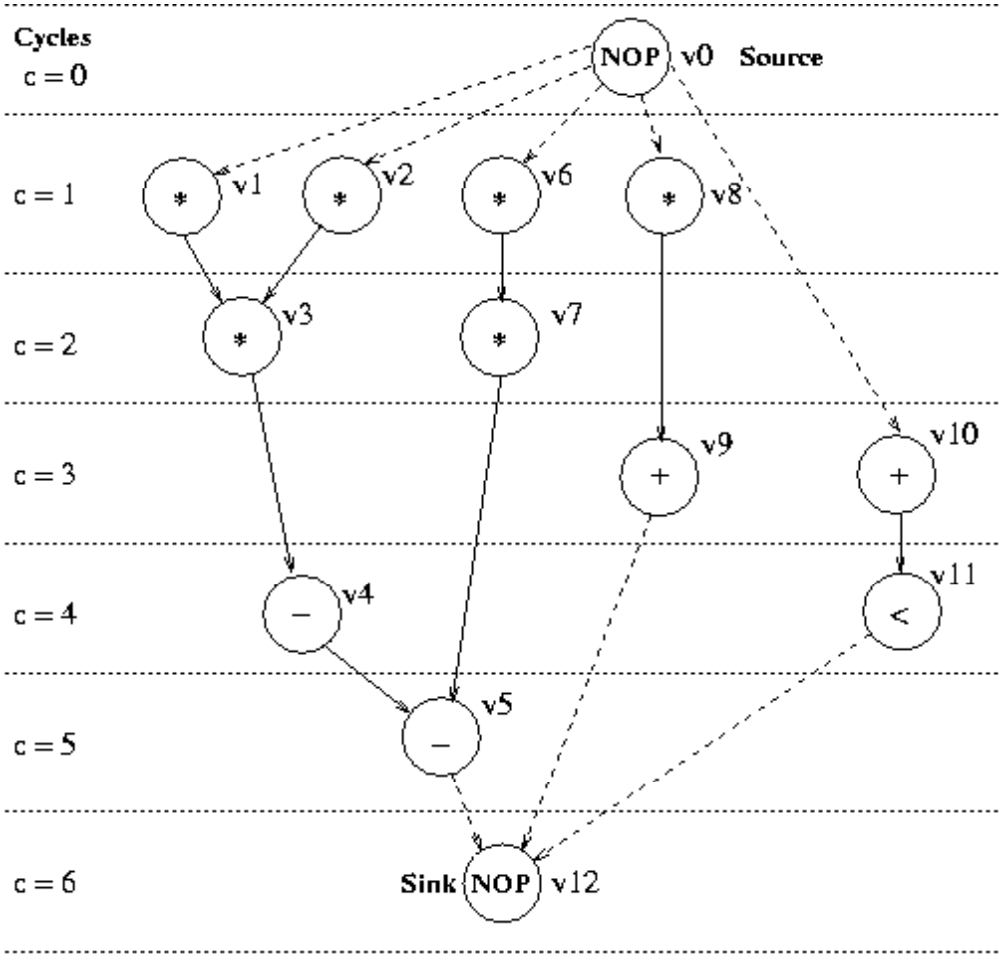
Table : Frequency selection : Left to right

v0	v1	v2	v6	v8	v3	v7	v10	v9	v11	v4	v5	v12
0	1	2	3	4	5	6	7	8	9	10	11	12

Table : Vertex Priority List

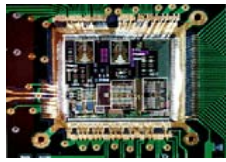


TC-DFC : Intermediate Schedule

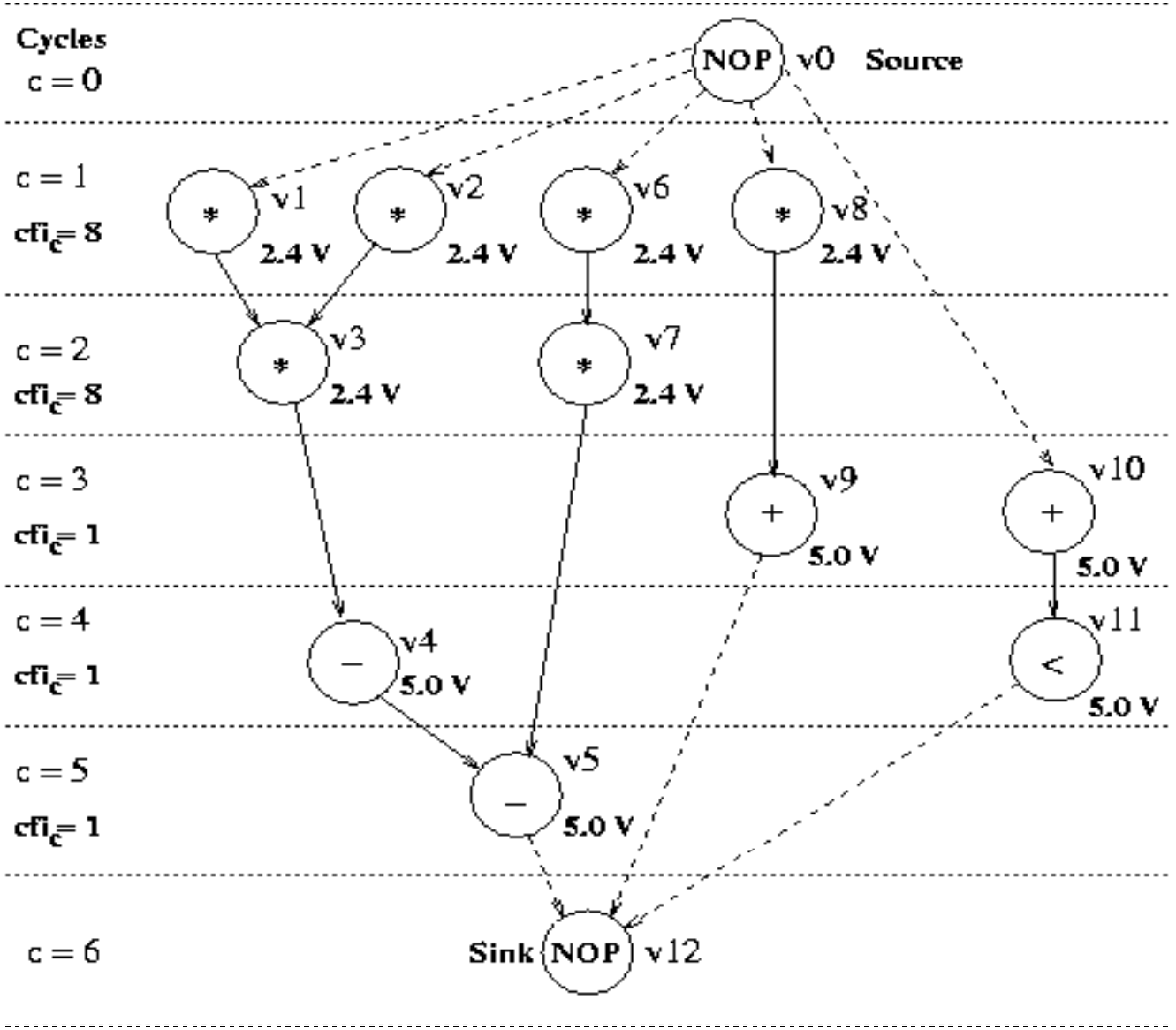


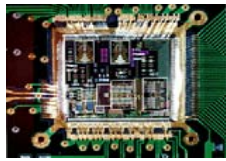
Cycles	c5	c4	c3	c2	c1	c6	c0
Priorities	0	1	2	3	4	5	6

Table : $T_c = 2\ T_{cp}$ or $1.75\ T_{cp}$

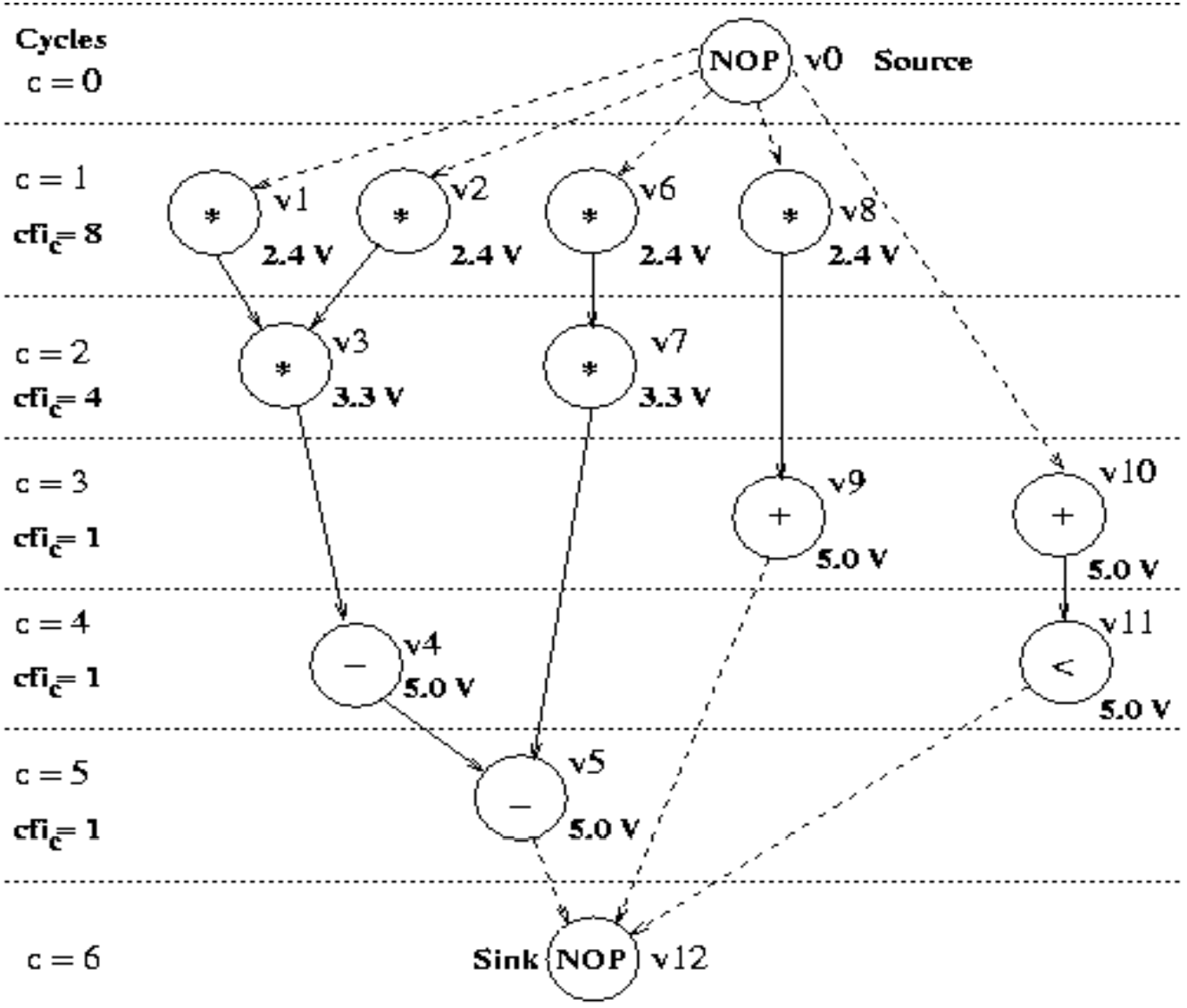


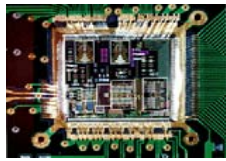
TC-DFC : Schedule : $T_c = 2.0T_{cp}$



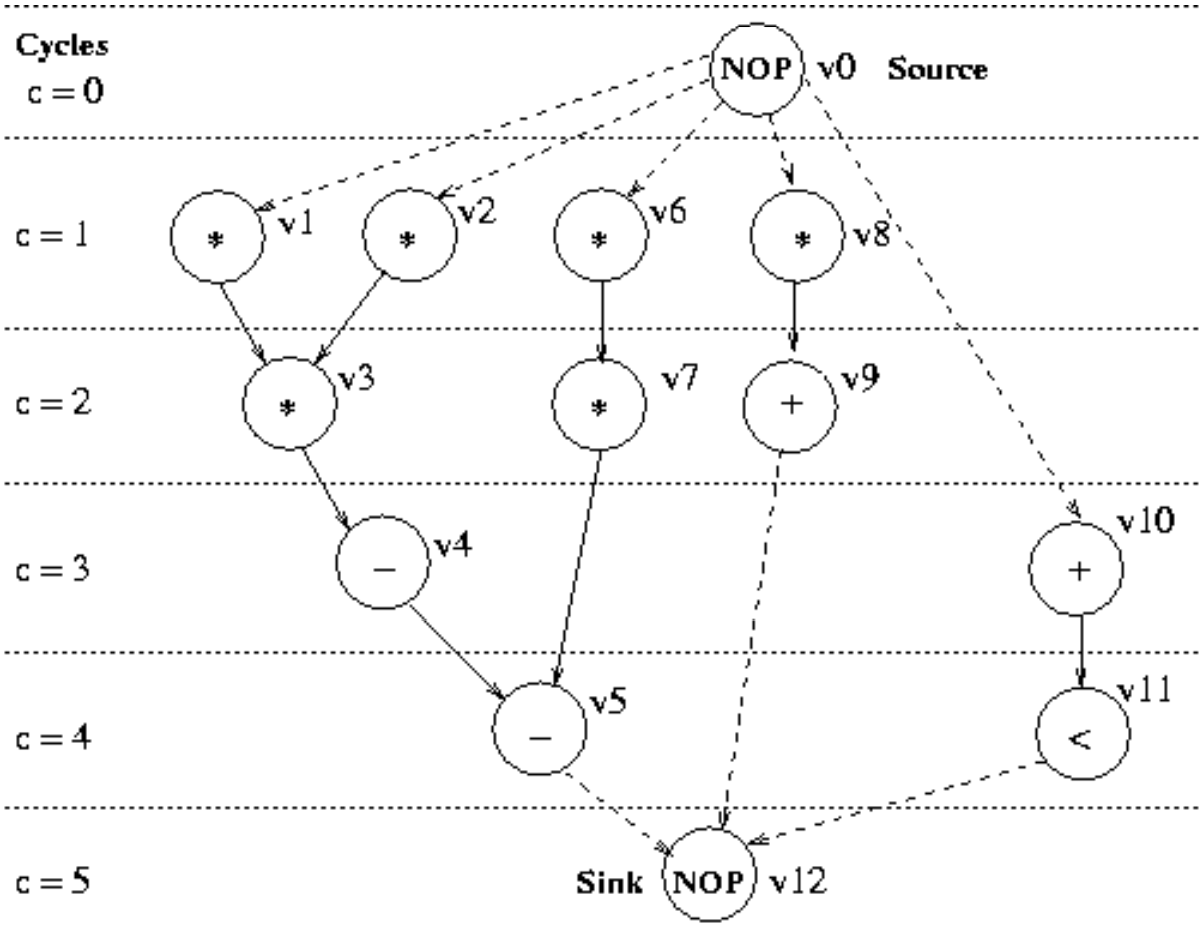


TC-DFC : Schedule : $T_c = 1.75T_{cp}$



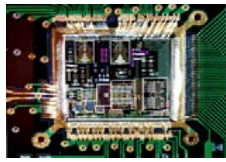


TC-DFC : Intermediate Schedule

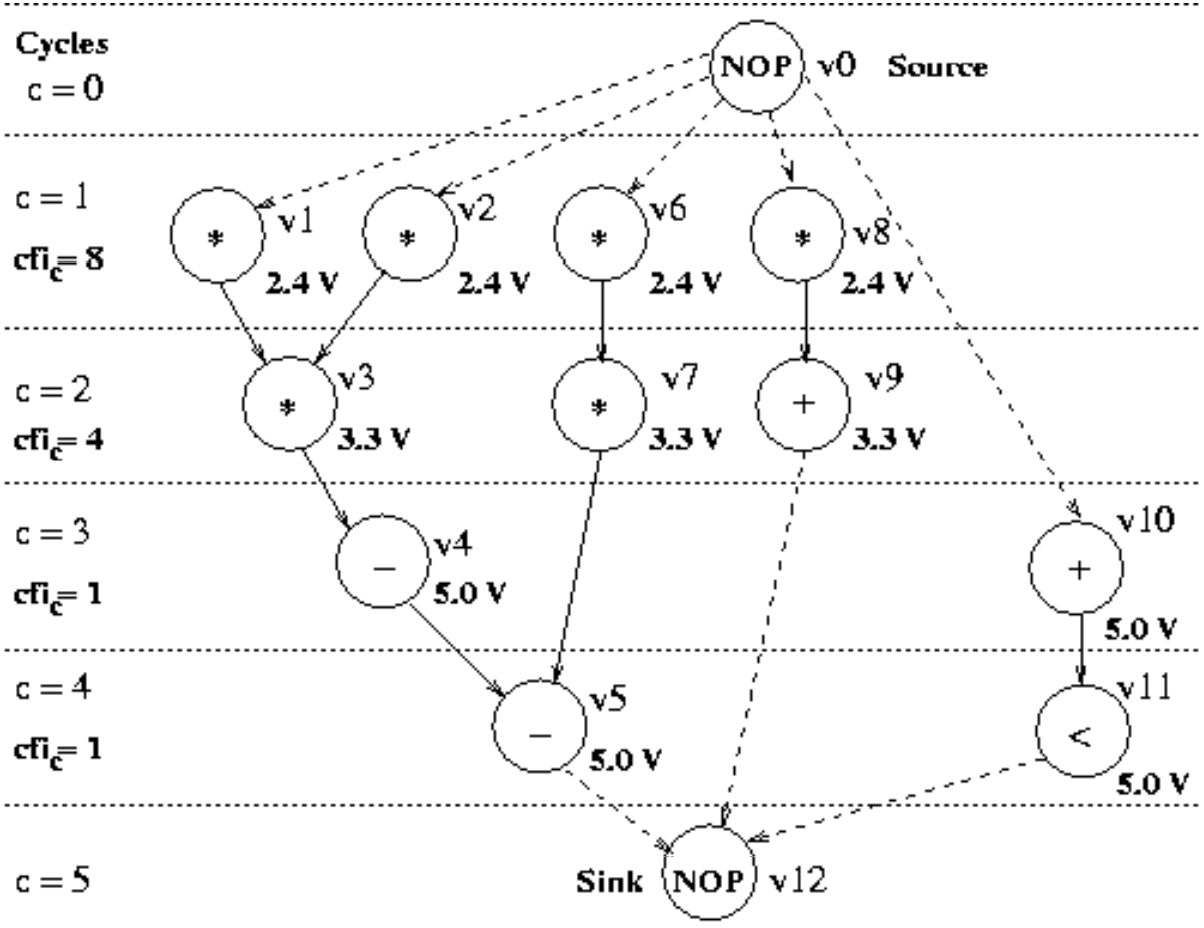


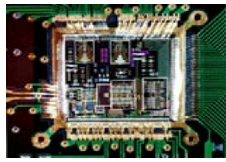
Cycles	c4	c3	c2	c1	c5	c0
Priorities	0	1	2	3	4	5

Table : $T_c = 1.5\ T_{cp}$



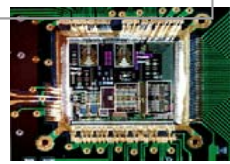
TC-DFC Schedule : $T_c = 1.5T_{cp}$



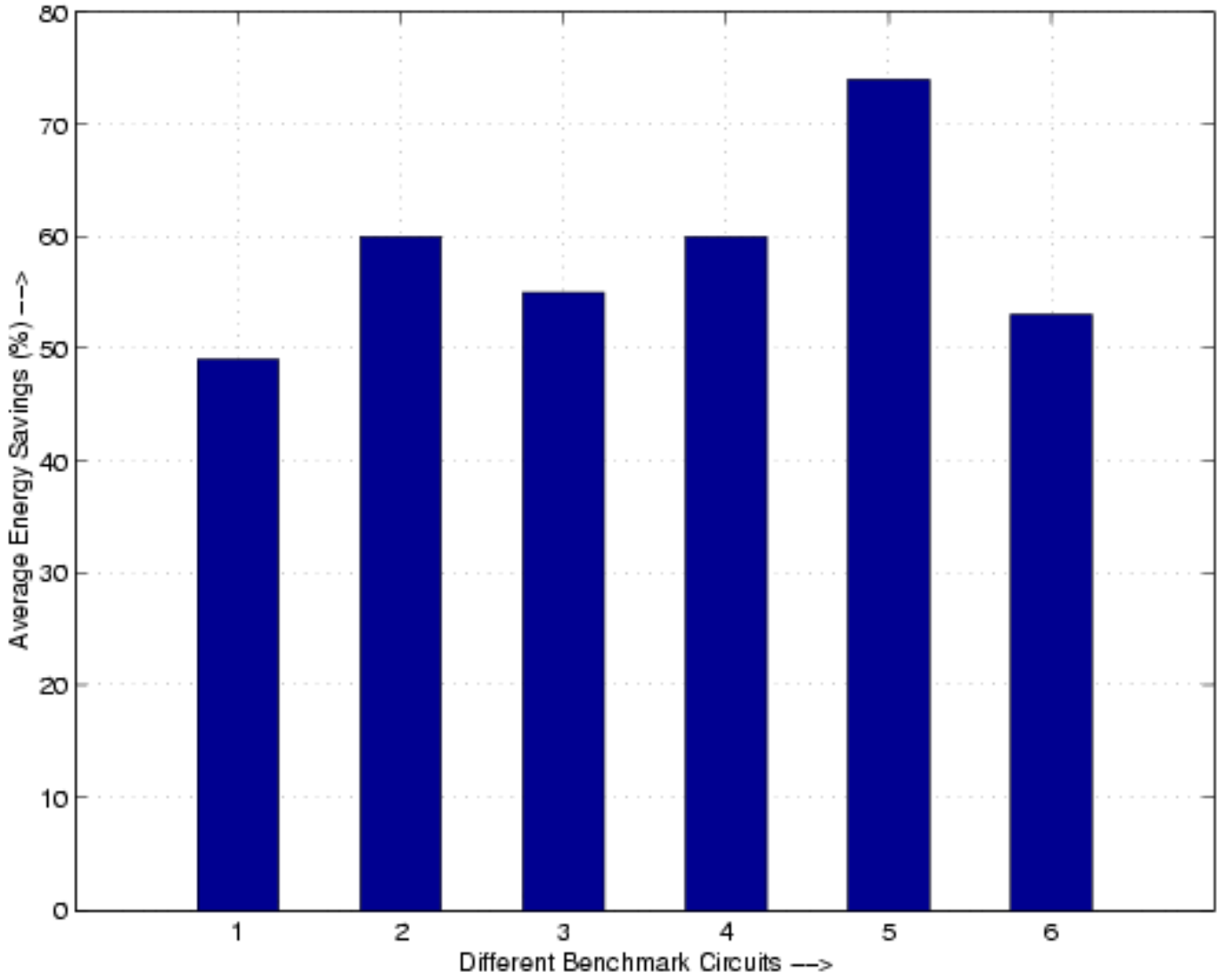


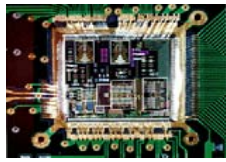
TC-DFC : Savings for different benchmarks

Benchmarks	Time Constraints (ns)	$E_{single}\,(pJ)$	$E_{dynamic}\,(pJ)$	% Savings
1. AR	$1.5T_{cp}$, $1.75T_{cp}$, $2.0T_{cp}$	36186	21491, 18139, 15274	40.61, 46.61, 57.79
2. BPF	$1.5T_{cp}$, $1.75T_{cp}$, $2.0T_{cp}$	27672	15187, 9350, 8249	45.12, 66.12, 70.19
3. EWF	$1.5T_{cp}$, $1.75T_{cp}$, $2.0T_{cp}$	19422	12335, 8814, 5341	36.49, 54.62, 72.50
4. FDCT	$1.5T_{cp}$, $1.75T_{cp}$, $2.0T_{cp}$	30675	14611, 14489, 7714	52.37, 52.77, 74.85
5. FIR	$1.5T_{cp}$, $1.75T_{cp}$, $2.0T_{cp}$	18696	4910, 4877, 4820	73.74, 73.91, 74.21
6. HAL	$1.5T_{cp}$, $1.75T_{cp}$, $2.0T_{cp}$	13614	7808, 6821, 4449	42.64, 49.90, 67.31



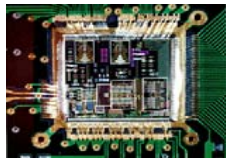
TC-DFC : Average savings for 3 time constraints





TC-DFC : Energy savings using different algorithms

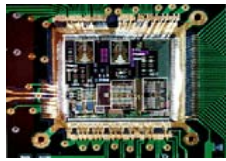
	TC-DFC	Chang[3]	Shiue[14]	Manzak[9]
ARF	41-58	40-63	38-76	25-61
BPF	45-70	-	-	-
EWF	36-73	44-69	13-76	10-55
FDCT	52-75	43-69	-	-
FIR	74-74	-	-	-
HAL	43-67	41-61	22-77	19-72



RC-DFC Algorithm

Input: Unscheduled DFG, Resource constraints (Number of resources at different operating voltages), Maximum number of allowable operating frequencies

Output: Scheduled DFG with frequency assignment for each control step (cycle)



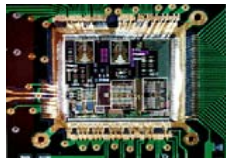
RC-DFC : Frequency and Resource LUTs

FU in a cycle	Frequency priority order
Multipliers only	$MULT_{Low}$, $MULT_{Med}$, $MULT_{High}$
Both Multipliers and ALUs	$MULT_{Low}$, ALU_{Low}, $MULT_{High}$
ALU only	ALU_{High}, ALU_{Med}, ALU_{Low}

Frequency selection look up from left to right

	Multipliers			ALUs		
	2.4V	3.3V	5.0V	2.4V	3.3V	5.0V
For each clock cycle	1	2	1	1	1	0

Resource look up from left to right



RC-DFC Scheduling Algorithm

Step 1 : Get the ASAP and ALAP schedule

Step 2 : Modify the ASAP and ALAP schedules using the number of resources without operating voltage constraint

Step 3 : Total No. of control steps = Max (ASAP steps, ALAP steps)

Step 4 : Construct the Freq. Selection and Resource Assignments LUTs

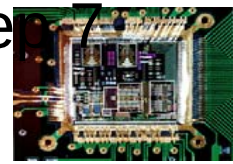
Step 5 : Find the vertices having zero and non-zero mobility and assume ASAP schedule as the current schedule

Step 6 : Do voltage and freq. assignment using current schedule

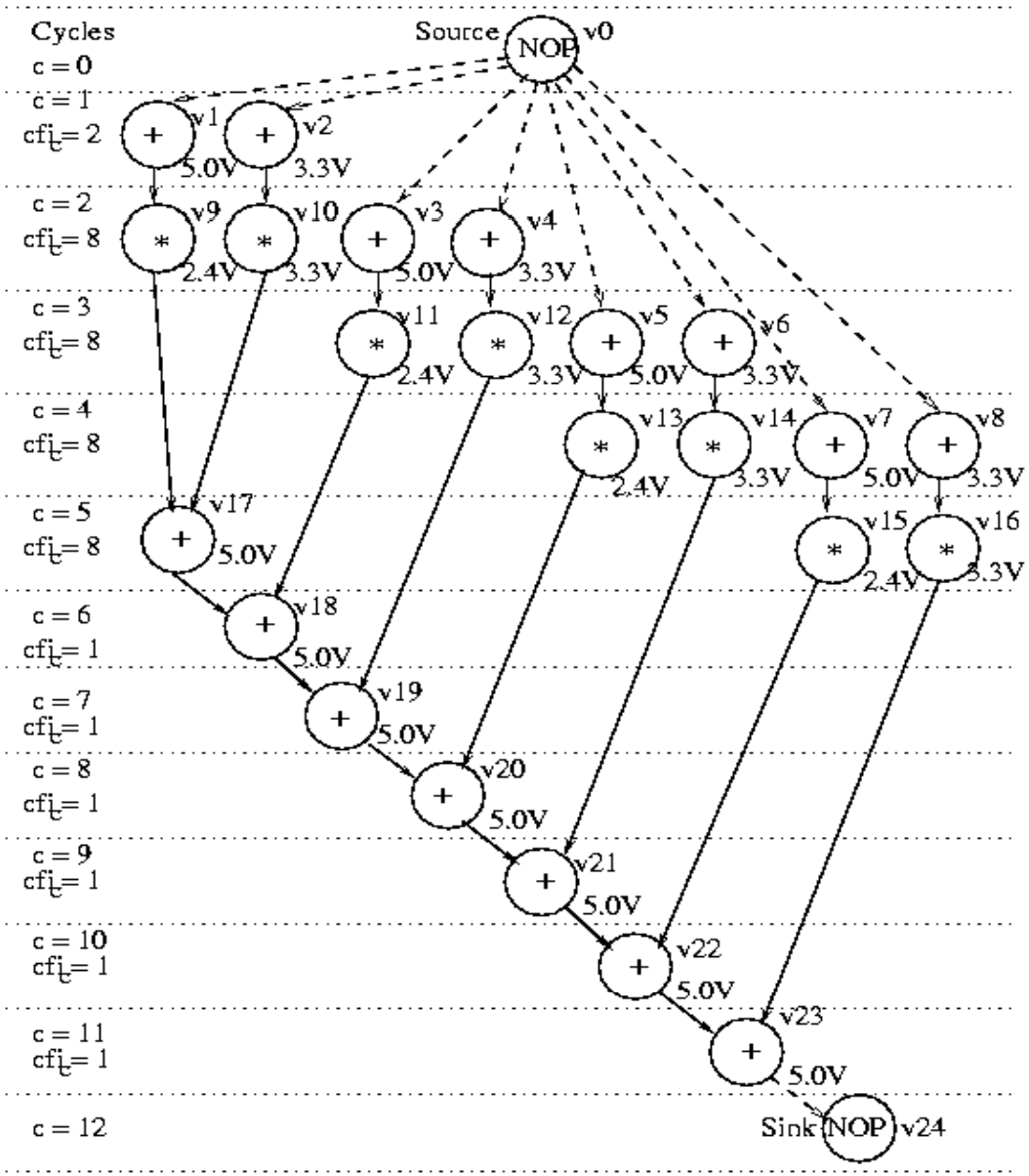
Step 7 : Taking non-zero mobility vertex find proper time stamp for it using LUTs such that number of level conversions needed is minimum

Step 8 : Adjust current schedule, predecessor / successor time stamp, resource assignment LUT and repeat Step 6 and Step 7

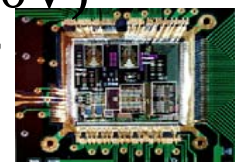
Step 9 : Find cycle frequency index for each cycle



RC-DFC : A Scheduled DFG (FIR benchmark)

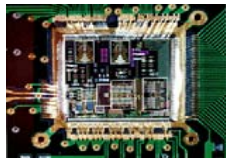


FIR ; Resource constraint : MULT(1 at 2.4V, 1 at 3.3V) and (1 ALU at 5.0V)



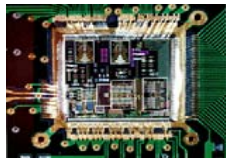
RC-DFC : Resource constraints used in our experiment

Multipliers		ALUs		Serial
3.3V	5.0V	3.3V	5.0V	No
2	1	1	1	1
3	0	1	1	2
2	0	0	2	3
1	1	0	2	4
1	1	0	1	5
2	0	0	1	6

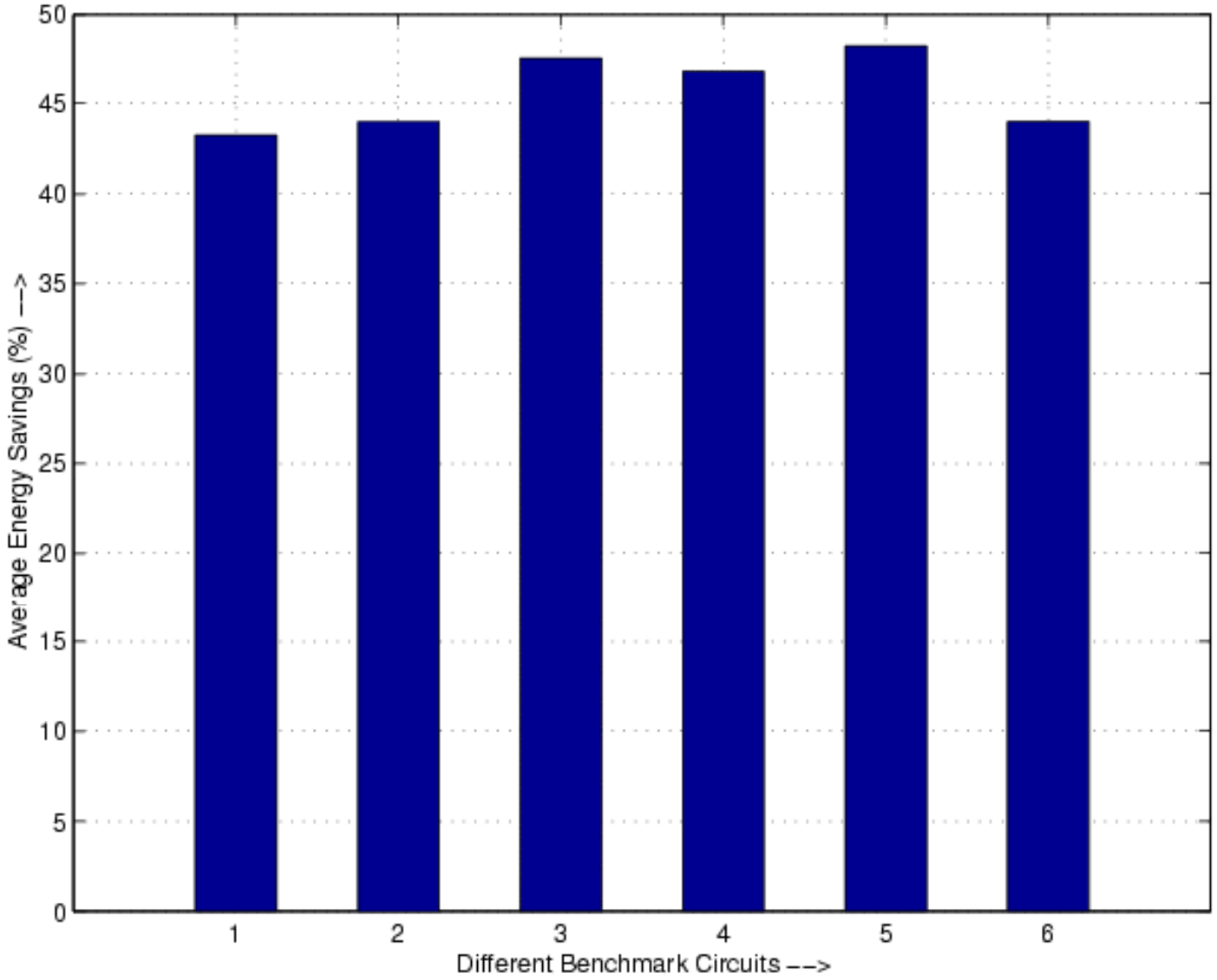


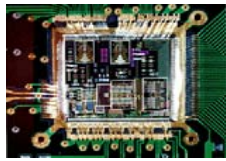
RC-DFC : Savings for different benchmarks

	Resource Cons.	Energy (SF) (pJ)	Energy (DFC) (pJ)	% Savings
ARF	1	36168	21768	40
	2	36168	18205	50
	3	36168	19065	47
BPF	1	27654	16491	40
	2	27654	14175	49
	3	27654	14827	46
EWF	1	19404	10802	44
	2	19404	10802	44
	3	19404	10853	39
FIR	1	18678	9979	47
	2	18678	9979	47
	3	18678	10126	45



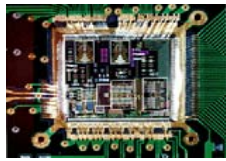
RC-DFC : Average Savings for benchmarks





RC-DFC : Energy savings using different algorithms

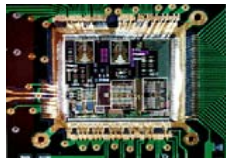
	RC-DFC	Shiue[14]	Sarrafzadeh[13]	Johnson[6]
ARF	24-58	11-14	16-20	16-59
BPF	27-56	-	-	-
EWF	38-61	14-14	13-32	11-50
FDCT	41-63	-	-	-
FIR	20-67	-	16-29	28-73
HAL	29-62	19-28	-	-



Related Research

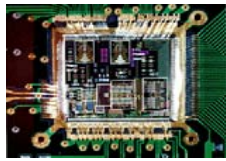
Low Power Scheduling using Voltage Reduction

- Johnson & Roy [6], 1997 – MOVER algorithm, multiple voltage
- Chang & Pedram [3], 1997 – dynamic programming
- Kumar & Bayoumi [7], 1999 – variable voltage
- Sarrafzadeh and Raje [13], 1999 - dynamic prog., geometric
- Schiue & Chakrabarti [14], 2000 – list based, multiple voltage
- Manzak & Chakrabarti [9], 2002 - energy minimization using Lagrange multiplier method
- And many other works



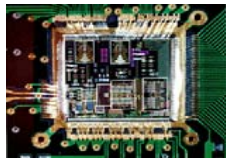
Related Research : MOVER [6]

- ILP formulations of multiple supply voltage scheduling (MOVER)
- Minimize energy consumption
- The DFG is partitioned into groups :
  - Higher voltage operation group
  - Lower voltage operation group
  - MOVER 1st fixes the minimum voltage of the lower group and then fixes the minimum voltage for the upper group
- Handle timing and resource constraints
- Exponential worst-case complexity
- Energy Savings : 0-50%, Area Penalty: 0-170%



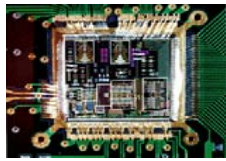
Related Research : Dynamic Programming[3]

- Dynamic Programming for multiple voltage scheduling
- Time-constraints scheduling
- Average energy savings : 40 %
- Non-exponential complexity
- Can handle large circuits, pipeline datapath



Related Research : List-Based [14]

- Multiple voltage scheme
- List based scheduling algorithms: resource constraints based and time constraints based
- Polynomial time complexity algorithms
- Multiple voltage scheduling and reduce switching activity
- Savings : Latency constrained case : 13-77%



Conclusions

- A time-constrained scheduling algorithm discussed
- In DFC, frequency can be switched dynamically
- Lowering frequency with voltage can save energy
- For TC-DFC average energy savings is 46% to 68%
- As the time-constraint is relaxed the energy savings increases
- For RC-DFC average energy savings is 20% to 67%
- For the circuits having almost equal number of addition and multiplier operations savings is maximum