CSCE 5730/4730: Digital CMOS VLSI Design

Assignment # 3, Total Marks = 100.
Assigned Date: 21st Oct 2009 (Wed), Due Date: 28th Oct 2009 (Wed)
Instructor: Dr. Saraju P. Mohanty

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1. Design a D-latch using 45nm technology in LTspice. Perform simulations to prove its functionality and transparent property.