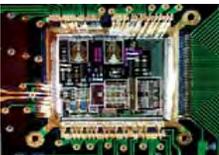# Lecture 2: CMOS Logic

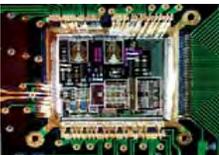## CSCE 5730
Digital CMOS VLSI Design

Instructor: Saraju P. Mohanty, Ph. D.

NOTE: The figures, text etc included in slides are borrowed from various books, websites, authors pages, and other sources for academic purpose only. The instructor does not claim any originality.

Lecture Outline

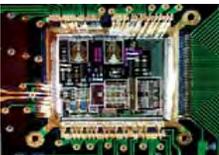- MOS Transistors
- CMOS Logic

Introduction

- Integrated circuits: many transistors on one chip.
- *Very Large Scale Integration* (VLSI): very many
- *Complementary Metal Oxide Semiconductor*
  - Fast, cheap, low power transistors
- How to build your own simple CMOS chip
  - CMOS transistors
  - Building logic gates from transistors
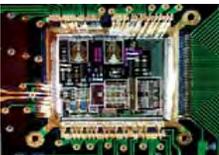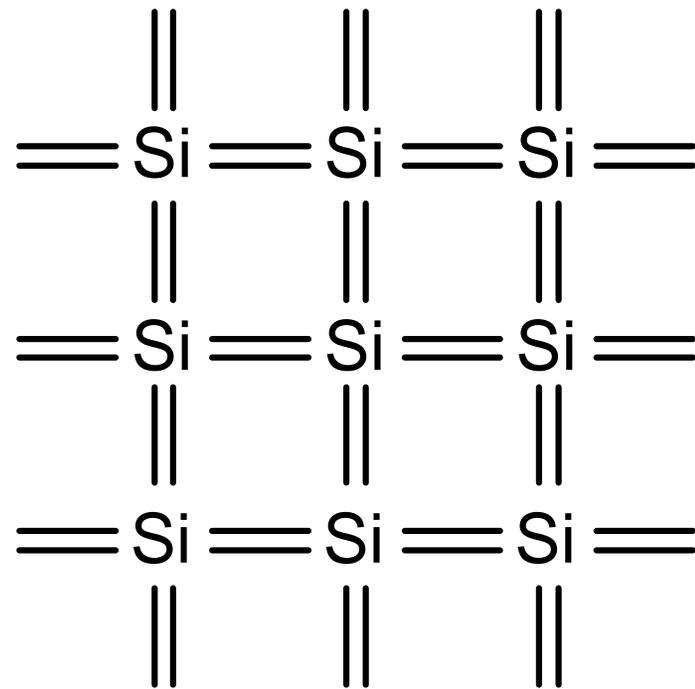 - Transistor layout and fabrication
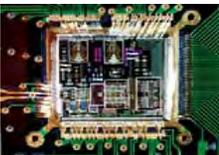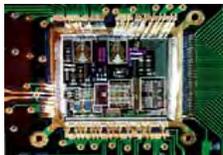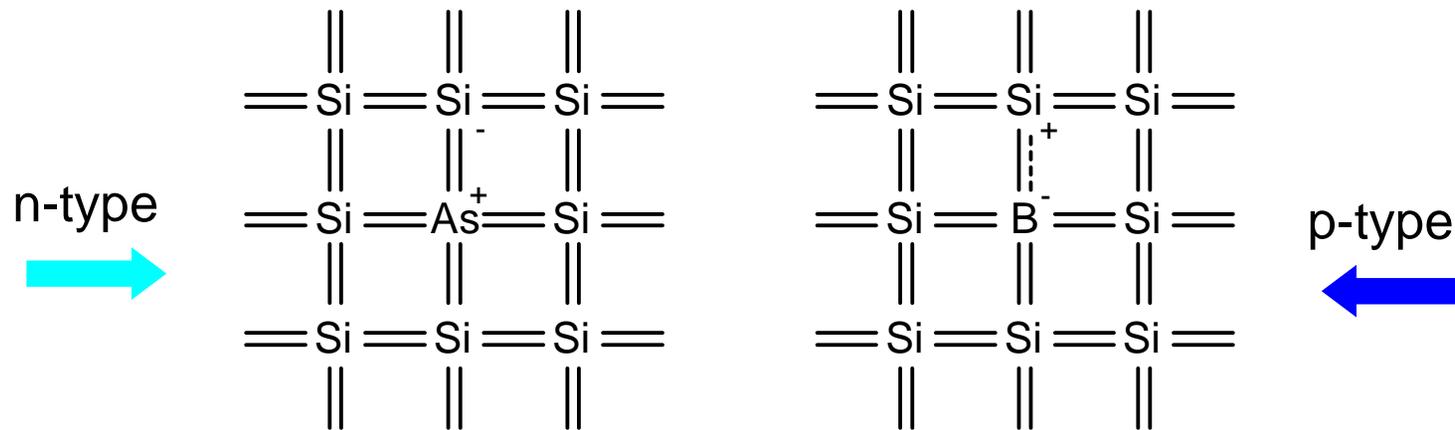
Silicon

Silicon Lattice

- Transistors are built on a silicon substrate.

- Silicon is a Group IV material.

- Forms crystal lattice with bonds to four neighbors.

$$
\begin{array}{ccc}
\| & \| & \| \\
=Si= & Si= & Si= \\
\| & \| & \| \\
=Si= & Si= & Si= \\
\| & \| & \| \\
=Si= & Si= & Si= \\
\| & \| & \|
\end{array}
$$

Dopants

- Silicon is a semiconductor.
- Pure silicon has no free carriers and conducts poorly.
- Adding dopants increases the conductivity.
- Group V: extra electron (n-type).
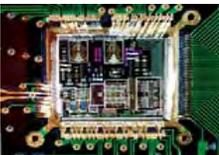- Group III: missing electron, called hole (p-type).

n-type

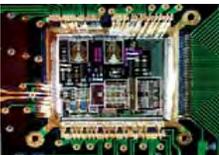$$=Si=Si=Si=$$
$$=Si=As^+=Si=$$
$$=Si=Si=Si=$$

p-type

$$=Si=Si=Si=$$
$$=Si=B=Si=$$
$$=Si=Si=Si=$$

Why Silicon?

Could any other group IV metal serve purpose ?

Key Advantages:

- Available abundantly in nature.

- Has excellent physical and electrical properties.
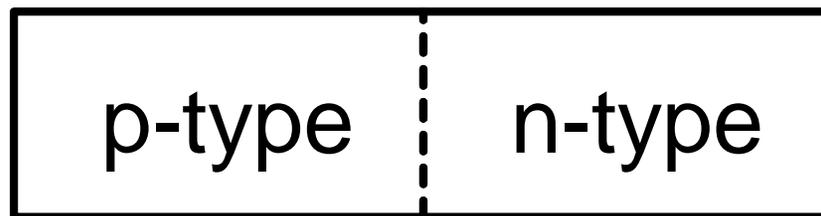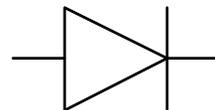
- Matured chemistry for fabrication.

Devices

p-n Junctions

- A junction between p-type and n-type semiconductor forms a diode.
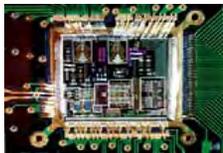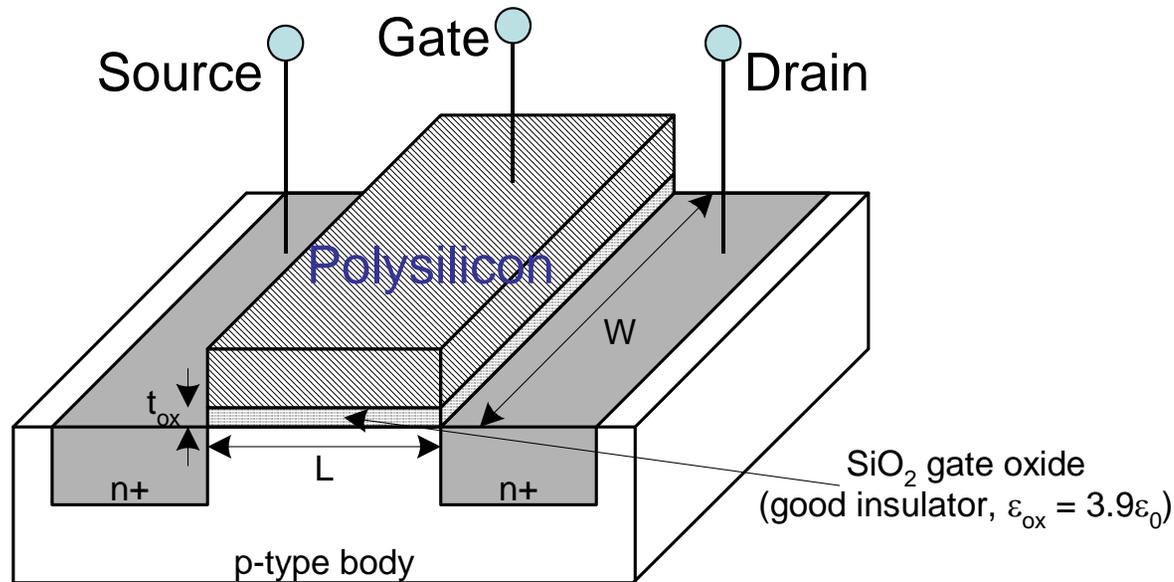- Current flows only in one direction.

p-type | n-type

anode   cathode

symbol

MOS Transistor

- Four terminals: gate, source, drain, body (bulk, or substrate)
- Gate – oxide – body stack looks like a capacitor
  - Gate and body are conductors
  - SiO_2 (oxide) is a very good insulator
  - Called metal – oxide – semiconductor (MOS) capacitor
 - Even though gate is no longer made of metal

Source   Gate   Drain

Polysilicon

W

t_{ox}

L

n+   n+

SiO_2 gate oxide
(good insulator, $\varepsilon_{ox} = 3.9\varepsilon_0$)

p-type body

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NMOS Operation

- Body is commonly tied to ground (0 V).
- When the gate is at a low voltage:
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF
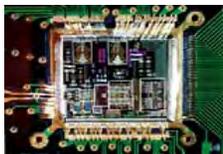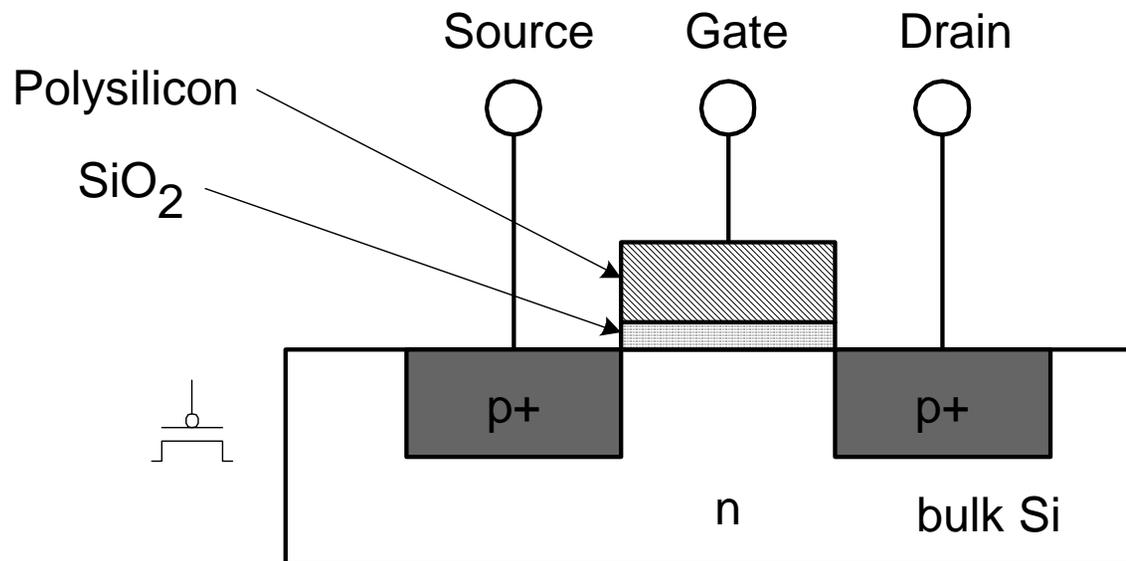 - No current flows, transistor is OFF
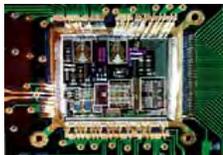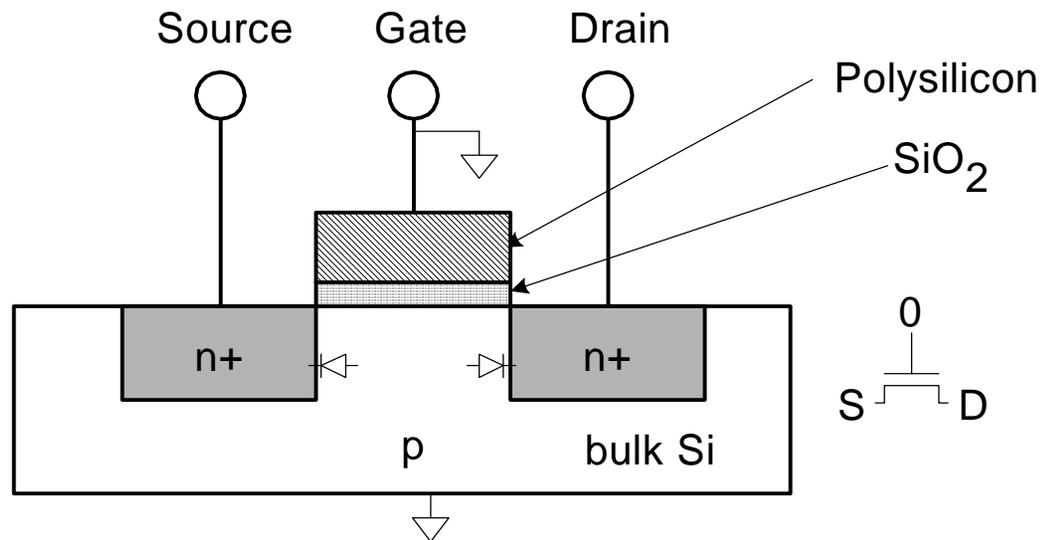
NMOS Operation .....

- When the gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted towards gate
  - Inverts a channel under gate to n-type
 - Now current can flow through n-type silicon from source through channel to drain, transistor is ON
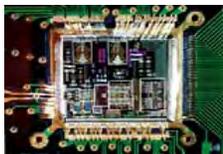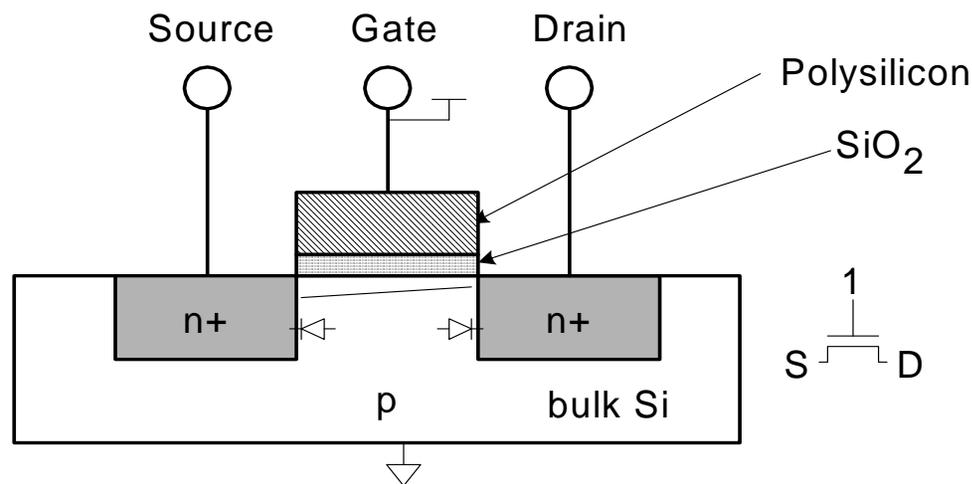
PMOS Transistor

- Similar, but doping and voltages reversed
  - Body tied to high voltage (V_{DD})
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - Bubble indicates inverted behavior

Source Gate Drain

Polysilicon

SiO_2

p+   p+

n   bulk Si

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Power Supply Voltage

- GND = 0 V

- In 1980's, V_{DD} = 5V

- V_{DD} has decreased in modern processes
  - High V_{DD} would damage modern tiny transistors
  - Lower V_{DD} saves power

- V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, …

- For 65nm or 45nm it is approximately 0.7V.
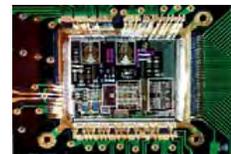
CMOS Circuits with Transistor as Switch
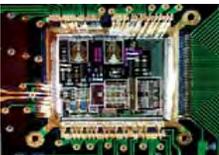
Transistors as Switches: Ideal

- We can view MOS transistors as electrically controlled switches.
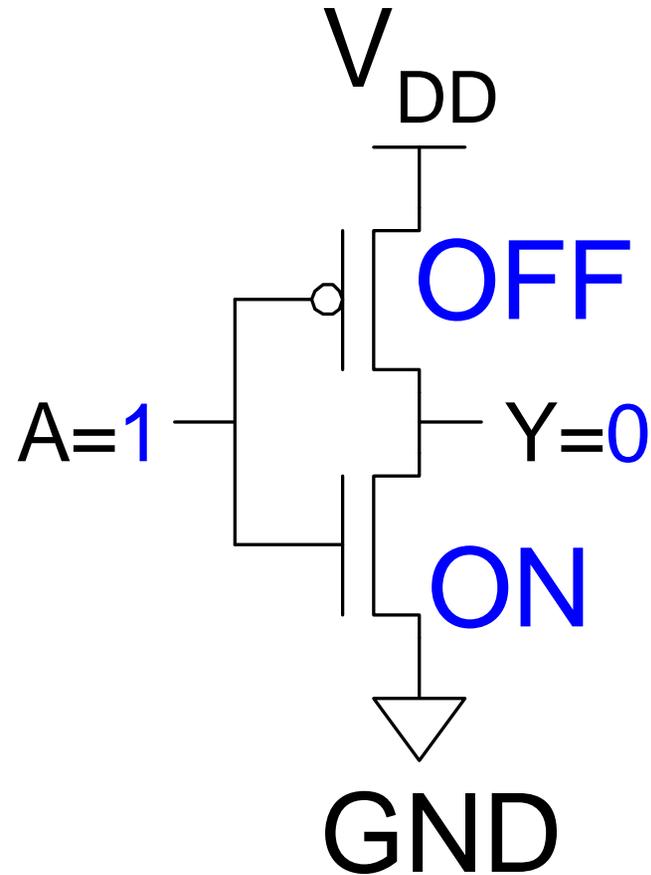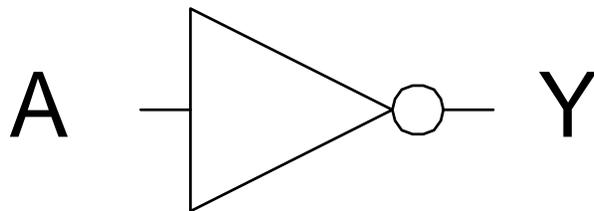
- Voltage at gate controls path from source to drain.

		$g = 0$	$g = 1$

nMOS

d
g
s

d
OFF
s

d
ON
s

pMOS

d
g
s

d
ON
s

d
OFF
s

CMOS Inverter

A	Y
0	
1	

V_{DD}

A ─▷○─ Y

A ─ Y

GND
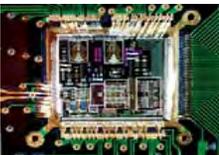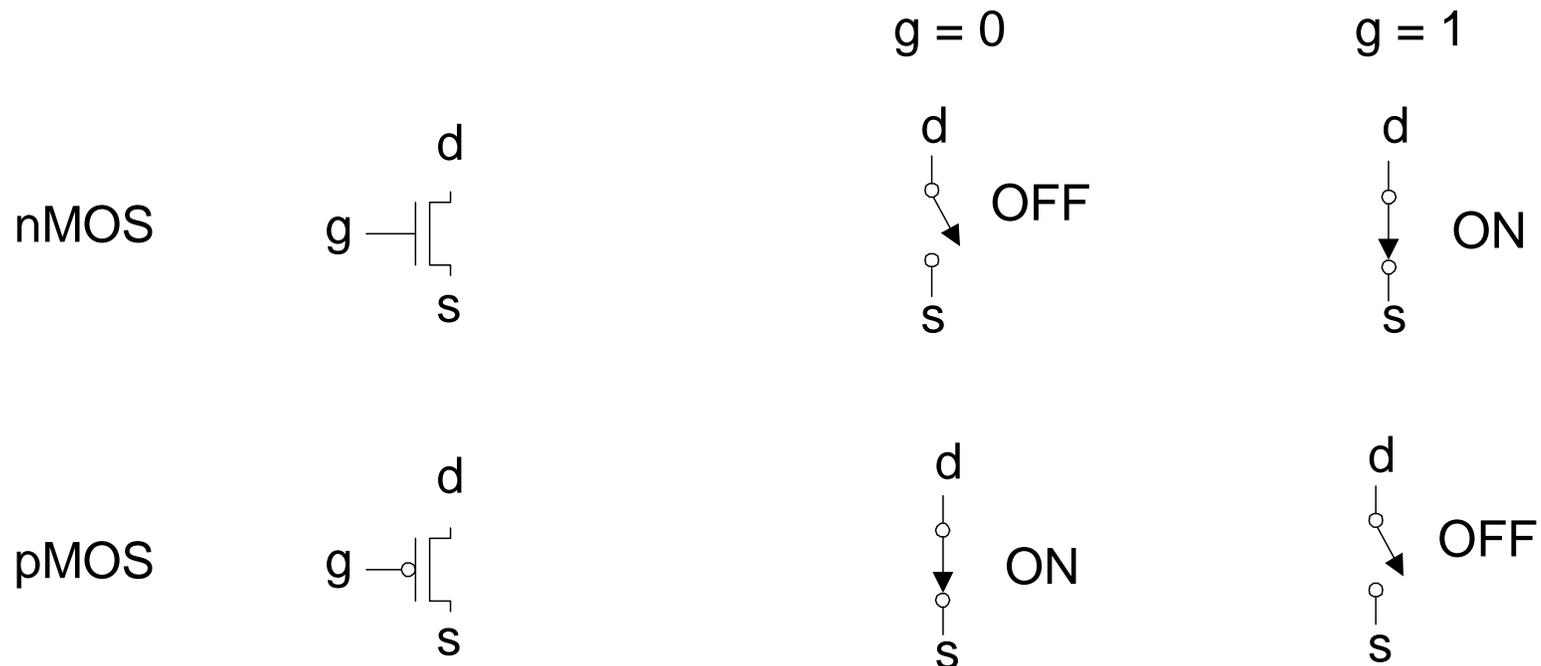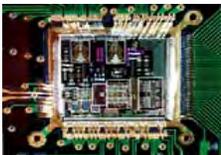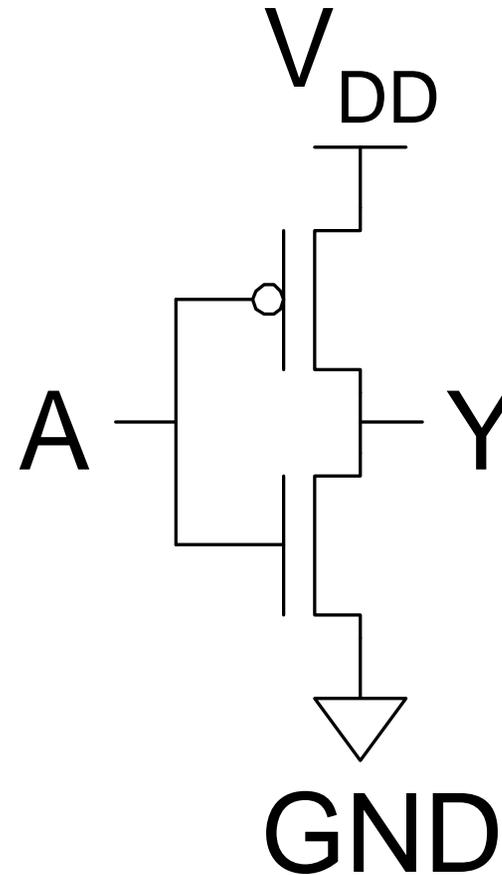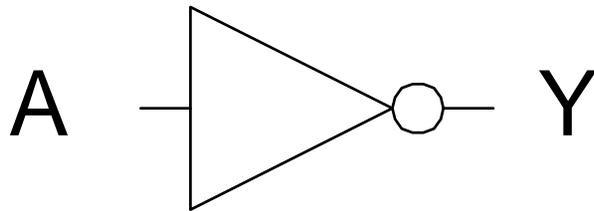
CMOS Inverter

A	Y
0	
1	**0**

A ──▷○── Y

V_{DD}

A=1 ── OFF

Y=0

ON

GND
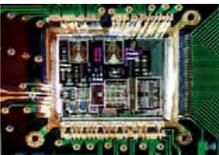
CMOS Inverter

A	Y
0	**1**
1	0

A $\triangleright\!\circ$ Y

V_{DD}

A=0 —| ON

Y=1

OFF

GND
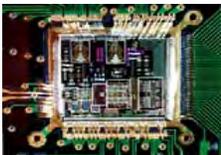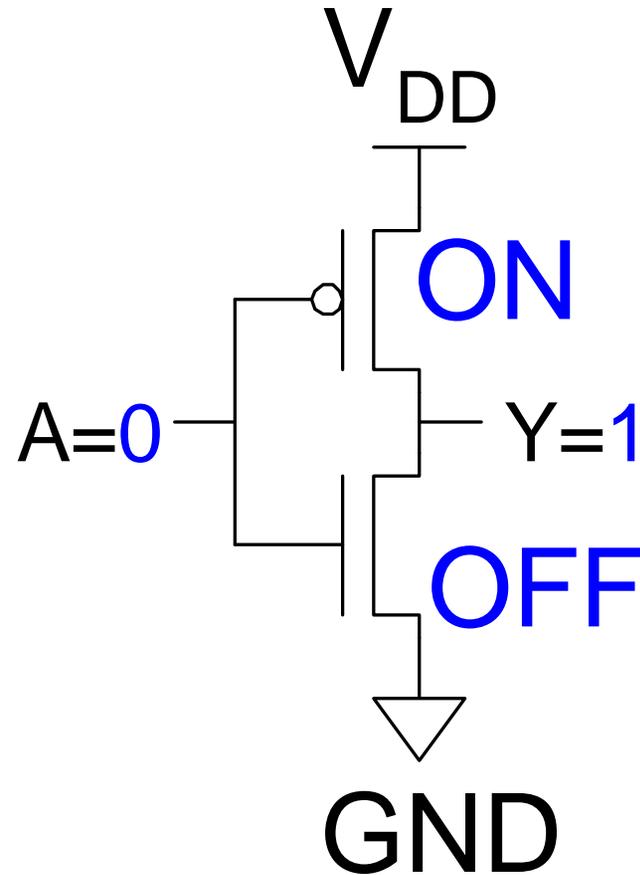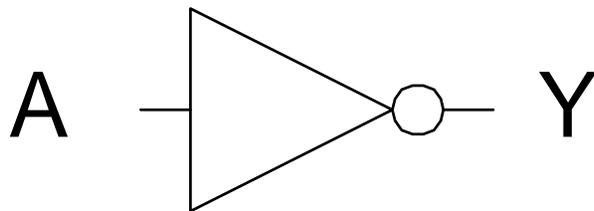
CMOS NAND Gate
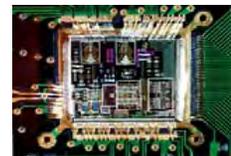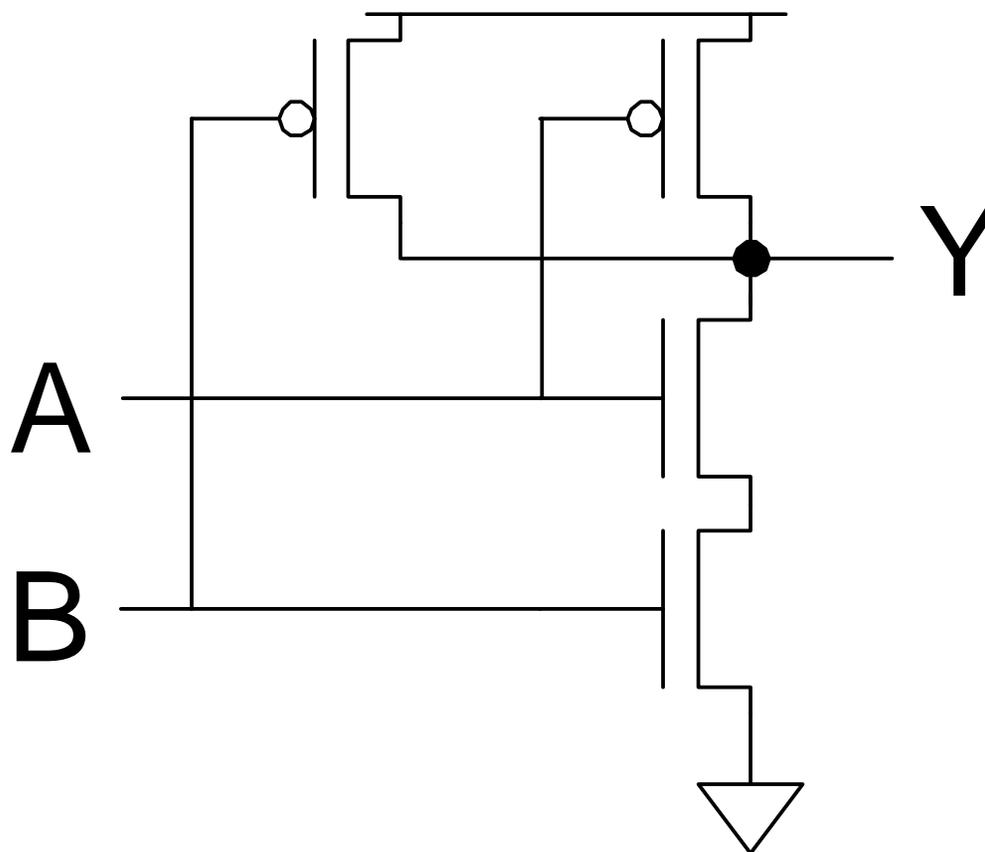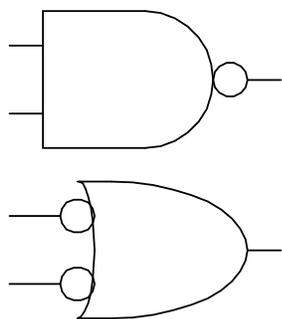
A	B	Y
0	0	
0	1	
1	0	
1	1	

CMOS NAND Gate

A	B	Y
0	**0**	**1**
0	1	
1	0	
1	1	

A=0

B=0

ON   ON

Y=1

OFF

OFF

CMOS NAND Gate

A	B	Y
0	0	1
0	**1**	**1**
1	0	
1	1	

A=0

B=1

OFF   ON

OFF

ON

Y=1

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CMOS NAND Gate

A	B	Y
0	0	1
0	1	1
1	**0**	**1**
1	1	

A=1

B=0

ON   OFF

Y=1

ON

OFF
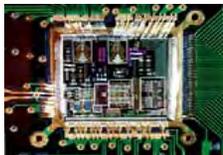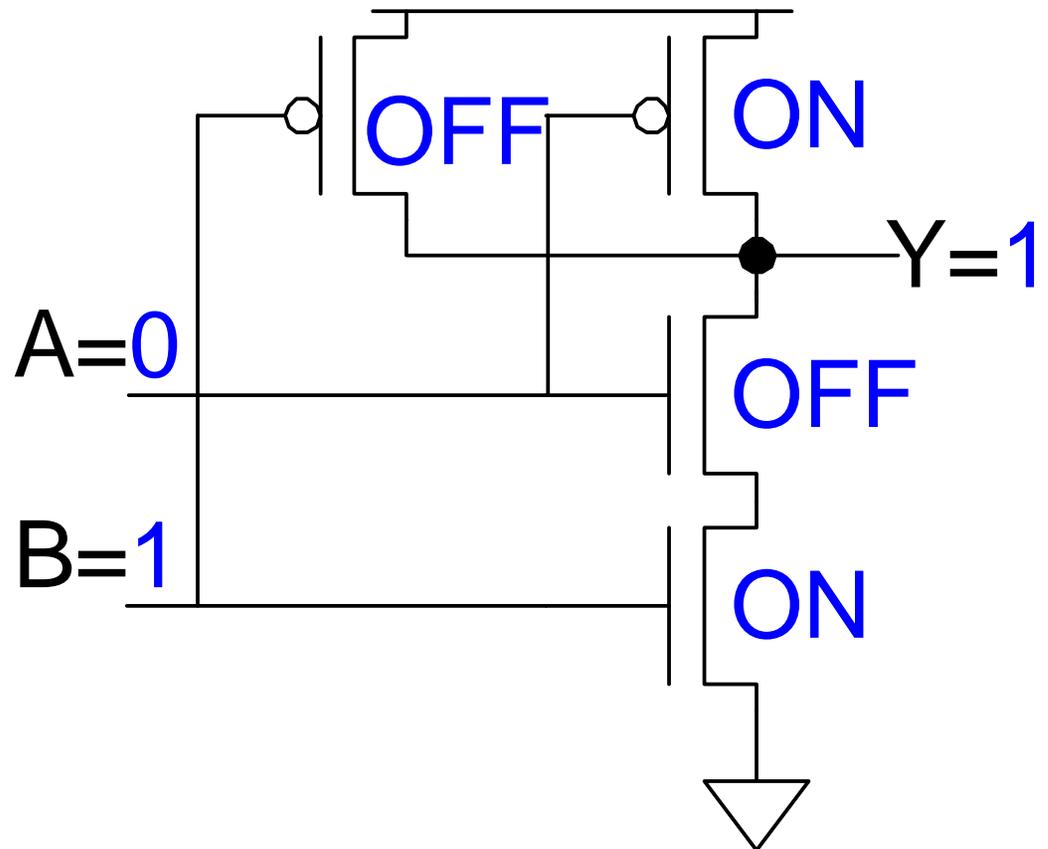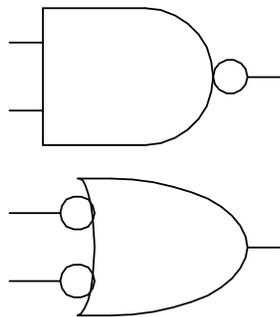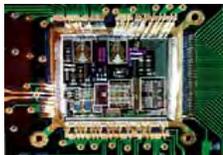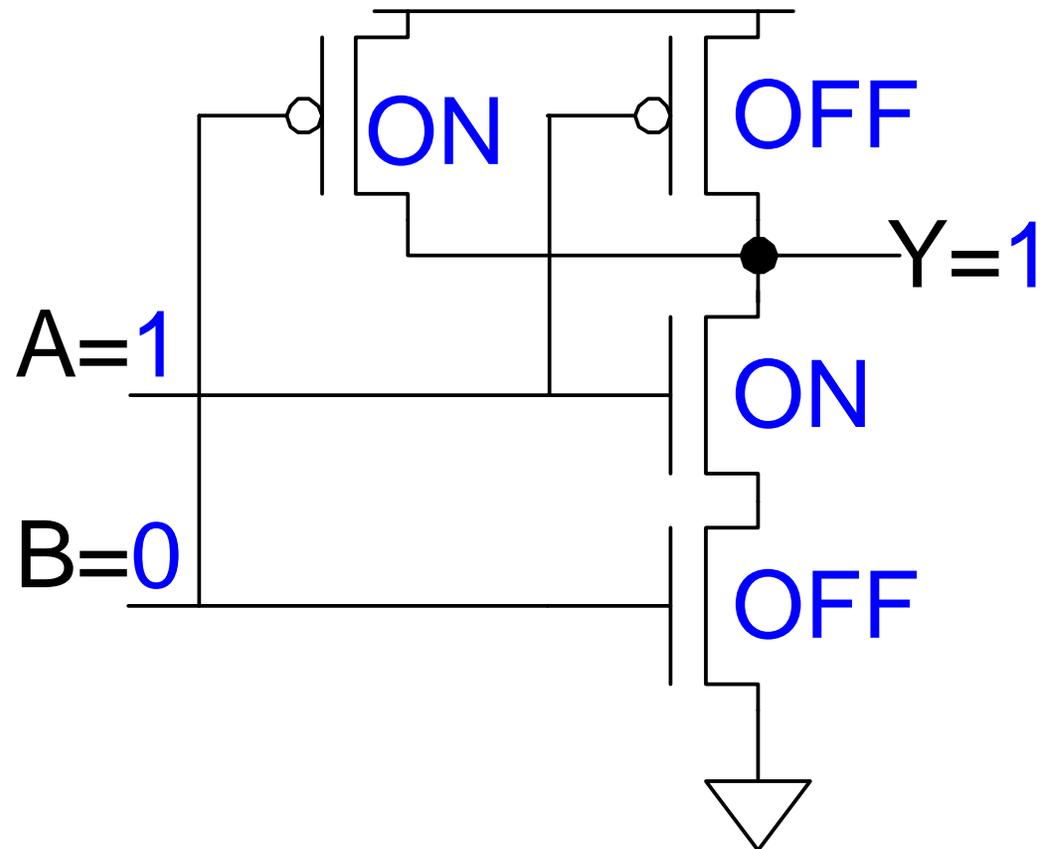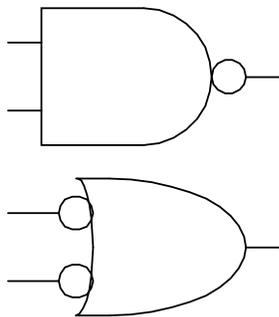
CMOS NAND Gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	**1**	**0**

A=1

B=1

OFF   OFF

Y=0

ON

ON

CMOS NOR Gate (Dual of NAND)

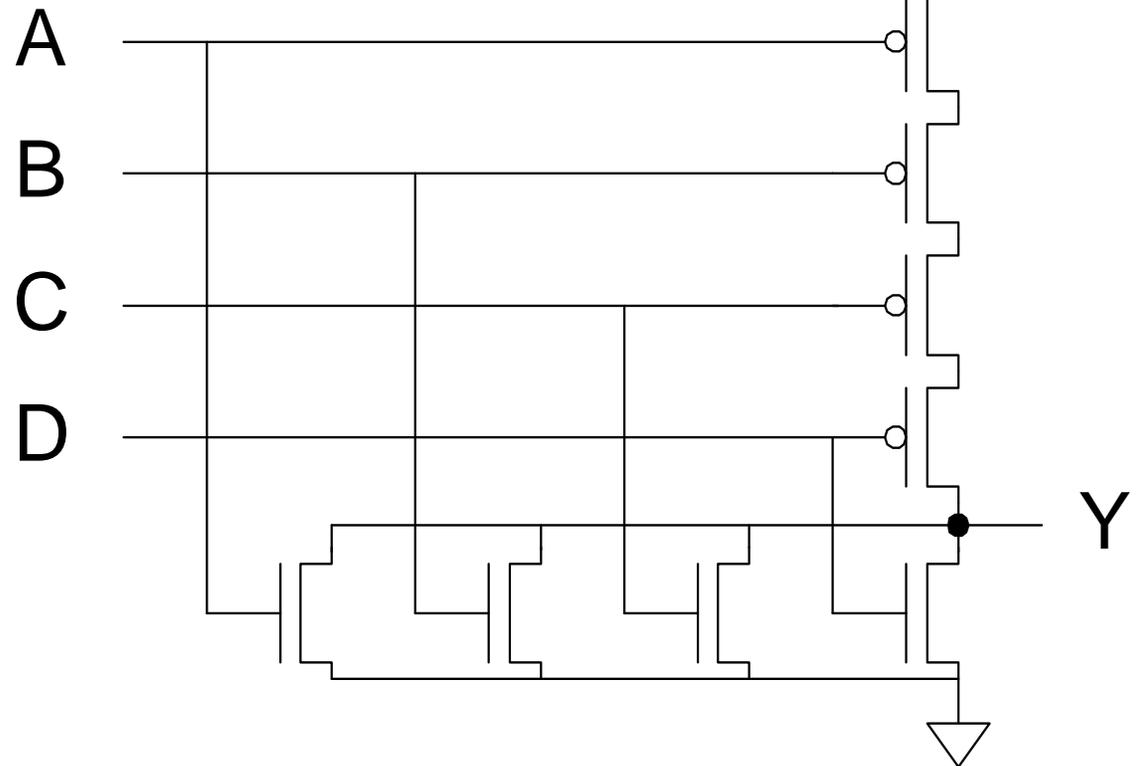| A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0
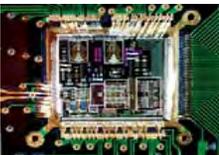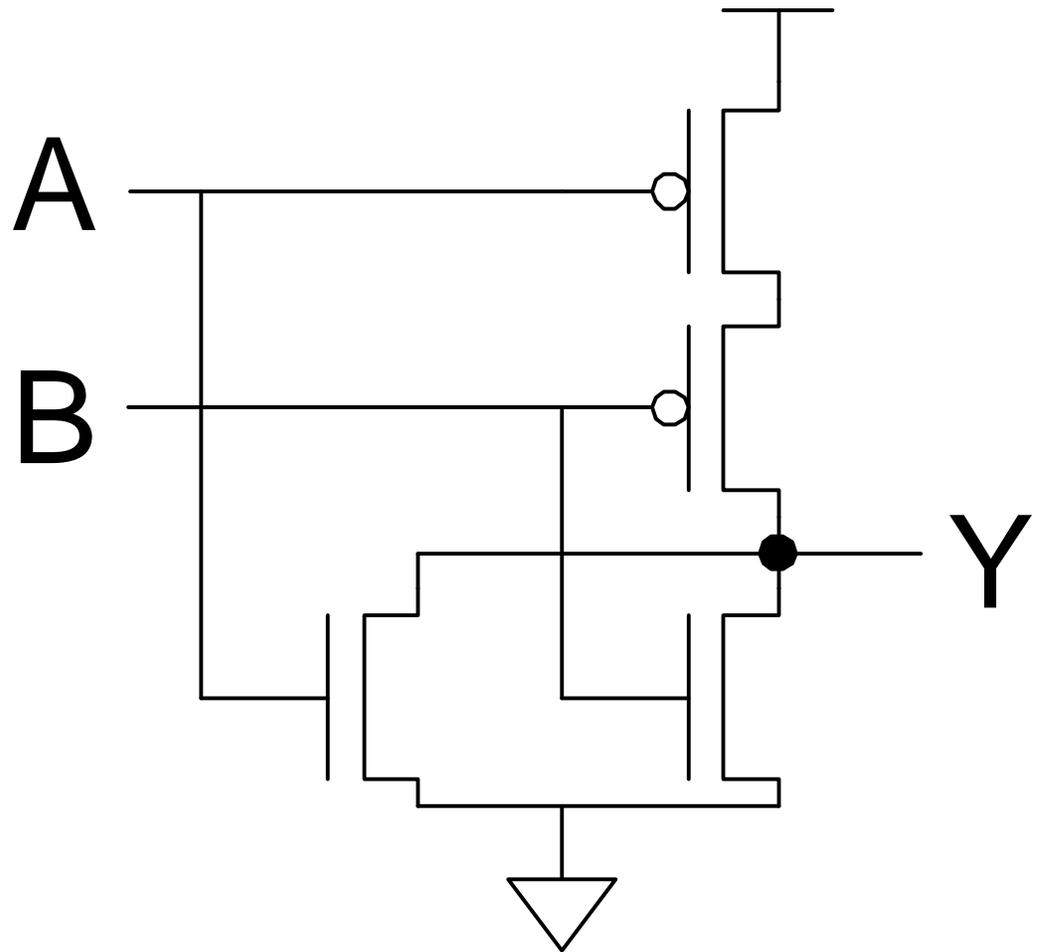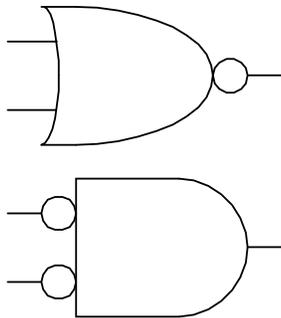
3-input NAND / 4-input NOR Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0
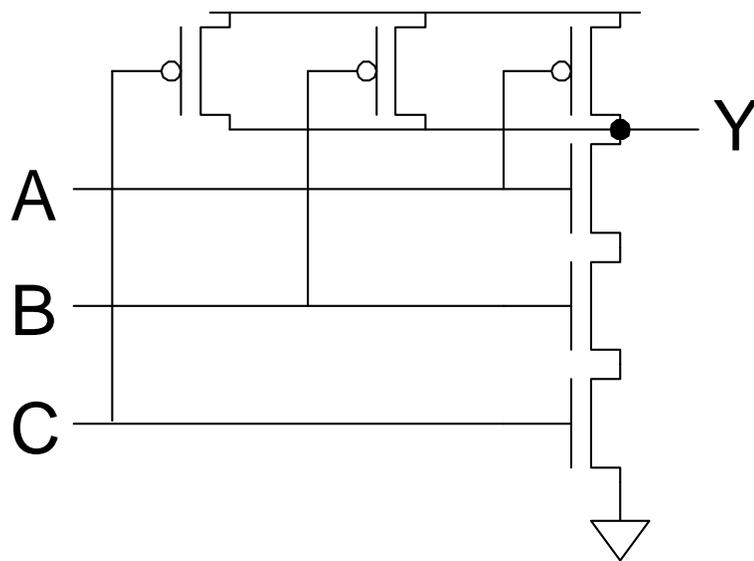
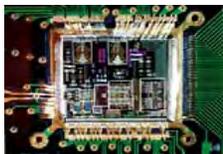4-input NOR Gate
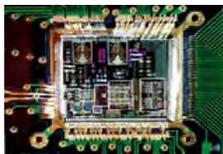
Complementary CMOS : General

- **Complementary CMOS logic gates:**
  - NMOS *pull-down network*
  - PMOS *pull-up network*
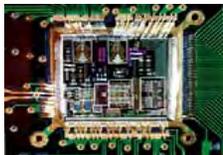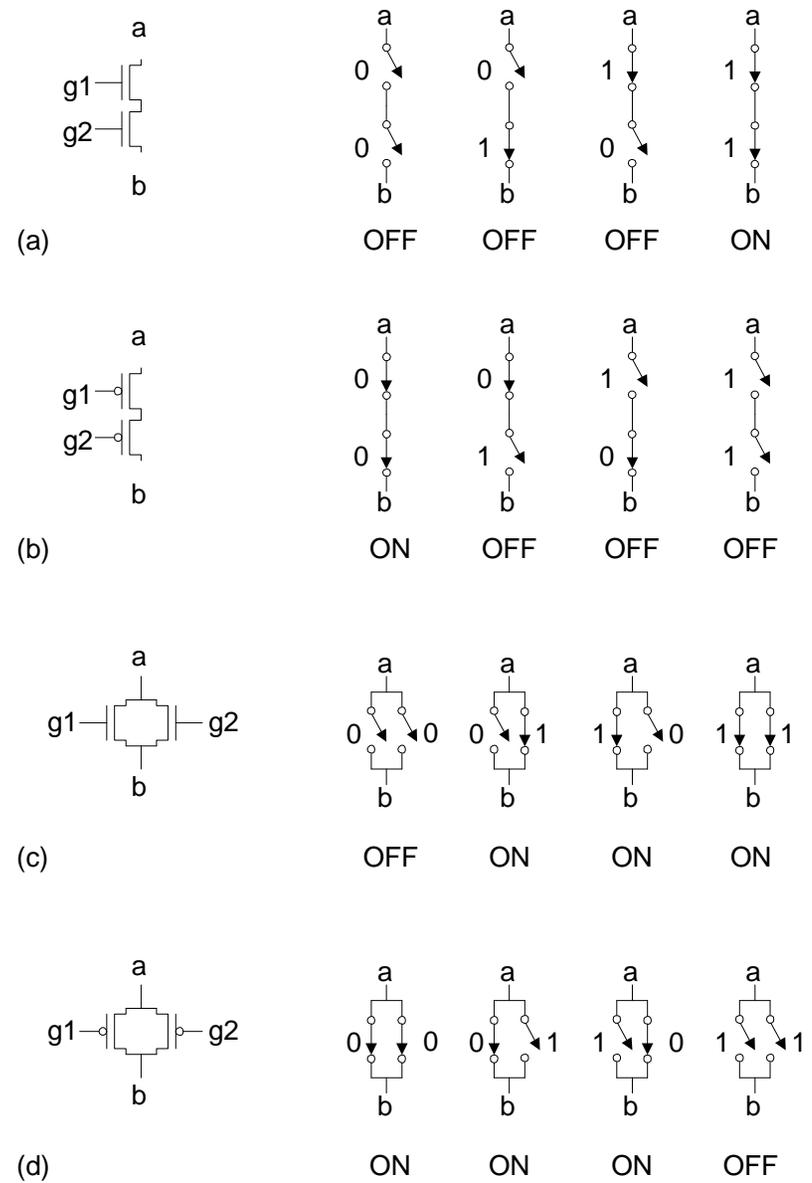 - *a.k.a.* static CMOS

inputs → [pMOS pull-up network] / [nMOS pull-down network] → output
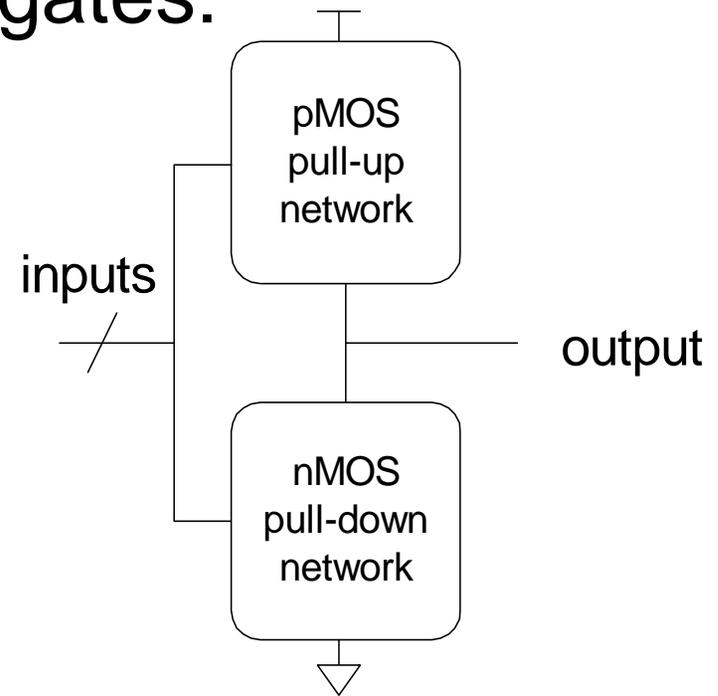
	Pull-up OFF	Pull-up ON
Pull-down OFF	Z (float)	1
Pull-down ON	0	X (crowbar)

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Connection and Behavior of Transistors

- **NMOS: 1 = ON**
- **PMOS: 0 = ON**
- *Series*: both must be ON
- *Parallel*: either can be ON

Conduction Complement

- Complementary CMOS gates always produce 0 or 1.

- Example: NAND gate
  - Series NMOS: Y=0 when both inputs are 1
  - Thus Y=1 when either input is 0
  - Requires parallel PMOS

- Rule of *Conduction Complements*
  - Pull-up network is complement of pull-down
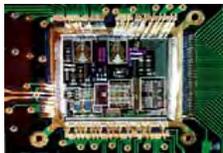 - Parallel -> series, series -> parallel
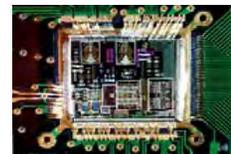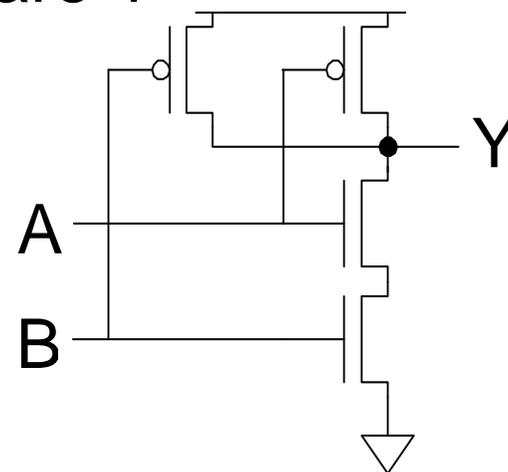
Signal Strength

- *Strength* of signal
  - How close it approximates ideal voltage source?
- V_{DD} and GND rails are strongest 1 and 0.
- NMOS pass strong 0
  - But degraded or weak 1
- PMOS pass strong 1
  - But degraded or weak 0
- Thus, NMOS are best for pull-down network.
- And, PMOS are best for pull-up network.

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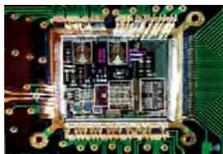
CMOS Transistor Synthesis of Boolean

- Formed using combination of series and parallel switch structures.

- *Compound gates* can do any inverting function.

- Synthesis Steps:

  - Express the function in inverting form.

  - Do NMOS realization of the new function without inverting. Series is AND and parallel is OR.

  - Do PMOS realization which is dual of NMOS. Dual means NMOS becomes PMOS, series becomes parallel and parallel becomes series.

  - Connect the NMOS and PMOS realizations. Connecting point is the output point.

Compound Gates

- ## Example:

$$Y = \overline{A \cdot B + C \cdot D} \ (\text{AND-AND-OR-INVERT})$$

(a)

(b)

(c)

(d)

(e)

(f)

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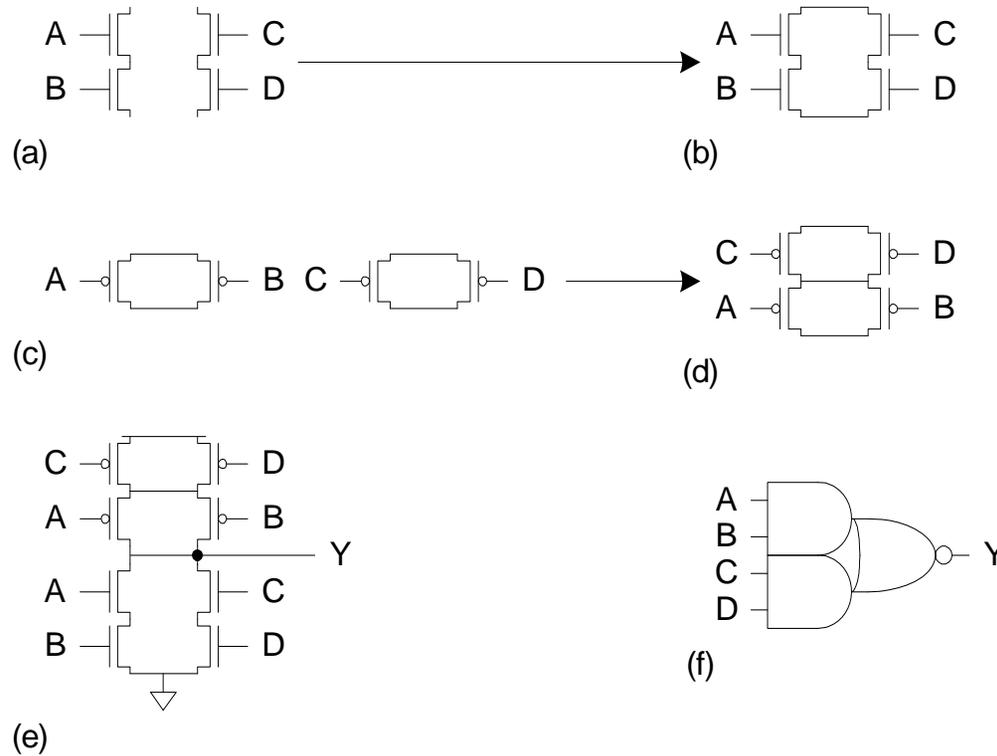
Compound Gates ...
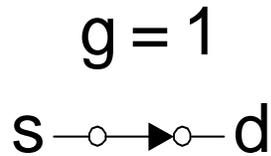
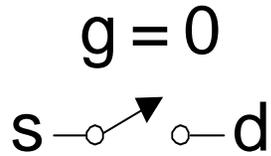Example: $Y = \overline{(A + B + C) \cdot D}$
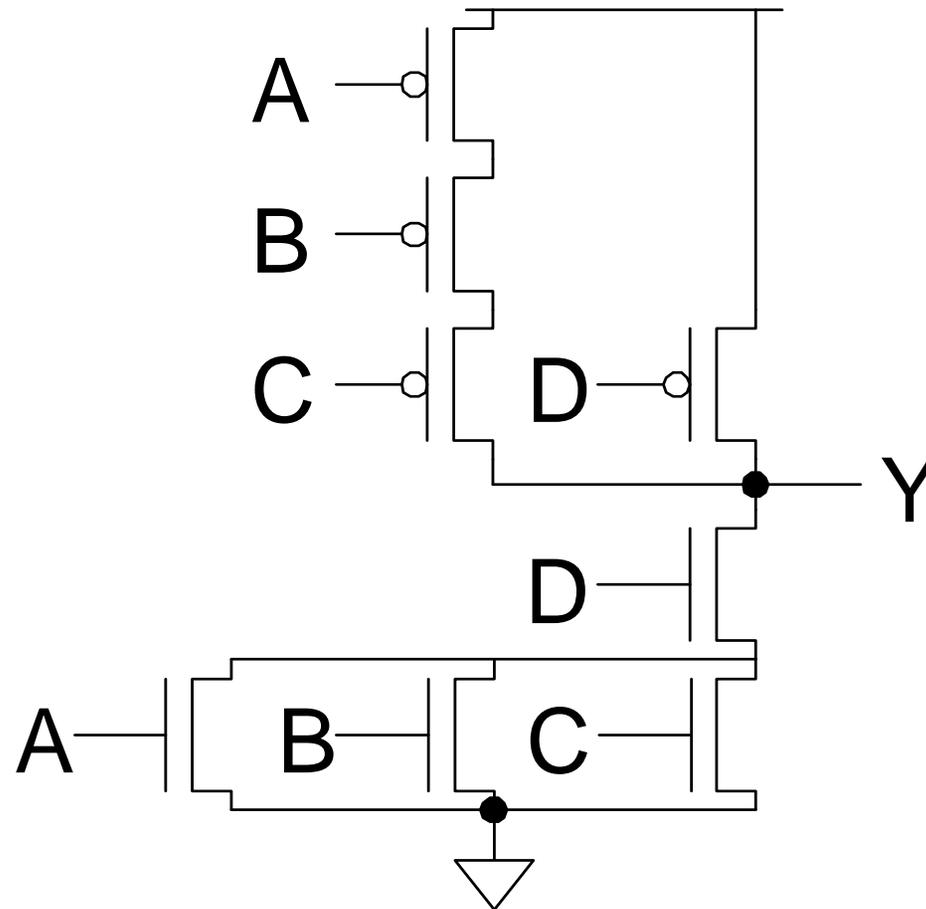
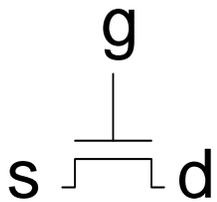Solve Example 6.2, page-240, Rabaey book.
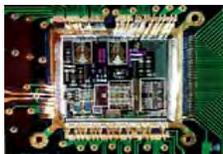
Pass Transistors

- Transistors can be used as switches.

g

s ⊣⊢ d

g = 0

s —○↗○— d

g = 1

s —○▶○— d

Input   g = 1   Output

0 —○▶○— strong 0

g = 1

1 —○▶○— degraded 1

g

s ⊣⊢ d

g = 0

s —○▶○— d

g = 1

s —○↗○— d

Input   g = 0   Output

0 —○▶○— degraded 0

g = 0

—○▶○— strong 1
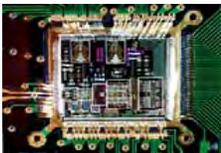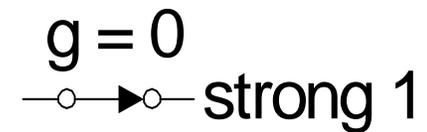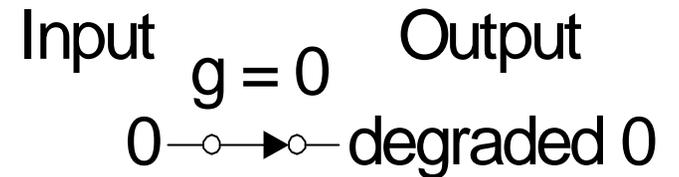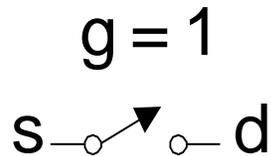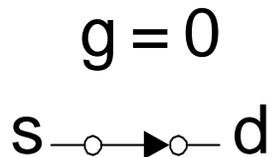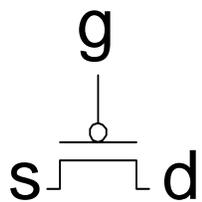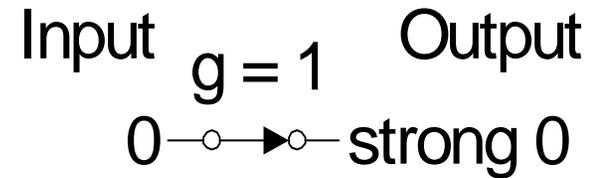
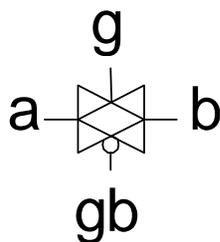# Transmission Gates

- Pass transistors produce degraded outputs.
- *Transmission gates* pass both 0 and 1 well.

Input   Output

g = 0, gb = 1

a — b

g = 1, gb = 0

a → b

g = 1, gb = 0

0 ⟶ strong 0

g = 1, gb = 0
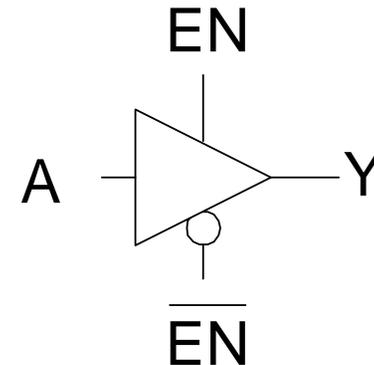
1 ⟶ strong 1

g

a ⊏⊐ b

gb

g

a ⧓ b

gb

g

a ⊗ b

gb

g

a ⊳ b

gb
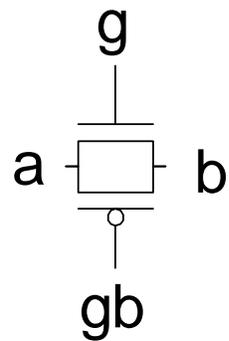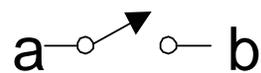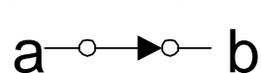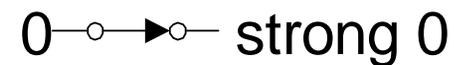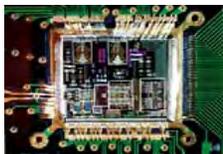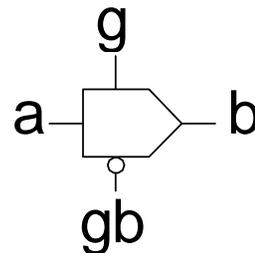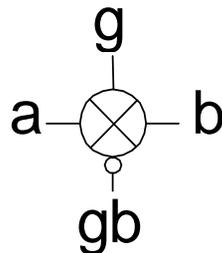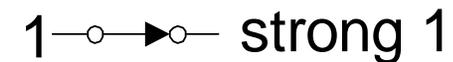
Tristate Buffer

- *Tristate buffer* produces Z when not enabled.

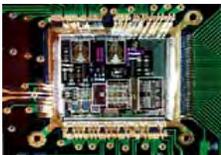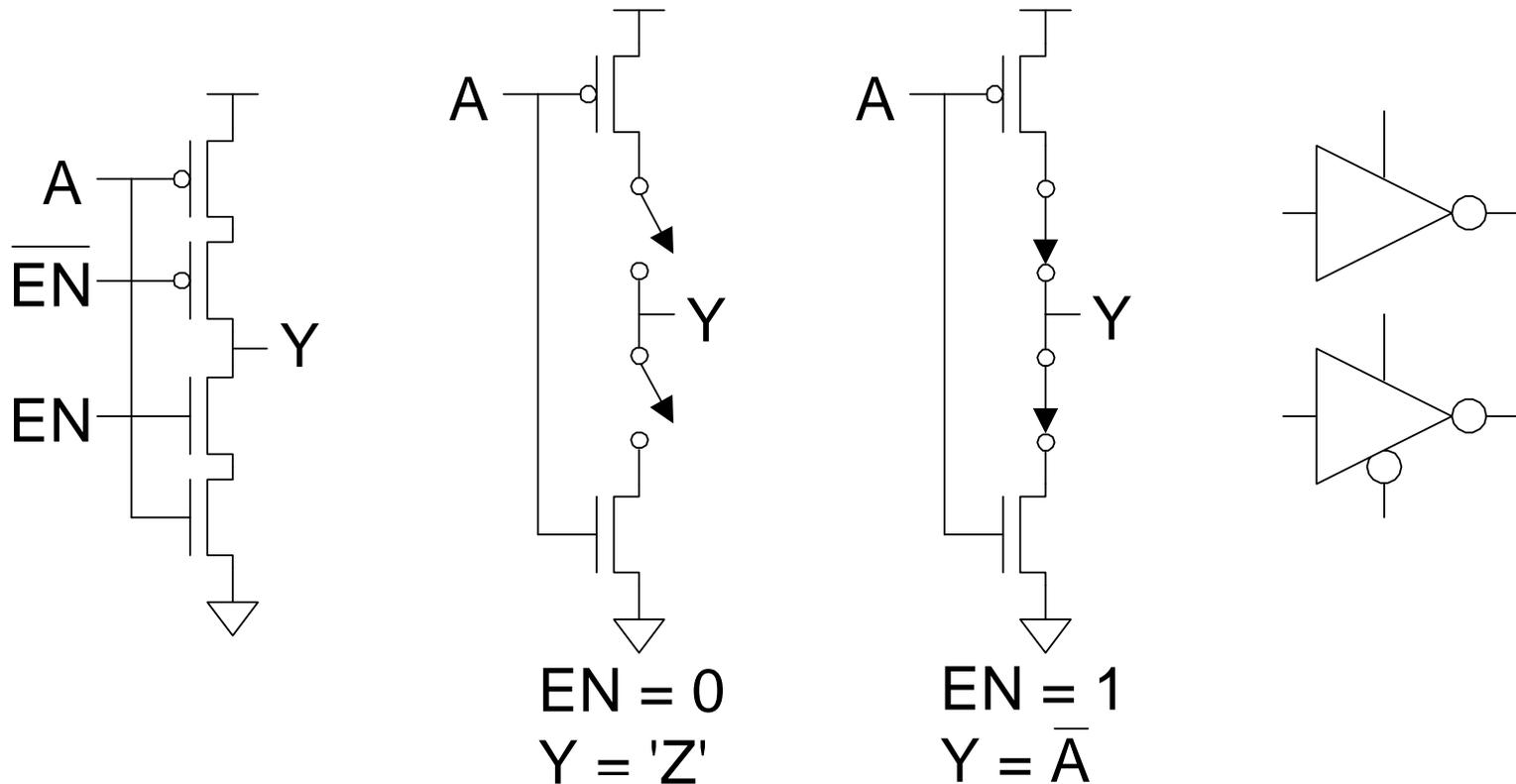| EN	A	Y
0	0	Z
0	1	Z
1	0	0
1	1	1
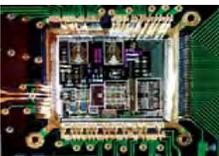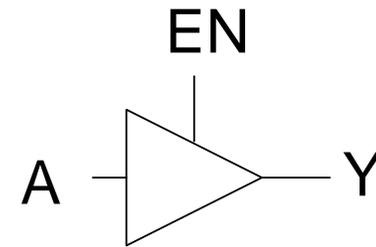
Nonrestoring Tristate Buffer

- ## Transmission gate acts as tristate buffer.
  - Only two transistors
  - But *nonrestoring*
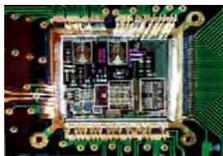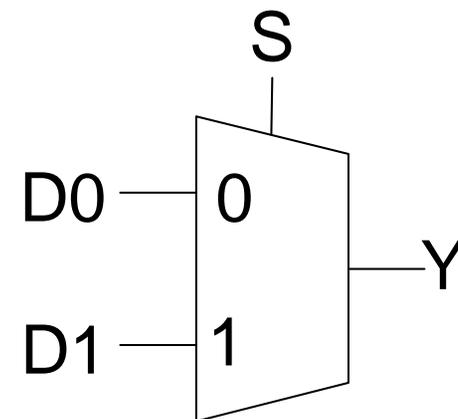   - Noise on A is passed on to Y
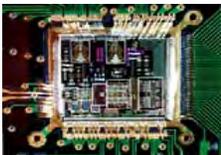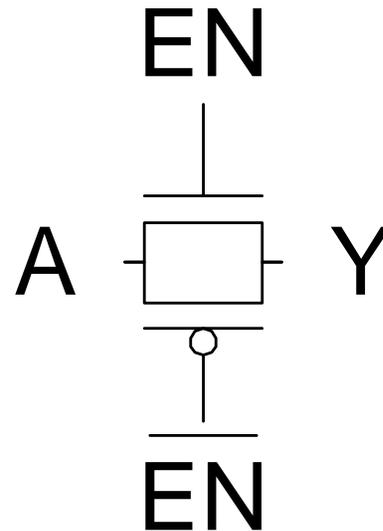
Tristate Inverter

- Tristate inverter produces restored output.
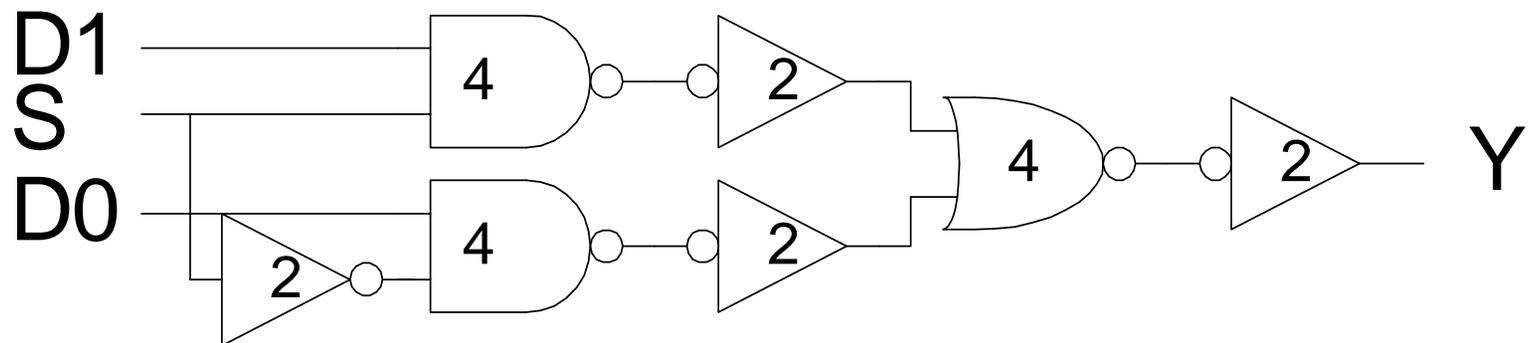 - Violates conduction complement rule
  - Because we want a Z output

A

$\overline{EN}$

EN

Y

A
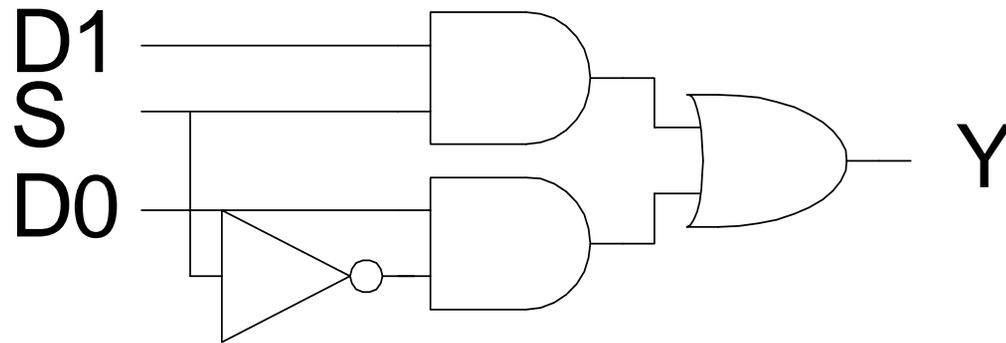
Y

EN = 0
Y = 'Z'

A

Y

EN = 1
Y = $\overline{A}$

Multiplexers

- 2:1 multiplexer chooses between two inputs.

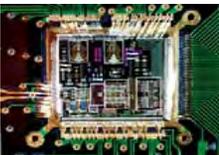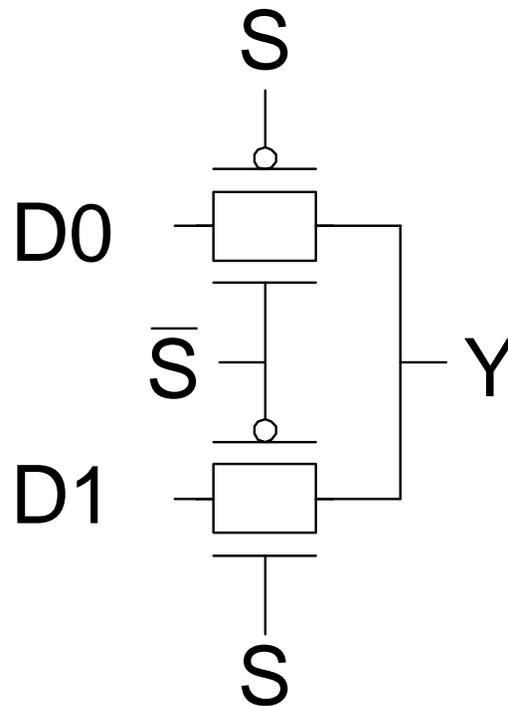| S	D1	D0	Y
0	X	0	0
0	X	1	1
1	0	X	0
1	1	X	1

Multiplexers Design : One Approach

- $Y = SD_1 + \overline{S}D_0$ (too many transistors)
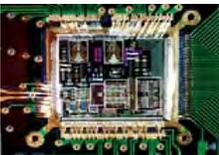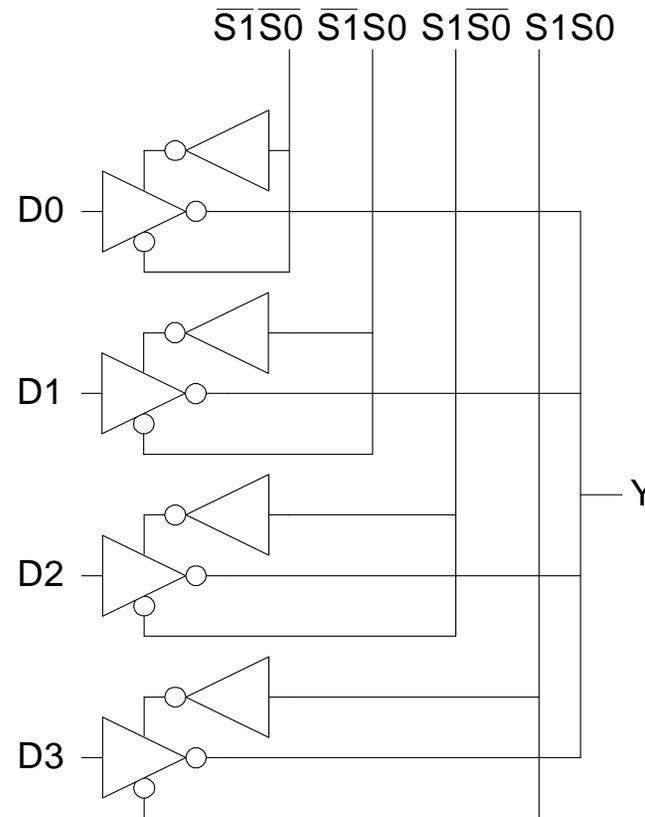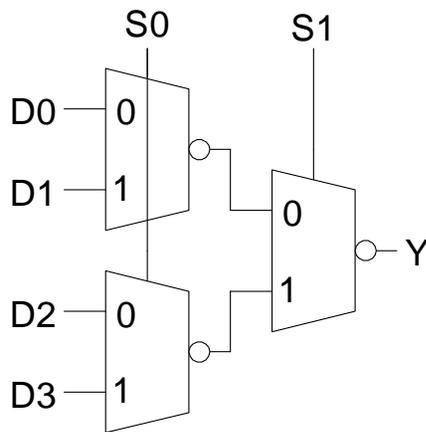- How many transistors are needed? 20

Multiplexers Design : 2nd Approach

- Nonrestoring mux uses two transmission gates.
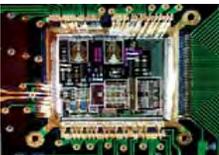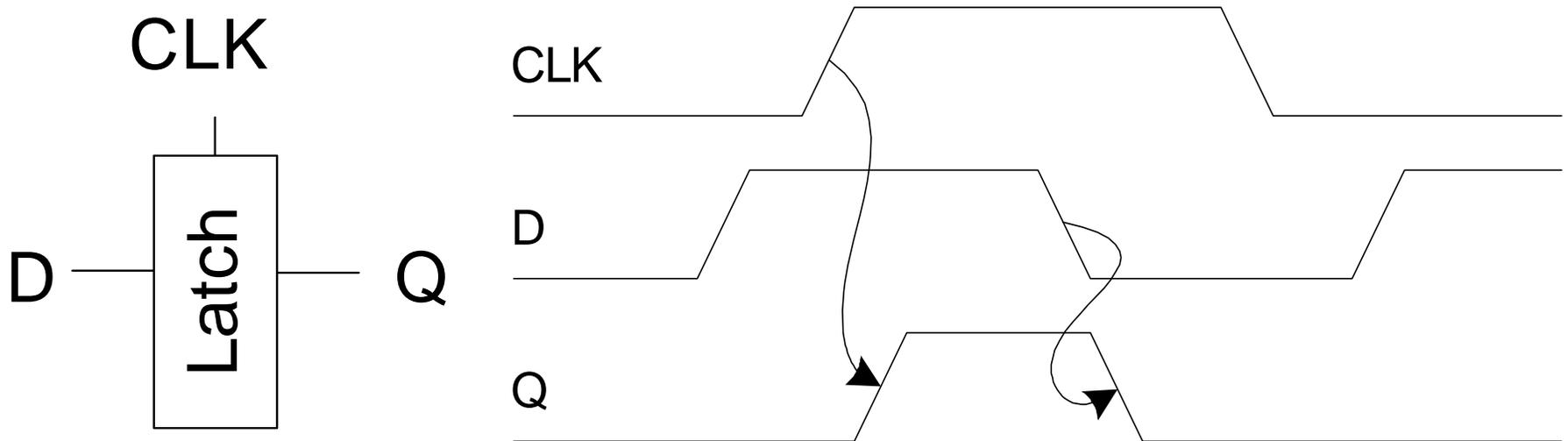 - Only 4 transistors

4:1 Multiplexer

- 4:1 mux chooses one of 4 inputs using two selects.
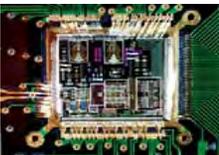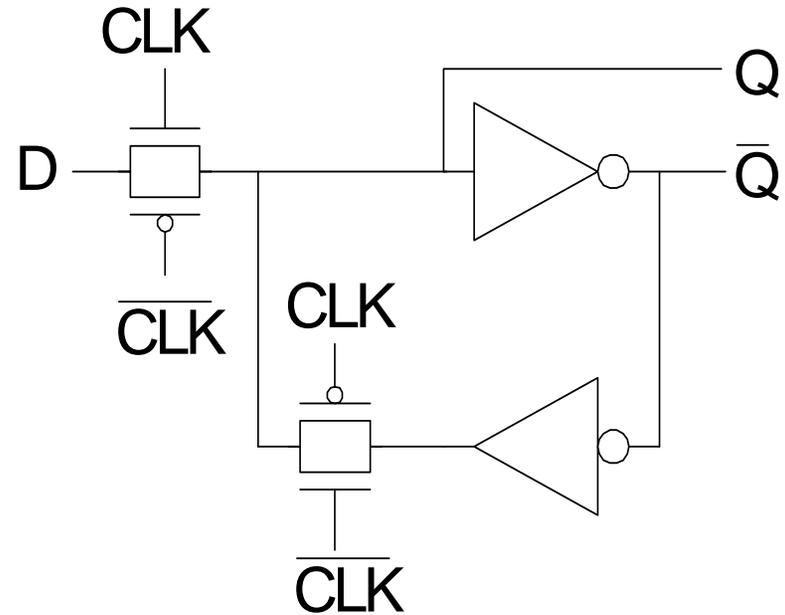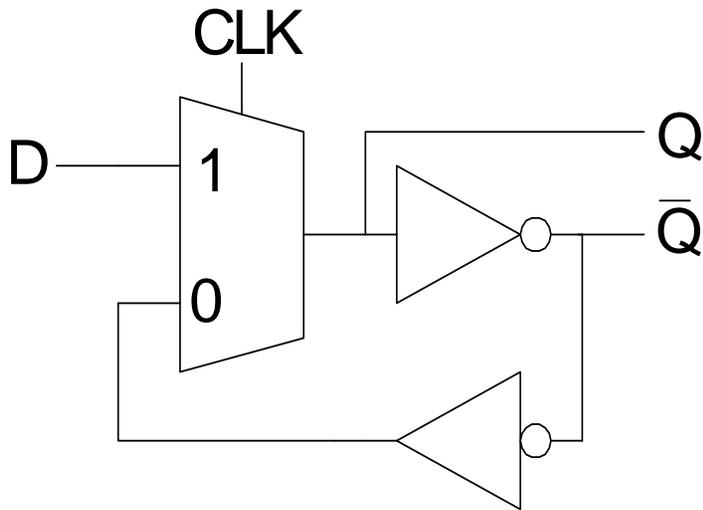 - Two levels of 2:1 muxes
  - Or four tristates

D Latch

- When CLK = 1, latch is *transparent*
  - D flows through to Q like a buffer
- When CLK = 0, the latch is *opaque*
  - Q holds its old value independent of D
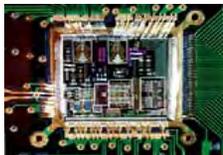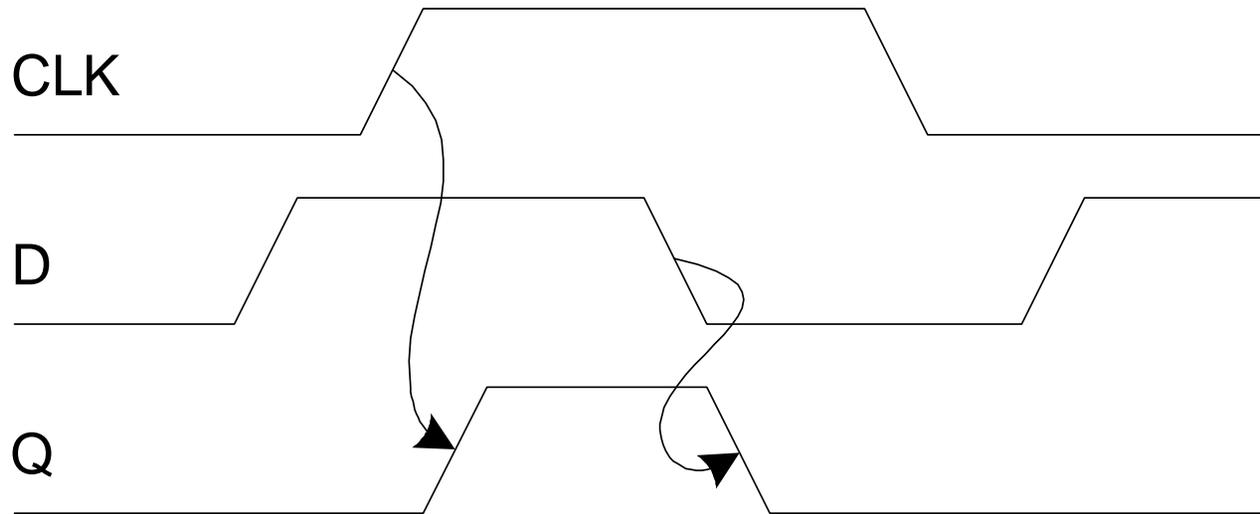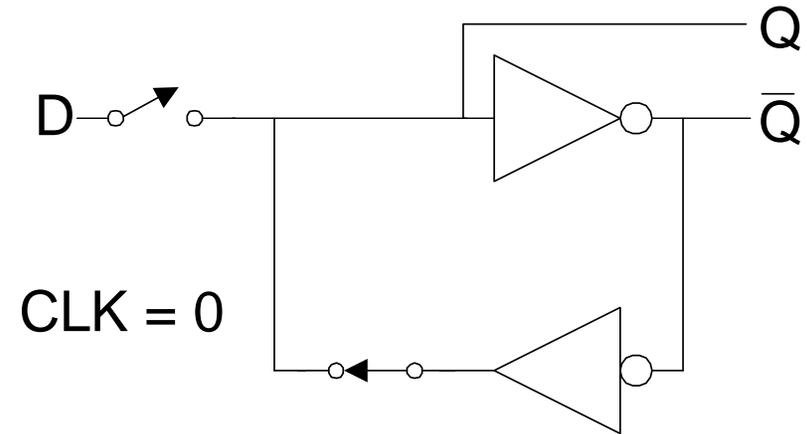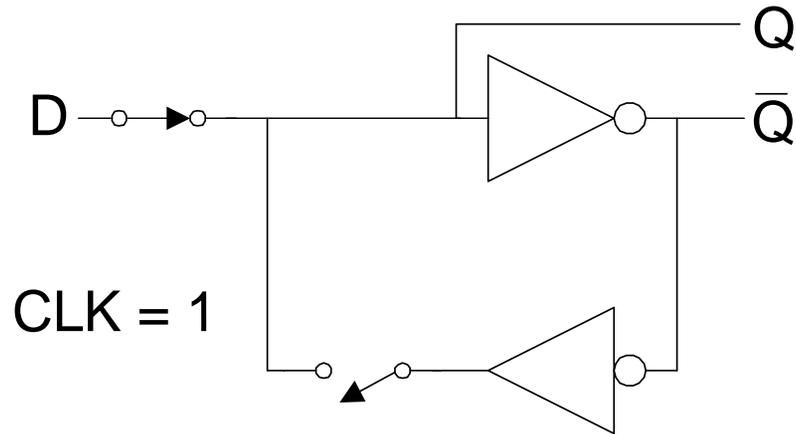- *a.k.a. transparent latch* or *level-sensitive latch.*

D Latch : Design

- Multiplexer chooses D or old Q.

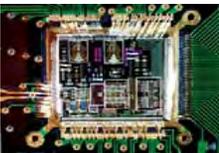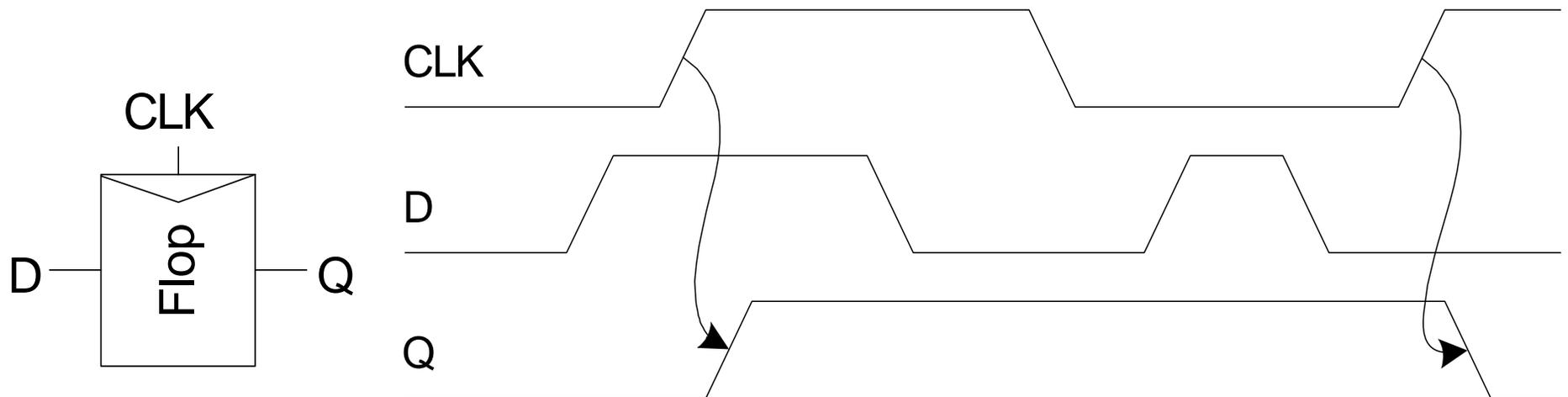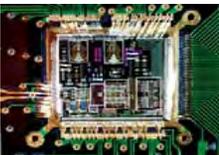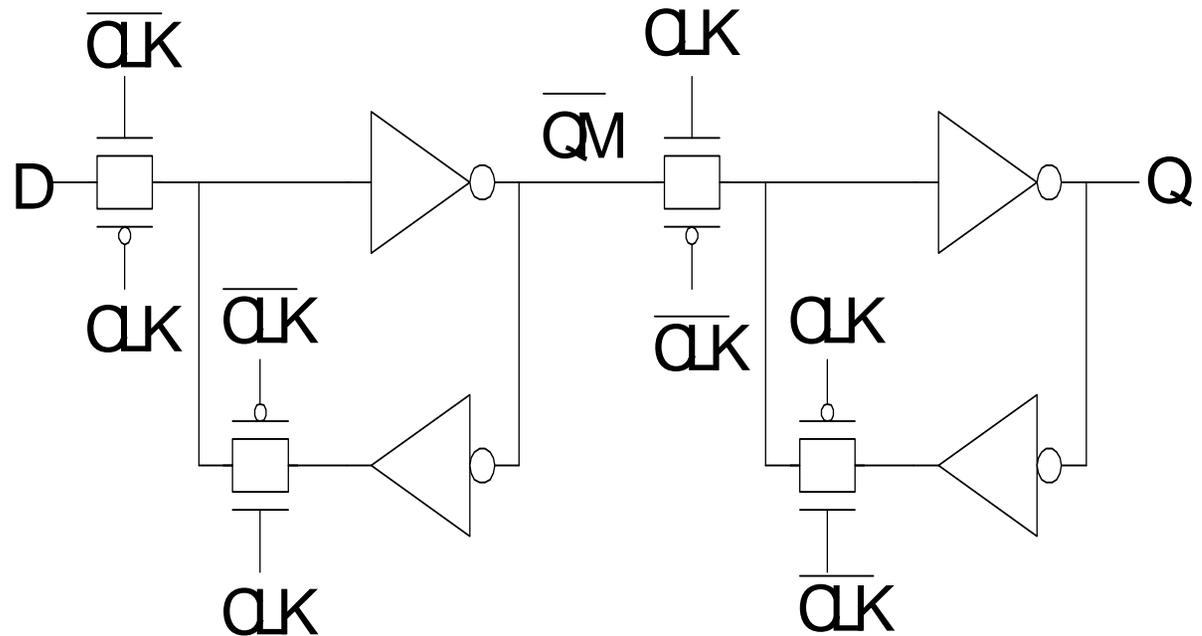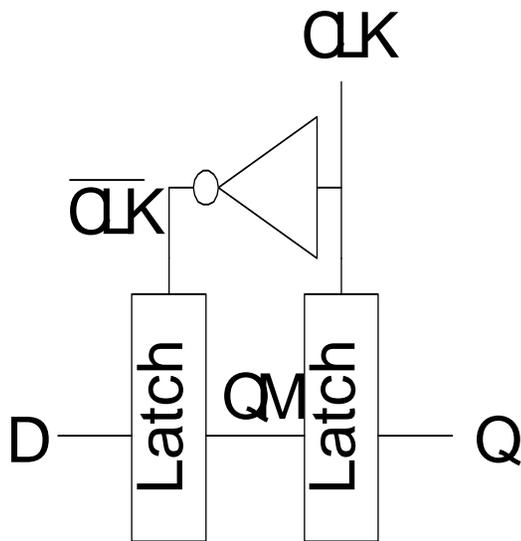# D Latch : Operation

CLK = 1

CLK = 0

D Flip-flop

- When CLK rises, D is copied to Q.
- At all other times, Q holds its value.
- a.k.a. *positive edge-triggered flip-flop, master-slave flip-flop.*
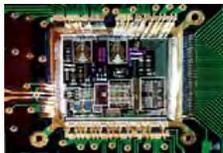
D Flip-flop : Design

- Built from master and slave D latches.

D Flip-flop : Operation

D-FF : Race Condition

- Back-to-back flops can malfunction from clock skew.
  - Second flip-flop fires late
  - Sees first flip-flop change and captures its result
  - Called *hold-time failure* or *race condition*
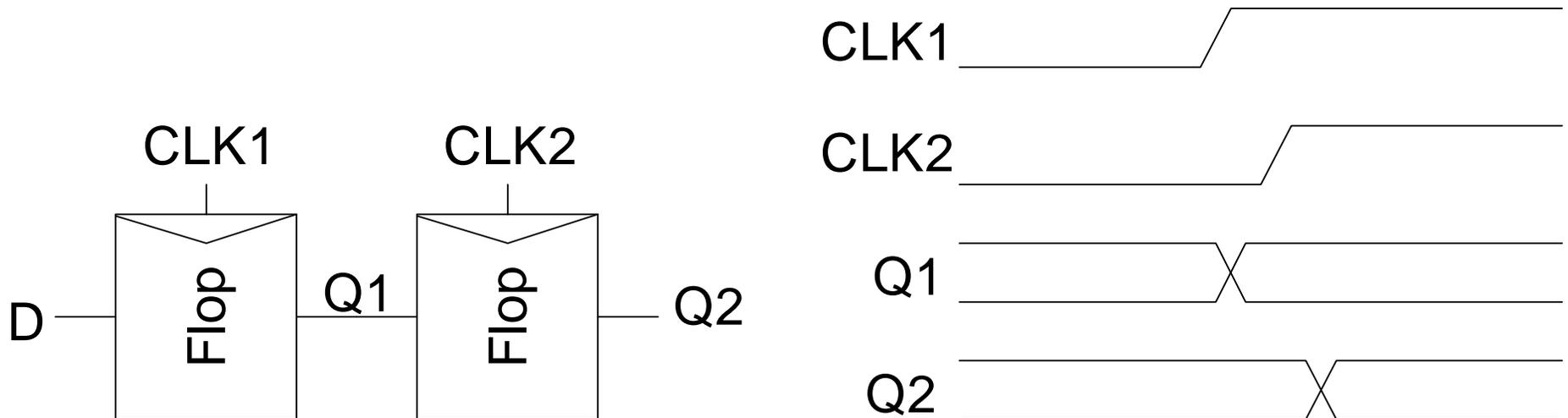
D-FF: Nonoverlapping Clocks

- Nonoverlapping clocks can prevent races.
  - As long as nonoverlap exceeds clock skew
- We will use them in this class for safe design.
  - Industry manages skew more carefully instead

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