CSCE 5730/4730: Digital CMOS VLSI Design

Assignment # 5, Total Points = 4*25 = 100.
Assigned Date: 10th Nov 2010 (Wed), Due Date: 17th Nov 2010 (Wed)
Instructor: Dr. Saraju P. Mohanty

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1. Explain mobility degradation in short channel transistors.
2. Why gate leakage occurs in nanoscale transistors? What device parameters affect it?
3. What are the effects of temperature on transistor performance?
4. Discuss origin and impact of process variation in nanoscale transistors.