

# Lecture 2: LTspice

## Digital CMOS VLSI Design

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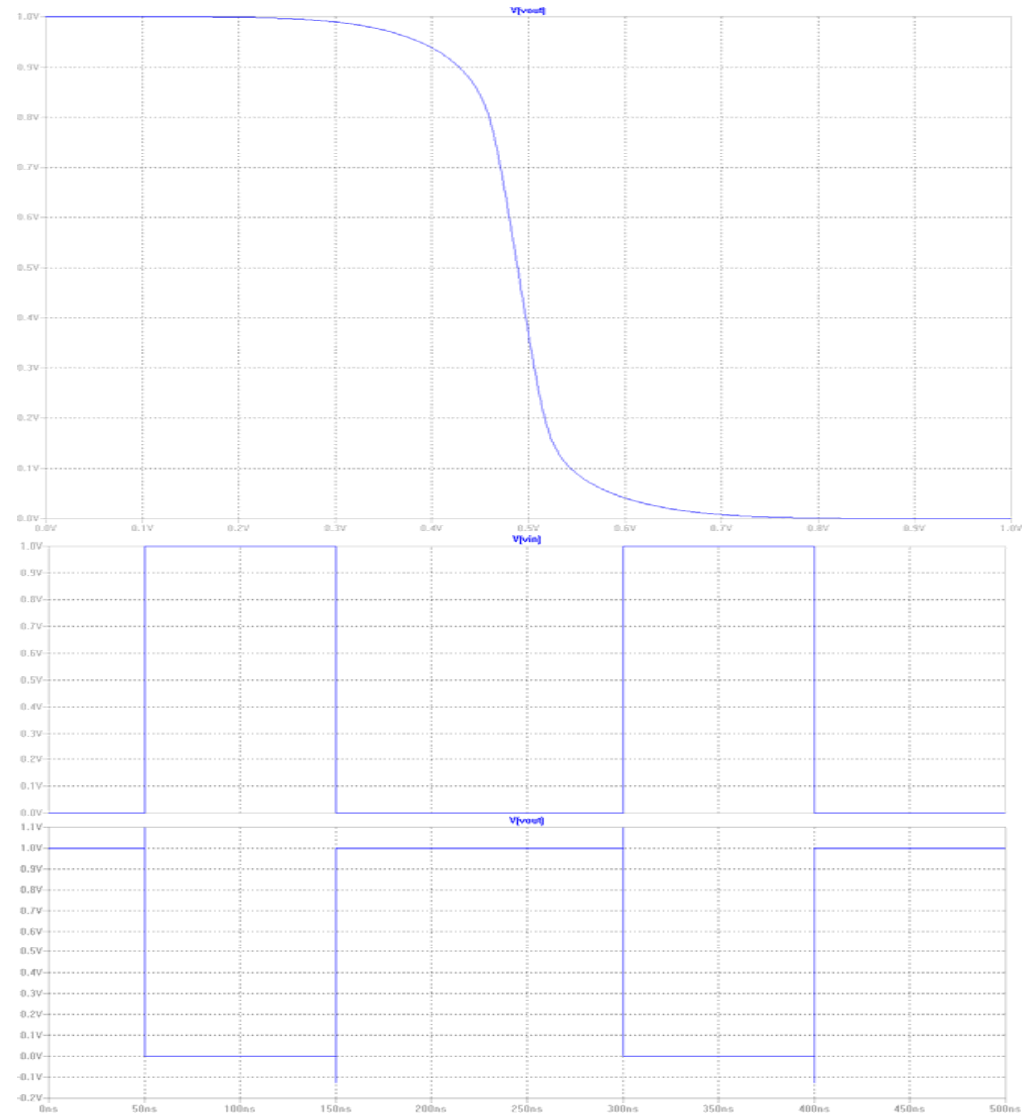
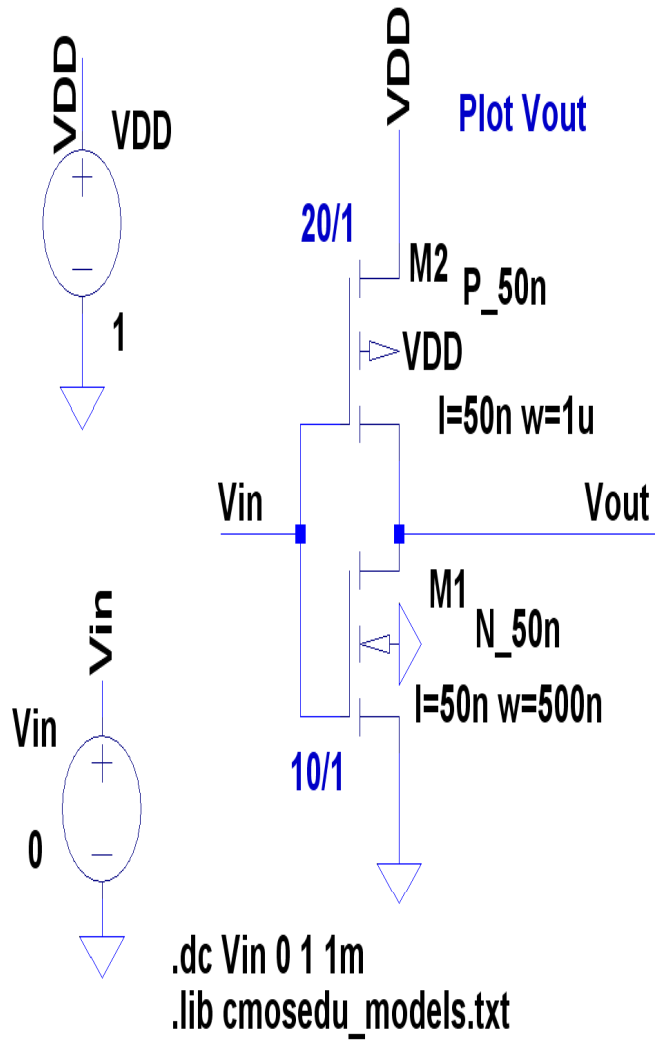


# USEFUL LINKS

- LTPSICE software available at:  
[http://www.linear.com/designtools/software/switc  
hercad.jsp](http://www.linear.com/designtools/software/switc<br/>hercad.jsp)
- 50nm model file available at:  
<http://www.cmosedu.com/cmos1/book.htm>
- More model files available at:  
<http://www.eas.asu.edu/~ptm/>



# CMOS Inverter



# Construct an Inverter using LTSPICE

- Discussion at Nano-CMOS: 50nm technology.
- PMOS: 20/1 ( $L = 50\text{nm}$ /  $W = 1\mu\text{m}$ )
- NMOS: 10/1 ( $L = 50\text{nm}$ /  $W = 500\text{nm}$ )
- $V_{DD}$ : Supply voltage ( $V_{dc} = 1\text{V}$ ).
- $V_{in}$ : changes depending upon analysis:
- DC analysis: DC voltage (1V).
- Transient analysis: Pulsed voltage (vpulse).
- Wire to connect components.
- Model file (cmosedu\_models.txt).



# What does a model file look like ?

```

*** Short channel models from CMOS Circuit Design, Layout, and Simulation, 2e
* 50nm BSIM4 models Udd=1U
.model N_50n nmos level = 14
+binunit = 1 paramchk= 1 mobmod = 0
+capmod = 2 igcm0d = 1 rgbmod = 1 geomod = 1
+diomod = 1 rdsmod = 0 rbodymod= 1 rgatemod= 1
+permod = 1 acnqsm0d= 0 trnqsm0d= 0

+tnom = 27 tox0 = 1.4e-009 toxp = 7e-010 toxm = 1.4e-009
+epsrox = 3.9 wint = 5e-009 lint = 1.2e-008 | wln = 1
+l1 = 0 w1 = 0 l1n = 1 wwn = 1
+lw = 0 ww = 0 lwn = 1 toxref = 1.4e-009
+lw1 = 0 ww1 = 0 xpart = 0

+uth0 = 0.22 k1 = 0.35 k2 = 0.05 k3 = 0
+k3b = 0 w0 = 2.5e-006 dvt0 = 2.8 dvt1 = 0 dvt2 = 0.52
+dvt2 = -0.032 dvt0w = 0 dvt1w = 0 dvt2w = 0
+ds0b = 2 minv = 0.05 voff1 = 0 dvtp0 = 1e-007
+dvtp1 = 0.05 lpe0 = 5.75e-008 lpeb = 2.3e-010 xj = 2e-008
+ngate = 5e+020 ndep = 2.8e+018 nsd = 1e+020 phin = 0
+cdsc = 0.0002 cdscb = 0 cdscd = 0 cit = 0
+voff = -0.15 nfactor = 1.2 eta0 = 0.15 etab = 0
+ufb = -0.55 u0 = 0.032 ua = 1.6e-010 ub = 1.1e-017
+uc = -3e-011 usat = 1.1e+005 a0 = 2 ags = 1e-020
+a1 = 0 a2 = 1 b0 = -1e-020 b1 = 0
+keta = 0.04 dwg = 0 dwb = 0 pclm = 0.18
+pdiblc1 = 0.028 pdiblc2 = 0.022 pdiblc3 = -0.005 drout = 0.45
+pvag = 1e-020 delta = 0.01 pscbe1 = 8.14e+008 pscbe2 = 1e-007
+fprout = 0.2 pdits = 0.2 pditsd = 0.23 rdw = 150 pdits1 = 2.3e+006
+rsh = 3 rdsw = 150 rsw = 150 prw = 0
+rdswmin = 0 rdwmin = 0 rswmin = 0 alpha0 = 0.074 alpha1 = 0.005
+prwb = 6.8e-011 wr = 1 bgidl = 2.1e+009 cgidl = 0.0002
+beta0 = 30 agidl = 0.0002

+aigbacc = 0.012 bigbacc = 0.0028 cigbacc = 0.002 cigbinv = 0.004
+nigbacc = 1 aigbinv = 0.014 bigbinv = 0.004 bigc = 0.0028
+eigbinv = 1.1 nigbinv = 3 aigc = 0.017 bigsd = 0.002 cigsd = 0.002
+cigc = 0.002 aigsd = 0.017 pigcd = 1 ntox = 1
+nigc = 1 poxedge = 1

+xrcrg1 = 12 xrcrg2 = 5 cgbo = 2.56e-011 cgdl = 2.495e-10
+cgso = 6.238e-010 cgdo = 6.238e-010 ckappad = 0.02 acde = 1
+cgsl = 2.495e-10 ckappas = 0.02 noff = 0.9 voffcv = 0.02

+kt1 = -0.21 kt11 = 0.0 kt2 = -0.042 ute = -1.5
+ua1 = 1e-009 ub1 = -3.5e-019 uc1 = 0 prt = 0
+at = 53000

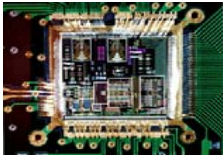
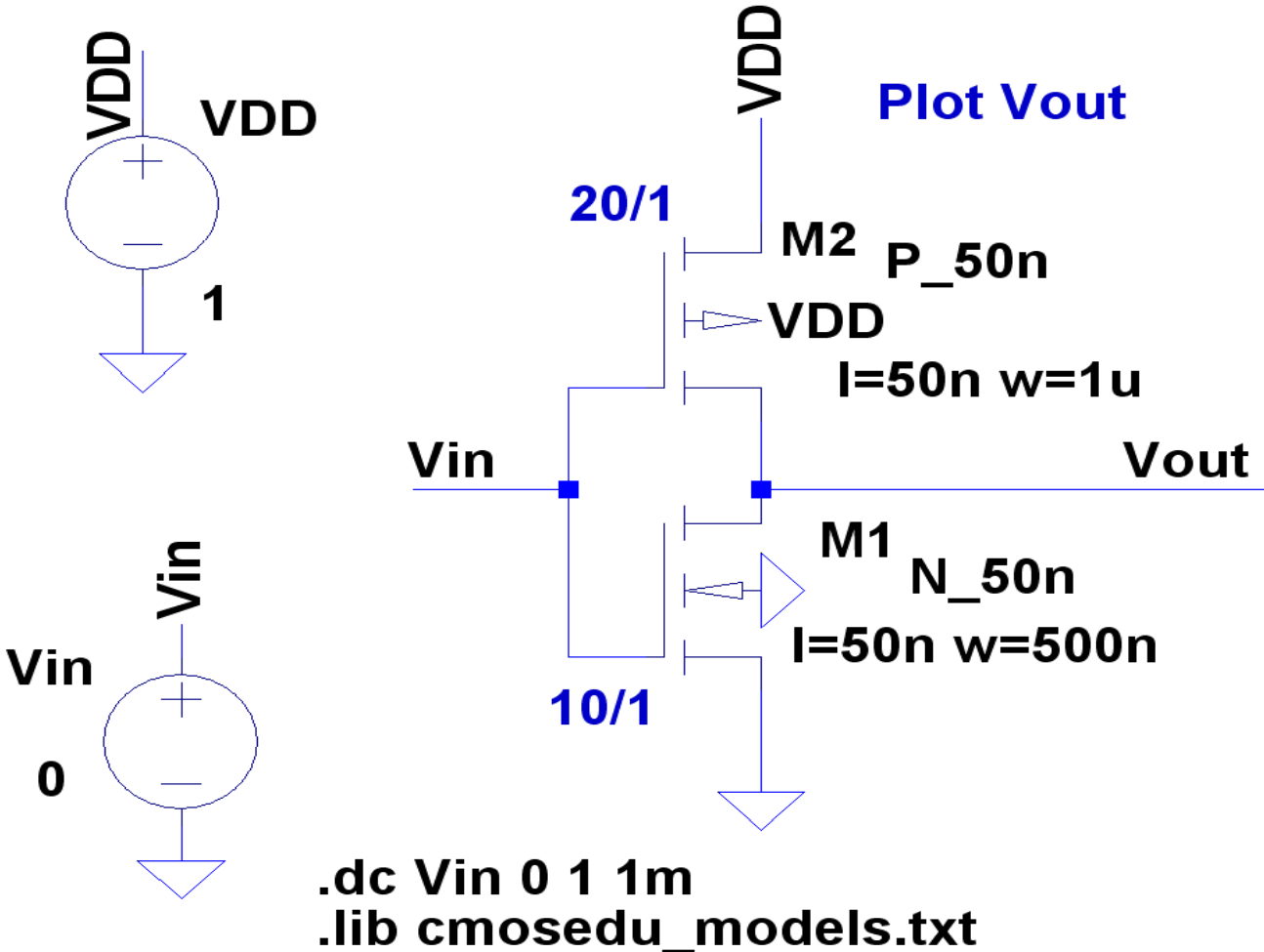
+fnoimod = 1 tnoimod = 0

+jss = 0.0001 jsws = 1e-011 jswgs = 1e-010 njs = 1
+ijthsfwd = 0.01 ijthsrev = 0.001 bus = 10 xjbus = 1
+icd = 0.0001 icud = 1e-011 ismod = 1e-010 nid = 1

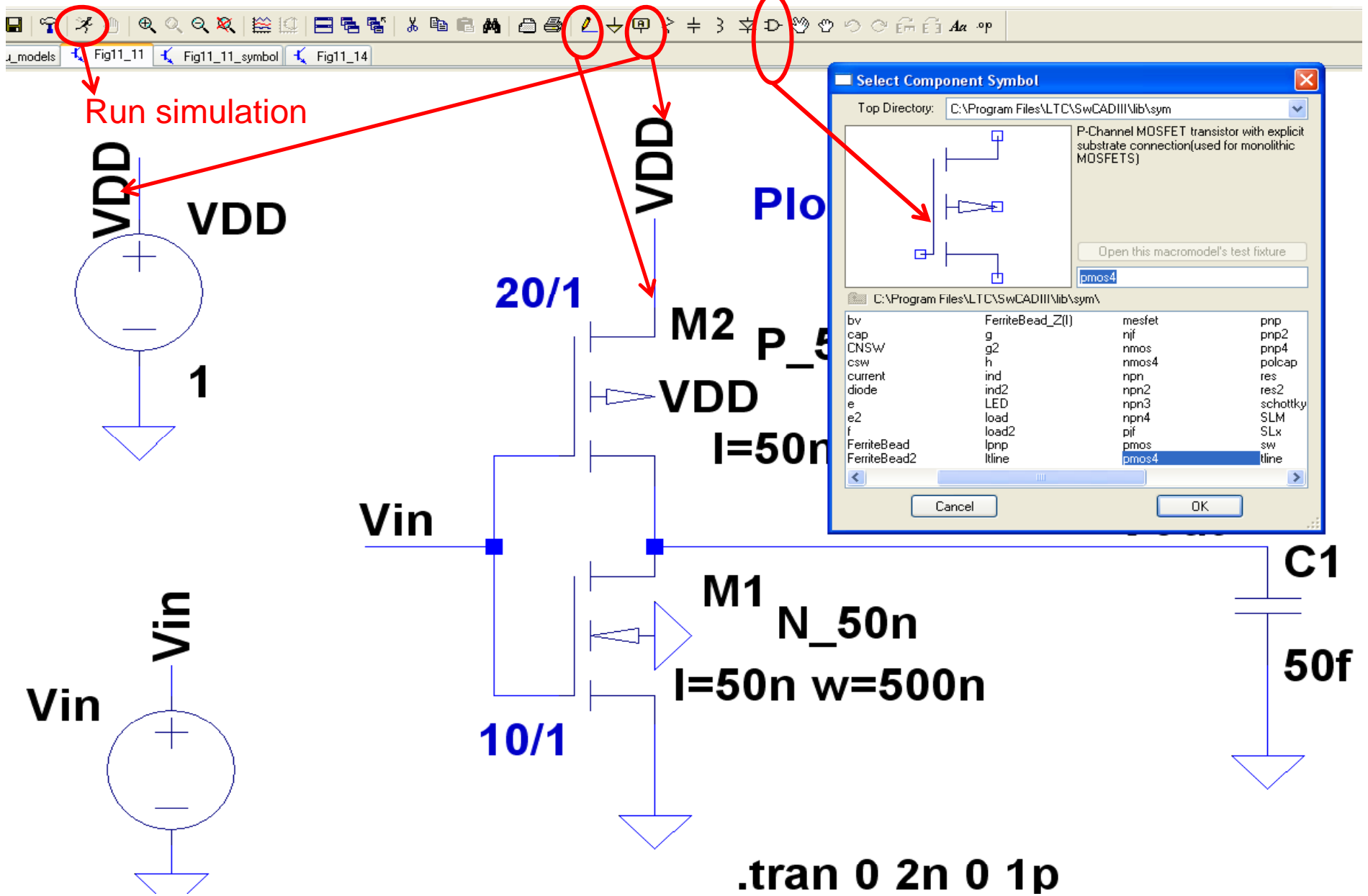
```



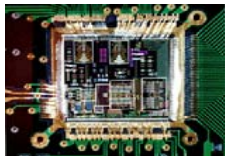
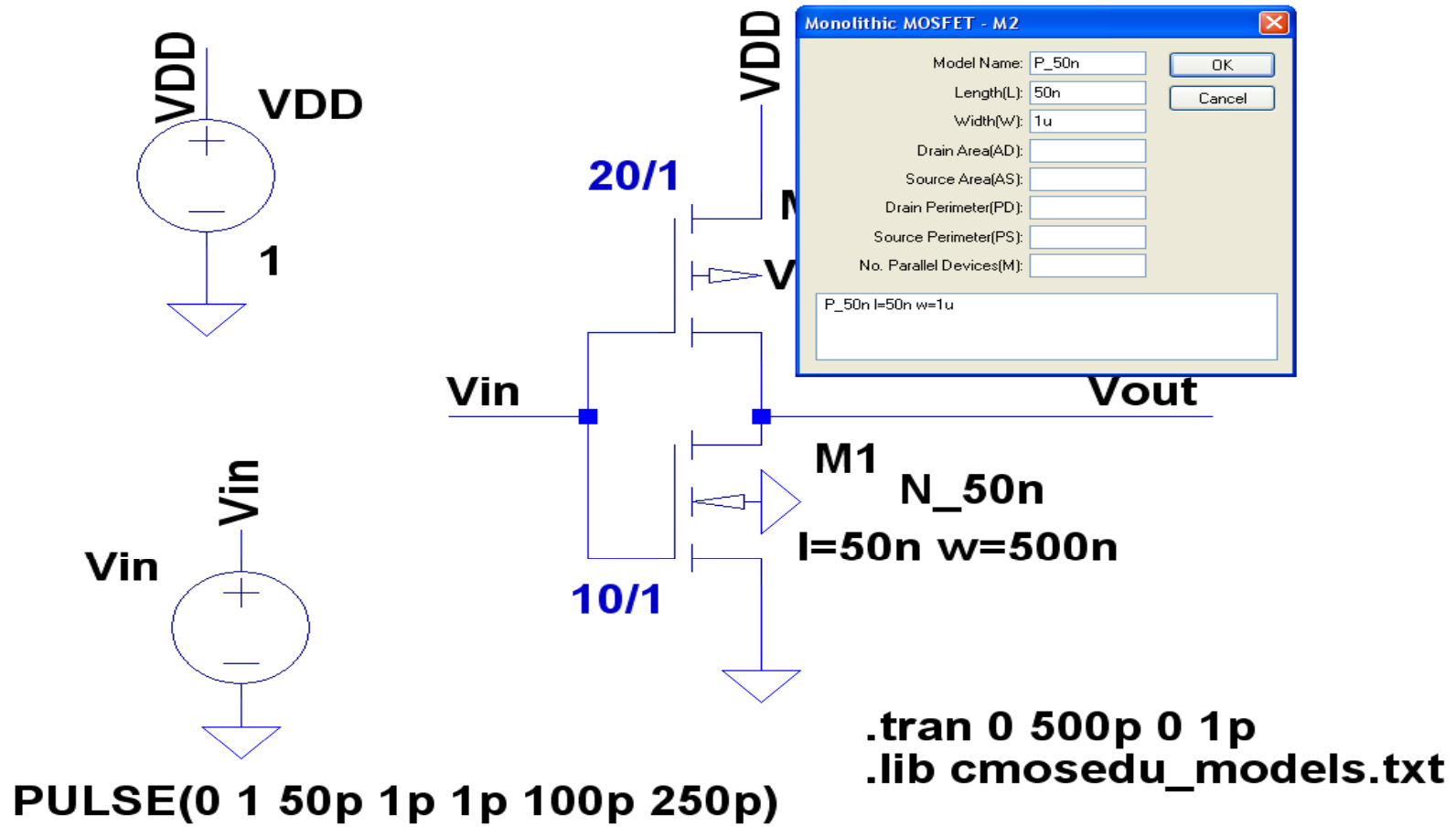
# Placing and connecting components



# Where to get components from ?

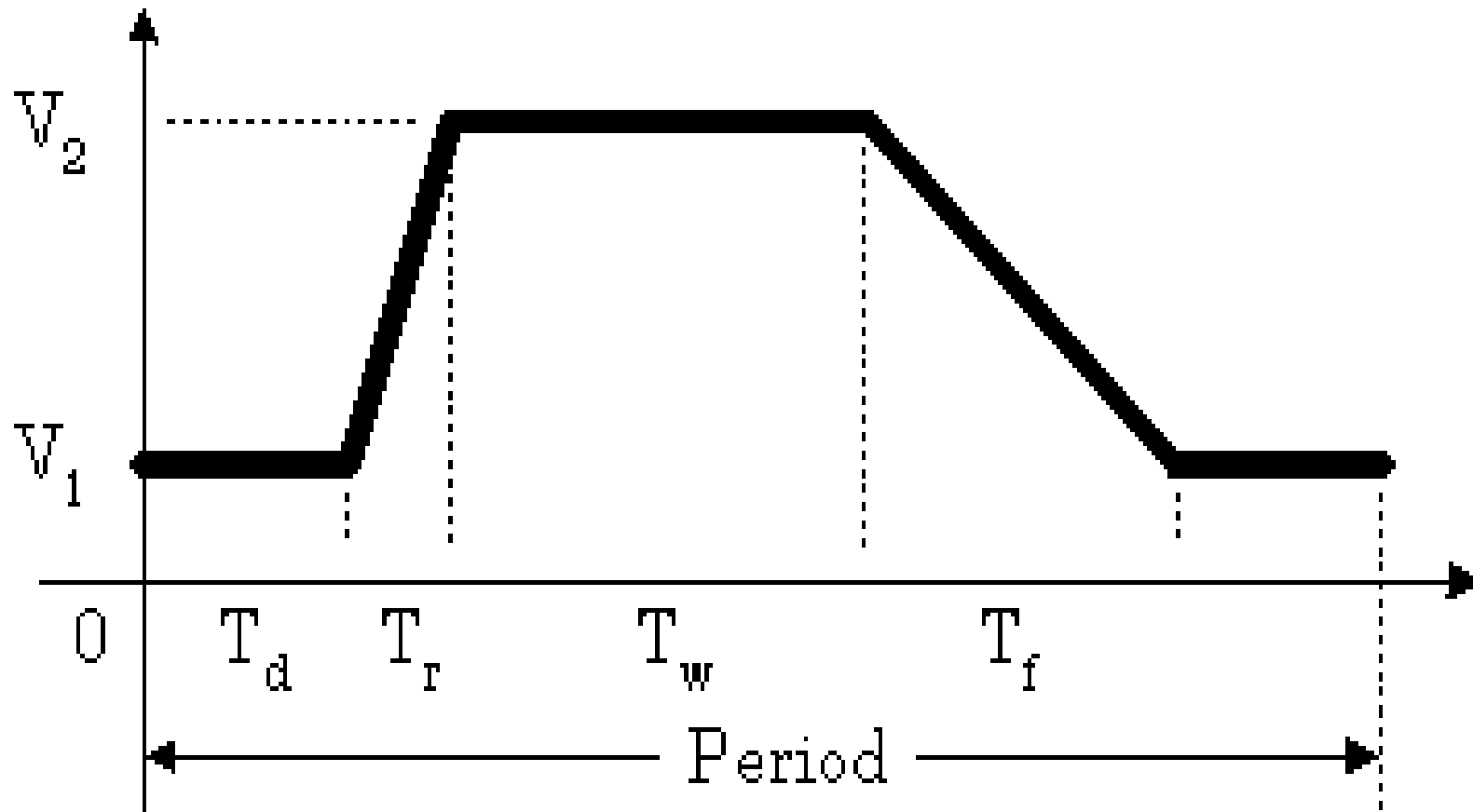


# How to assign W/L ?





# Interpreting a pulsed waveform



# How to assign Vin ?

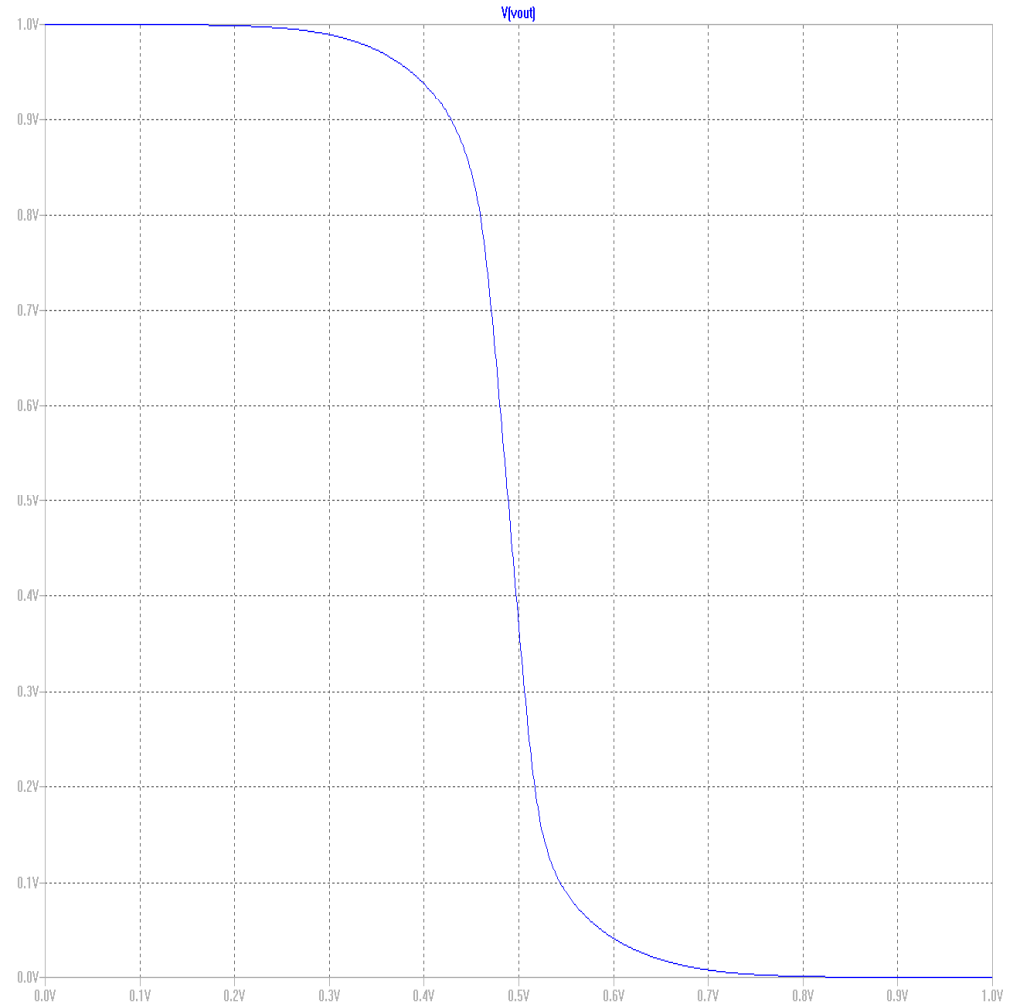
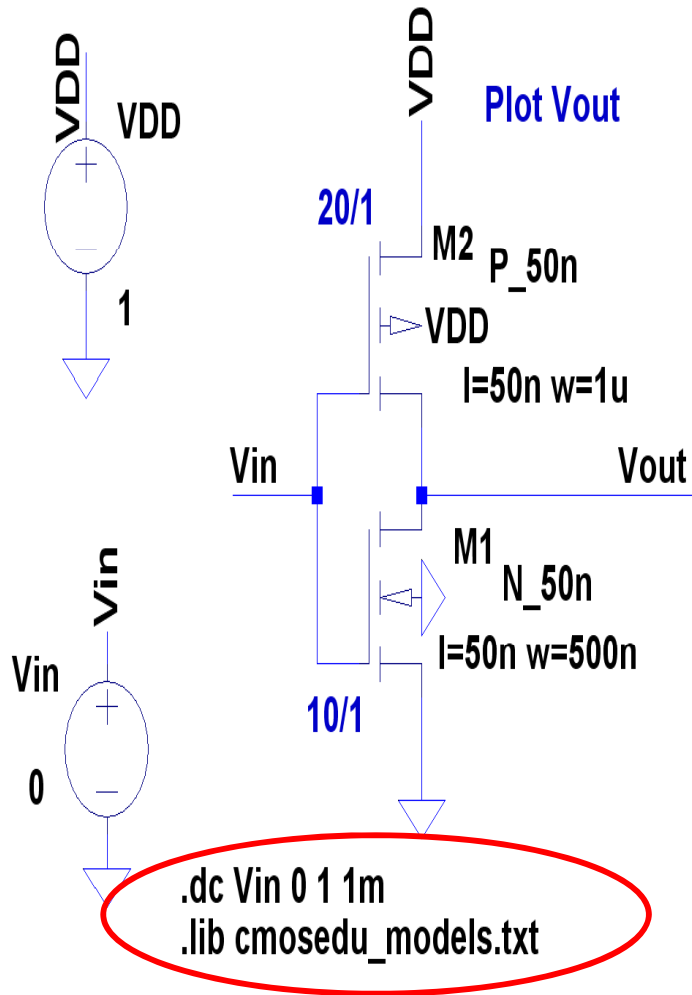
The image shows two circuit diagrams and a dialog box. The top diagram shows a voltage source labeled 'VDD' connected to a node labeled 'VD'. The bottom diagram shows a voltage source labeled 'Vin' connected to a node labeled 't'. The dialog box, titled 'Independent Voltage Source - Vin', is open and shows the 'PULSE' function selected. The parameters for the pulse are: Vinitial[V]: 0, Von[V]: 1, Tdelay[s]: 50p, Trise[s]: 1p, Tfall[s]: 1p, Ton[s]: 100p, Tperiod[s]: 250p, and Ncycles: (empty). The 'Make this information visible on schematic' checkbox is checked. The dialog also has sections for 'DC Value', 'Small signal AC analysis(.AC)', and 'Parasitic Properties', all with their respective checkboxes checked.

**PULSE(0 1 50p 1p 1p 100p 250p)**

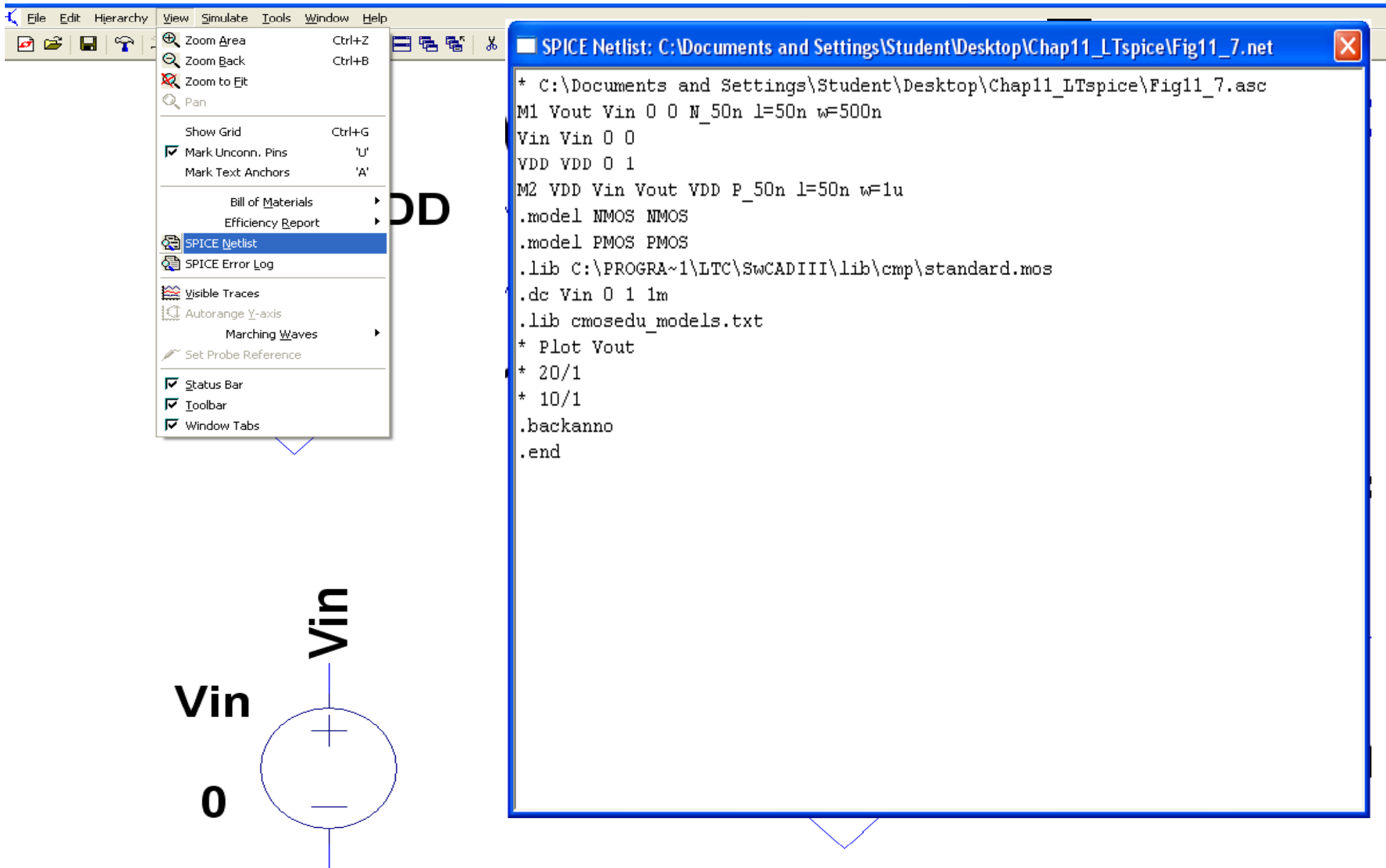
**.tran 0 500p 0 1p  
.lib cmosedu\_models.txt**



# DC Analysis



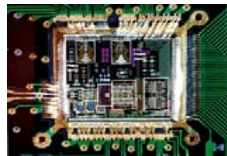
# View netlist



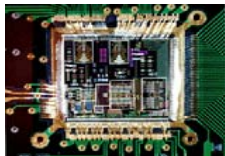
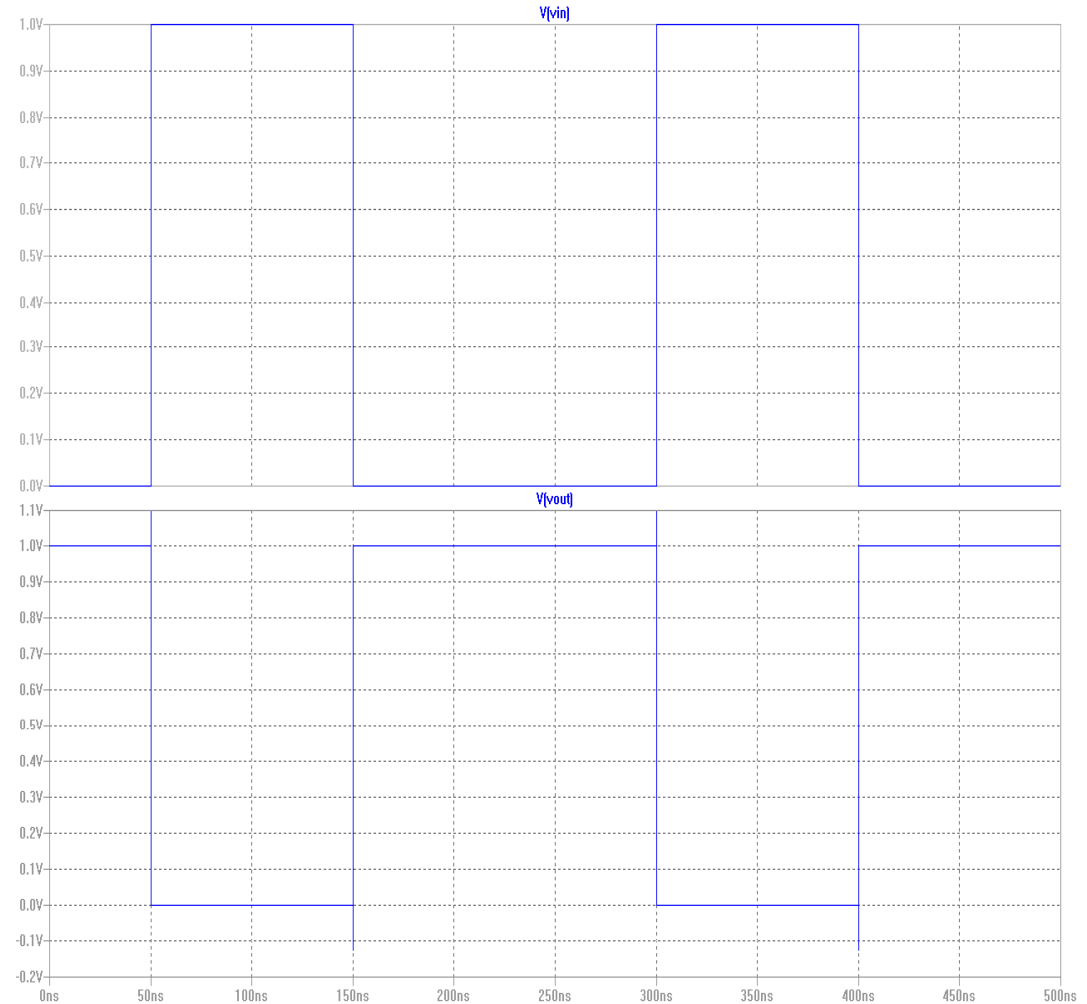
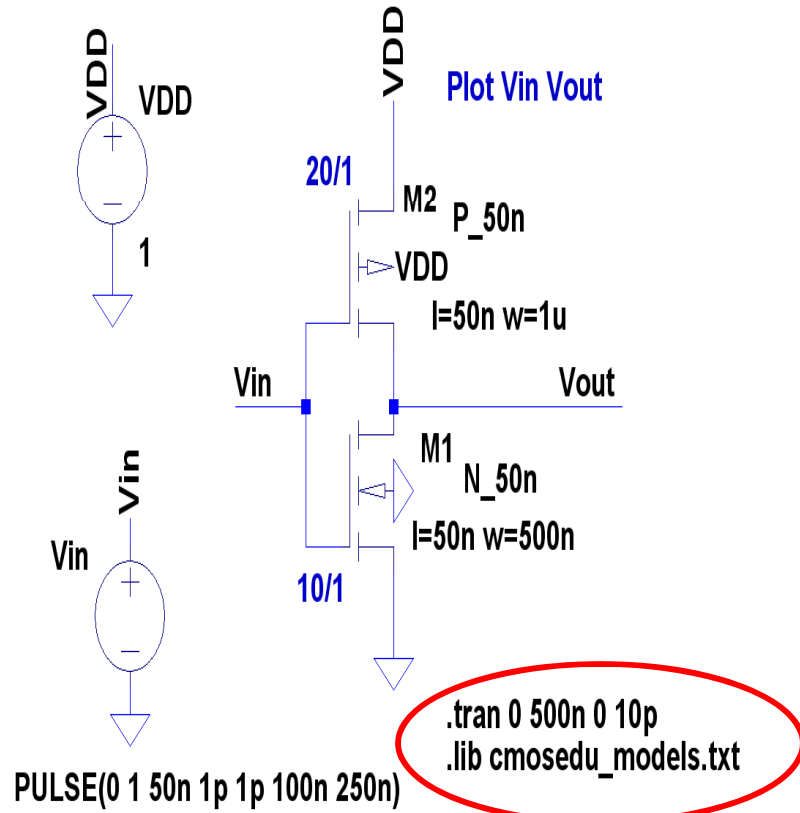
The screenshot shows a SPICE Netlist viewer window with the following content:

```
* C:\Documents and Settings\Student\Desktop\Chap11_LTspice\Fig11_7.asc
M1 Vout Vin 0 0 N_50n l=50n w=500n
Vin Vin 0 0
VDD VDD 0 1
M2 VDD Vin Vout VDD P_50n l=50n w=1u
.model NMOS NMOS
.model PMOS PMOS
.lib C:\PROGRA~1\LTC\SwCADIII\lib\cmp\standard.mos
.dc Vin 0 1 1m
.lib cmosedu_models.txt
* Plot Vout
* 20/1
* 10/1
.backanno
.end
```

Below the netlist, a schematic diagram of a voltage source is shown. It consists of a circle with a plus sign at the top and a minus sign at the bottom. The top terminal is labeled "Vin" and the bottom terminal is labeled "0".

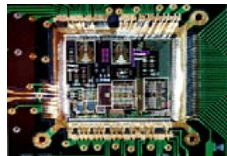
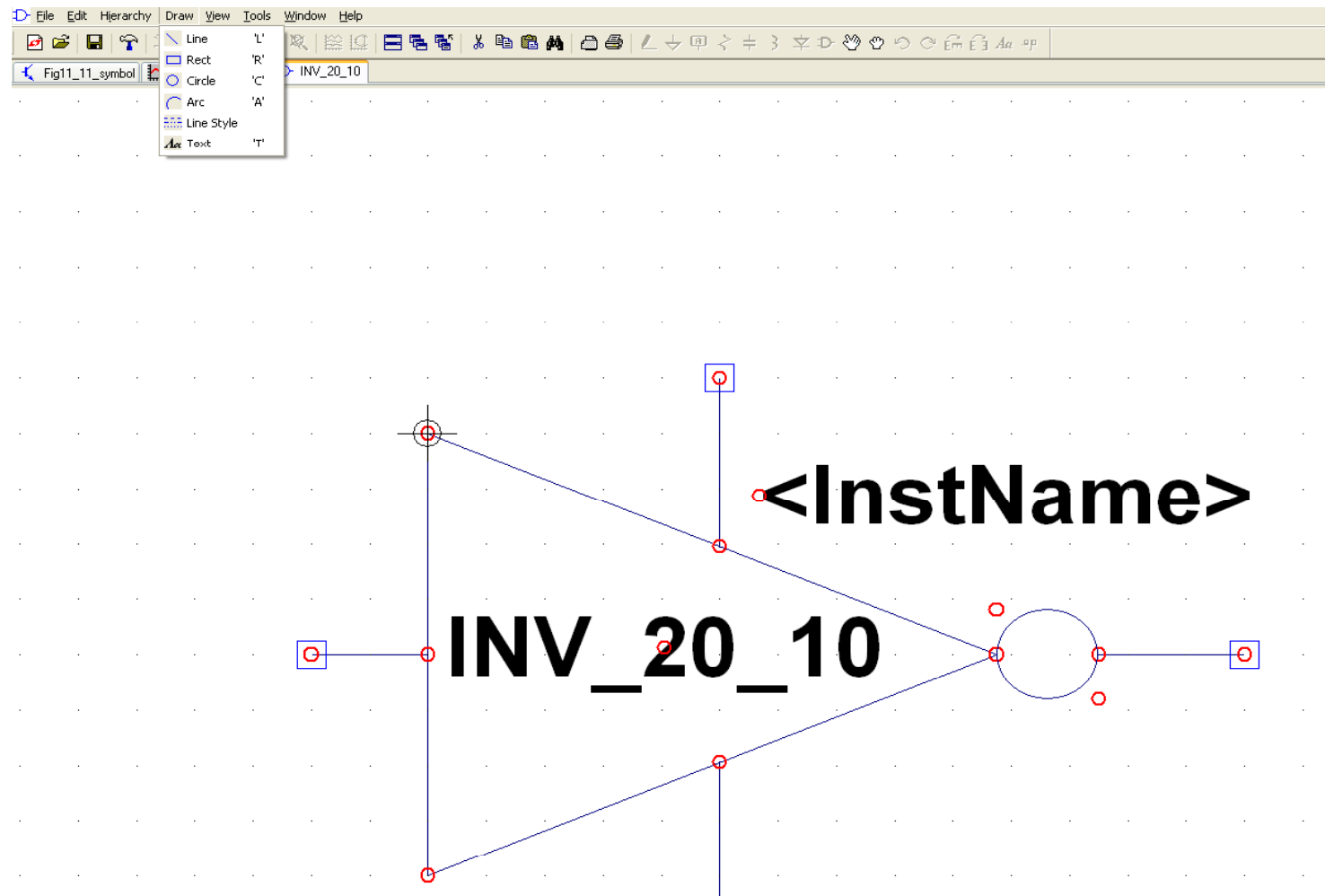


# Transient (time) Analysis

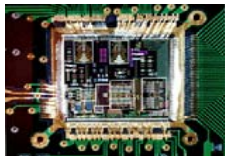
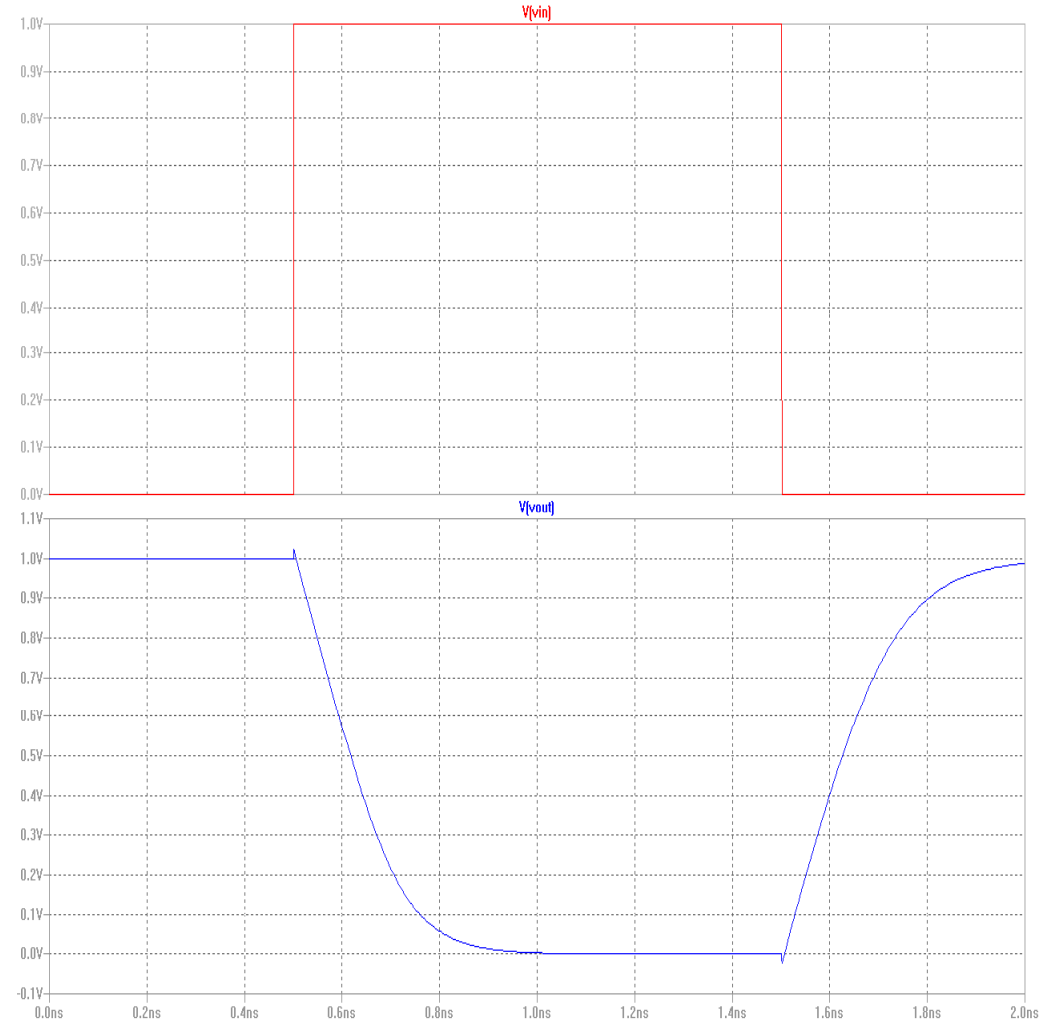
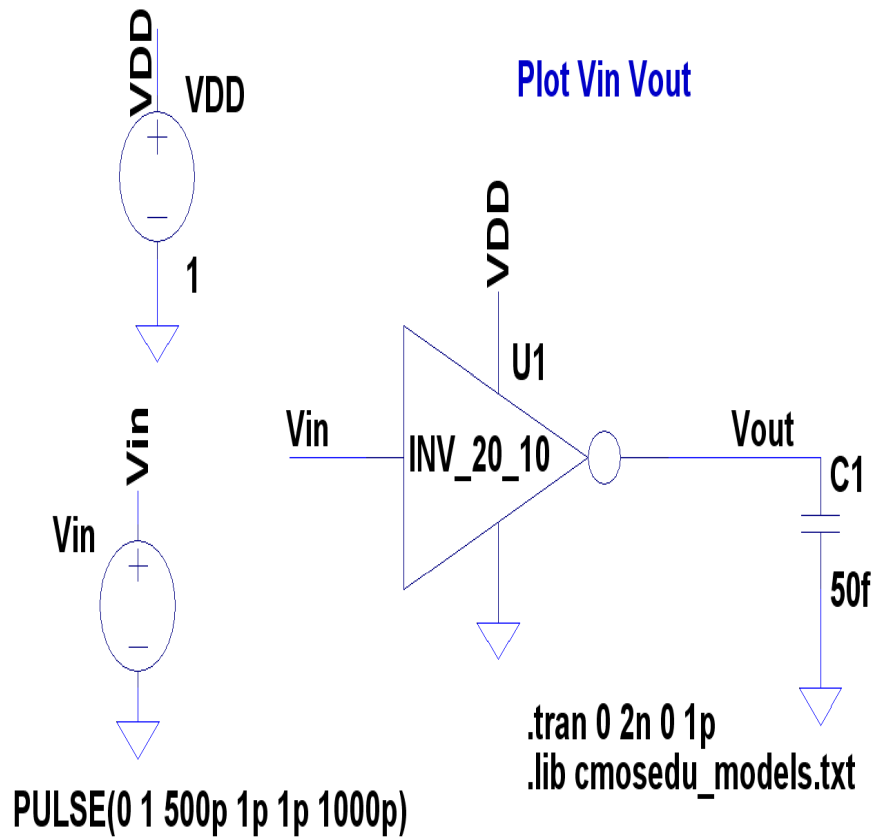


# Creating a symbol for Inverter

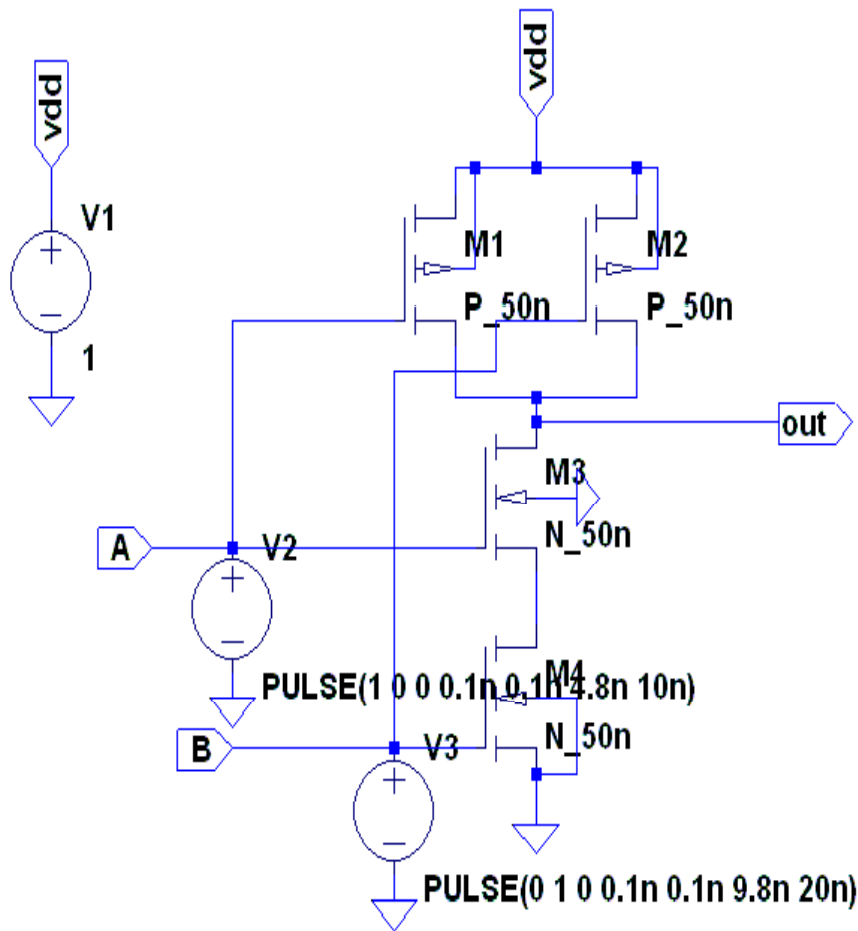
- Schematic files saved as \*.asc
- Symbol files saved as \*.asy



# Simulation using symbol: workspace much cleaner!



# One more example: NAND gate



.lib cmosedu\_models.txt

.tran 0 20n 0 100p

