CSCE 5730/4730: Digital CMOS VLSI Design

Assignment # 2, Total Marks = 2*50 = 100.
Assigned Date: 8th Feb 2010 (Mon), Due Date: 22nd Feb 2010 (Mon)
Instructor: Dr. Saraju P. Mohanty

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1. Using LTspice perform the transistor level static CMOS realization of an inverter gate. Perform its simulation to verify the truth table. Use 45nm PTM models.
2. Using LTspice perform the transistor level static CMOS realization of a NAND gate. Perform its simulation to verify the truth table. Use 32nm PTM models.