CSCE 5730/4730: Digital CMOS VLSI Design

Assignment # 3, Total Marks = 2*50 = 100.
Assigned Date: 1st Mar 2010 (Mon), Due Date: 8th Mar 2010 (Mon)
Instructor: Dr. Saraju P. Mohanty

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1. Cadence computer aided design (CAD) software tool has been installed in general access laboratory (GAL) of the college. Access the computers in GAL and list what are the individual tools that Cadence package contains. Briefly describe their usage and their functionalities.
2. Consider the following transistors: (1) SiO_2-bulk CMOS FET, (2) High-K CMOS FET, (3) Double gate FET, (4) Carbon Nanotube FET, and (5) Single Electron Transistor. Draw the cross section of these transistors clearing labeling each material, terminals, and dimensions.