CSCE 5730/4730: Digital CMOS VLSI Design

Assignment # 4, Total Marks = 4*25 = 100.
Assigned Date: 8th Mar 2010 (Mon), Due Date: 22nd Mar 2010 (Mon)
Instructor: Dr. Saraju P. Mohanty

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1. Using LTspice perform the transistor level static CMOS realization of 2-input logic gates (Inverter/NAND/NOR/AND/OR/XOR). Perform their simulation to verify the truth tables.
2. Synthesize the Boolean function $F = (\bar{A} \cdot B + C \cdot \bar{D})$. Show all the steps. Verify the circuit functionality using LTspice.
3. Design a D flip flop using 45nm technology in LTspice. Perform simulations to prove its functionality.
4. Perform the simulation of the above D flip flop for non-overlapping clocks.