CSCE 5730/4730: Digital CMOS VLSI Design

Assignment # 5, Total Marks = 2*50 = 100.
Assigned Date: 5th Apr 2010 (Mon), Due Date: 12th Apr 2010 (Mon)
Instructor: Dr. Saraju P. Mohanty

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1. Design the transistor-level circuit for a 3-input majority gate. Show all the steps of your design starting from the truth table.
2. Perform the simulation of the above circuit by PSPICE using generic MOS devices, such as those available in the BREAKOUT PSpice library.