

# Lecture 4: Device Theory

## CSCE 5730 Digital CMOS VLSI Design

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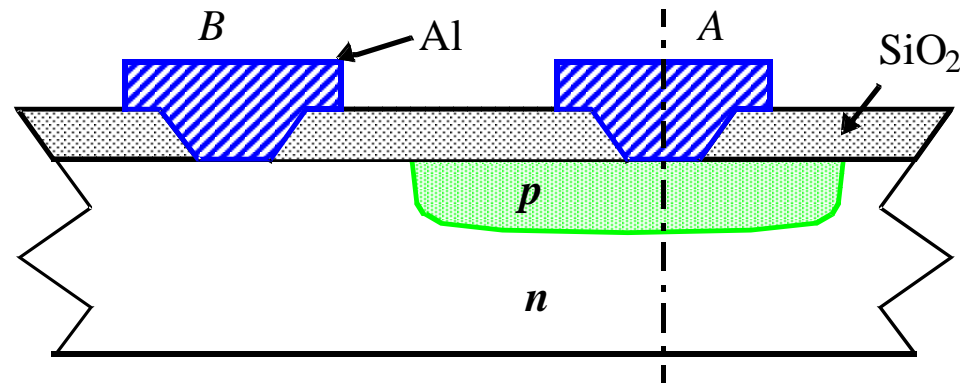


# Outline of the Lecture

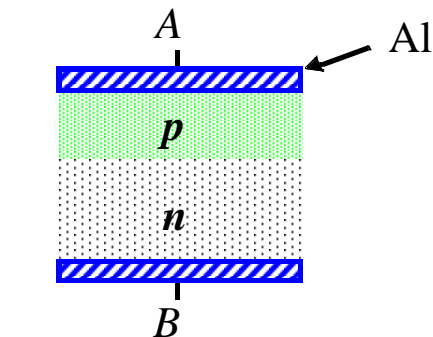
- Present intuitive understanding of device operation
- Introduction of basic device equations
- Introduction of models for manual analysis
- Introduction of models for SPICE simulation
- Analysis of secondary effects



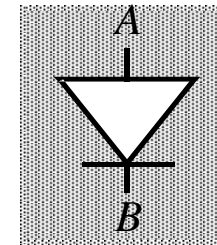
# The Diode



Cross-section of  $pn$ -junction in an IC process



One-dimensional representation

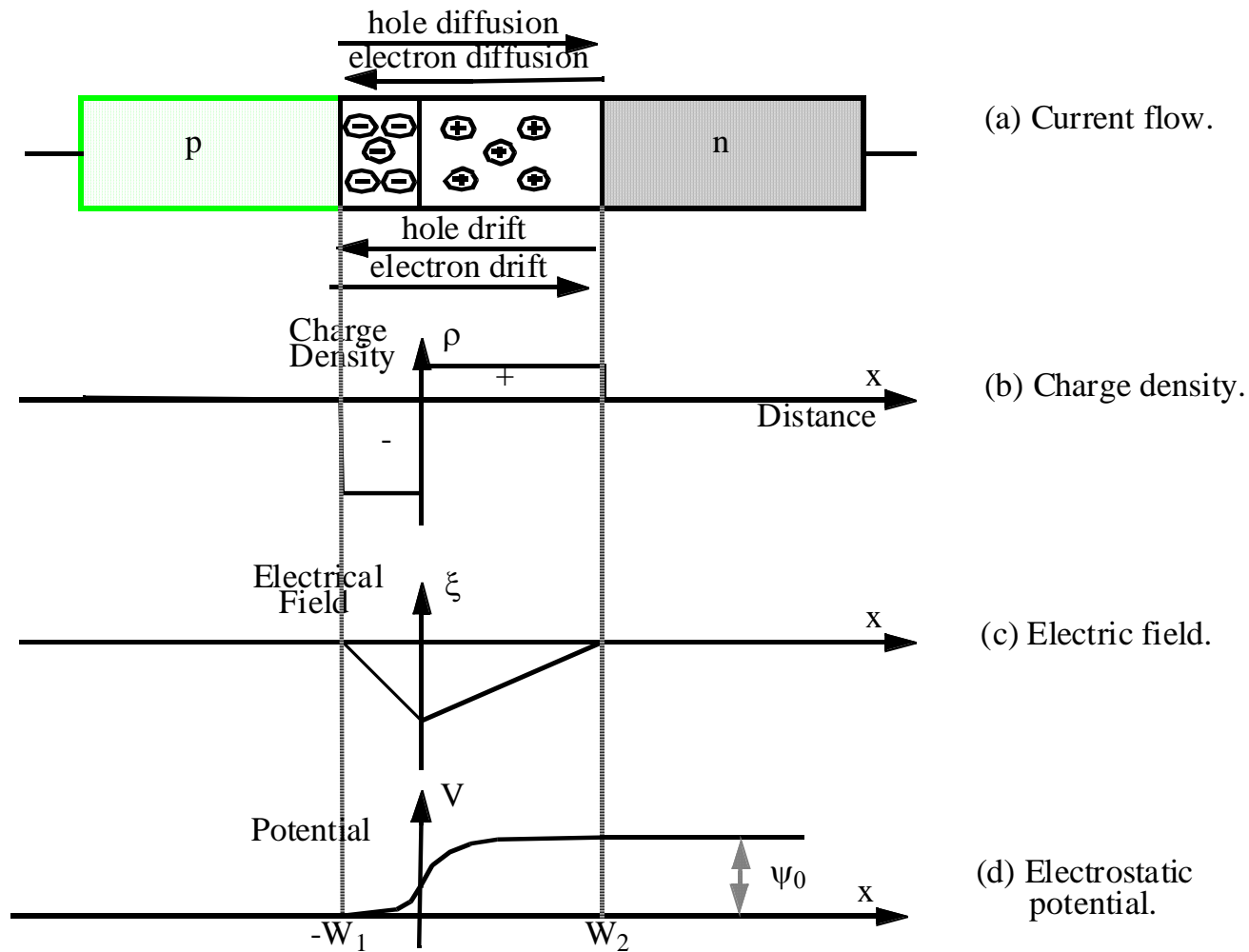


diode symbol

*Mostly occurring as parasitic element in Digital ICs*



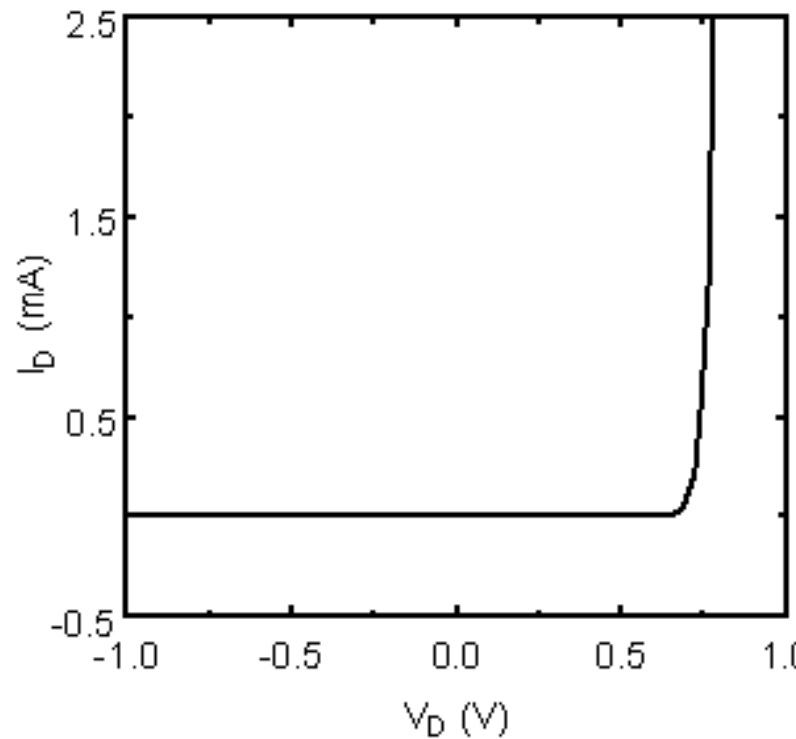
# Depletion Region



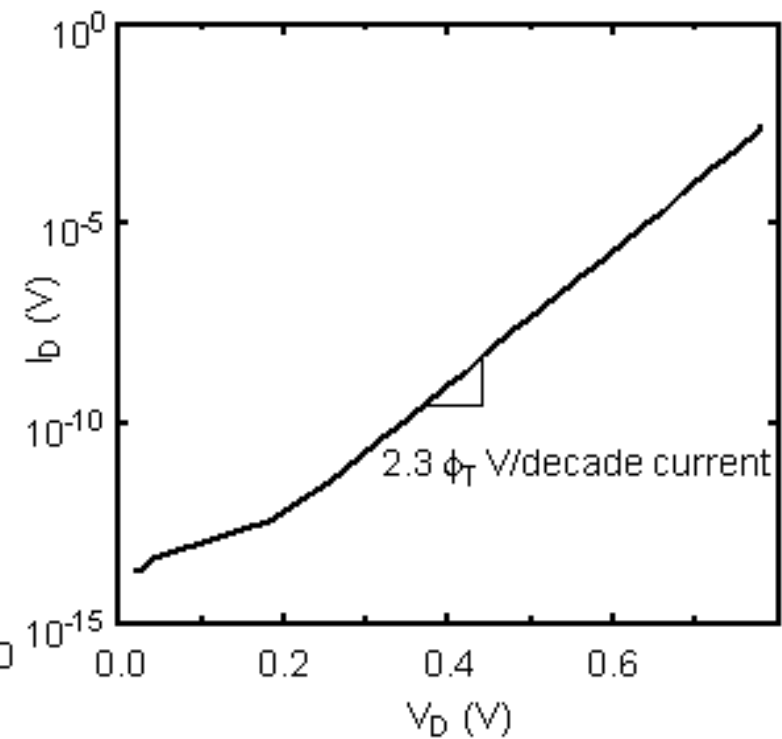
**NOTE:** Solve Example 3.1, page-76, Rabaey book.



# Diode Current

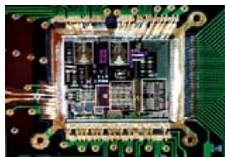


(a) On a linear scale.

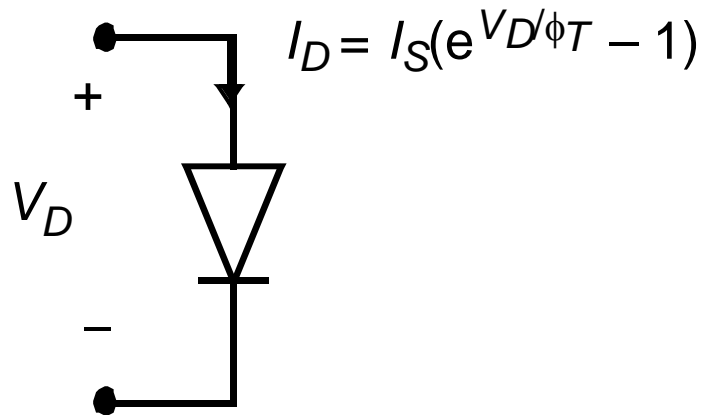


(b) On a logarithmic scale (forward bias).

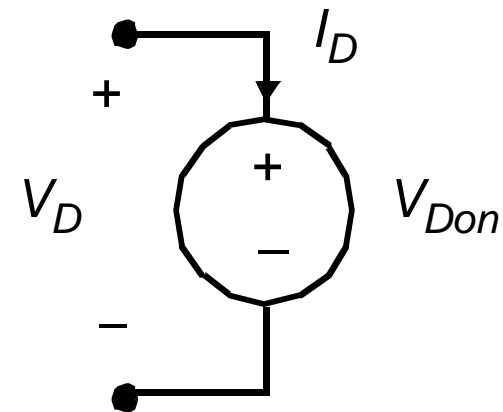
$$I_D = I_S \left( e^{V_D / \phi_T} - 1 \right)$$



# Diode Models for Manual Analysis



(a) Ideal diode model

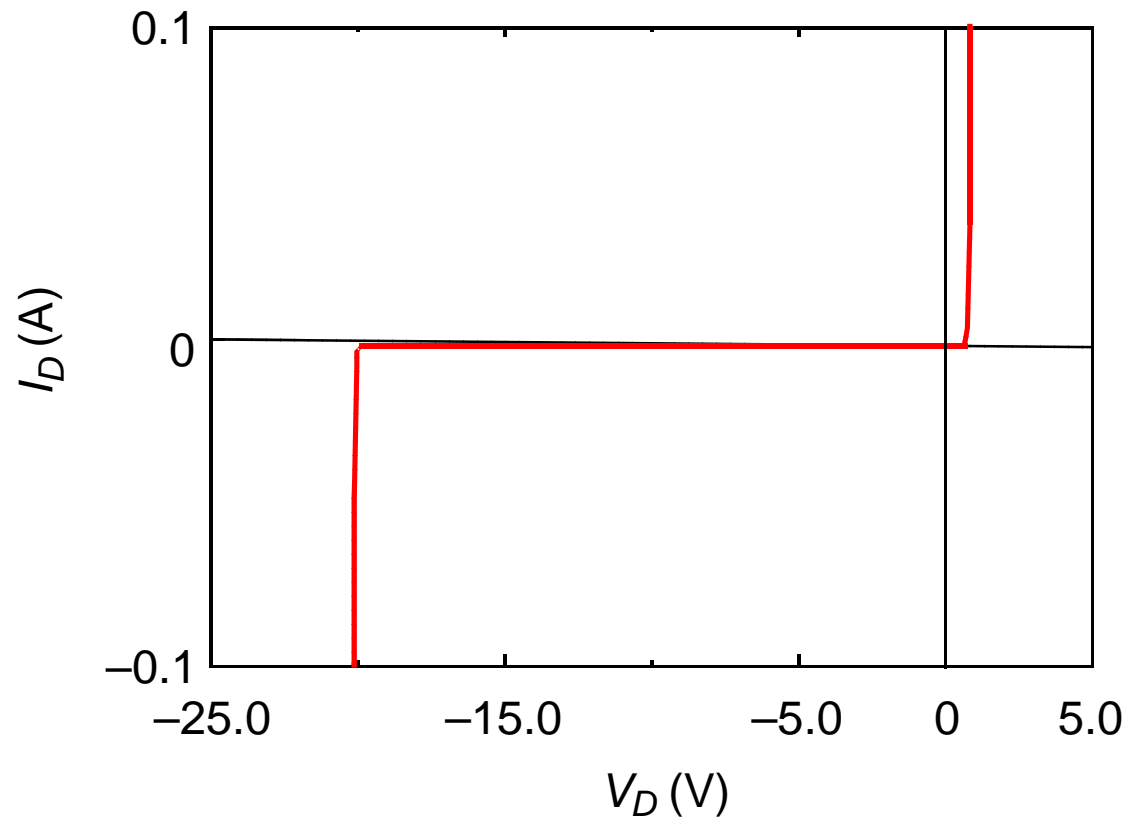


(b) First-order diode model

**NOTE:** Solve Example 3.2, page-80, Rabaey book.



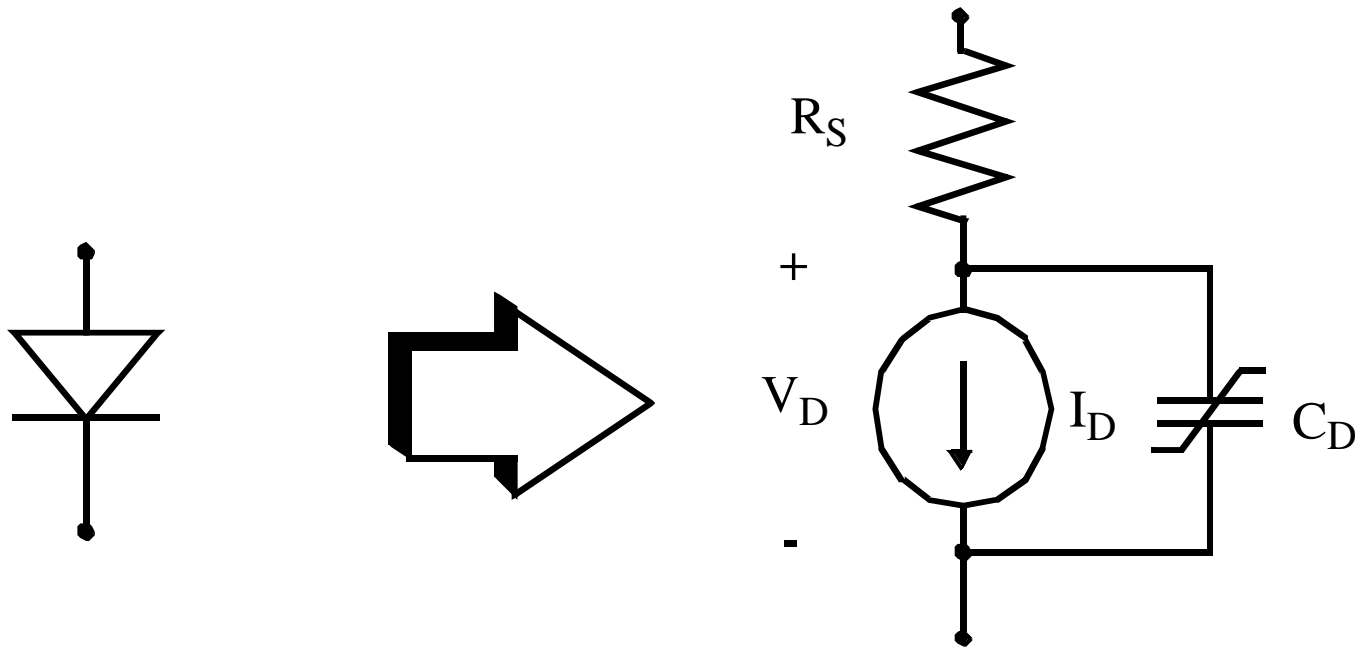
# Diode: Secondary Effects



**Avalanche Breakdown**



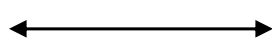
# Diode : SPICE Model



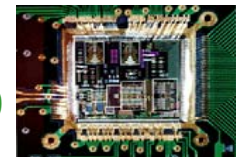
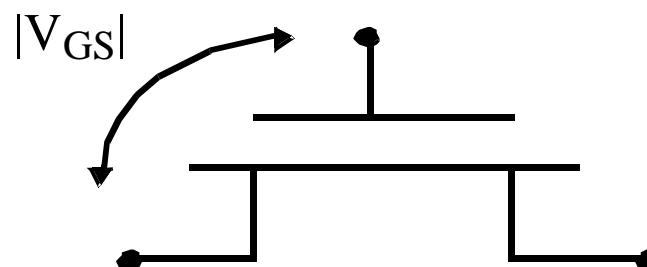
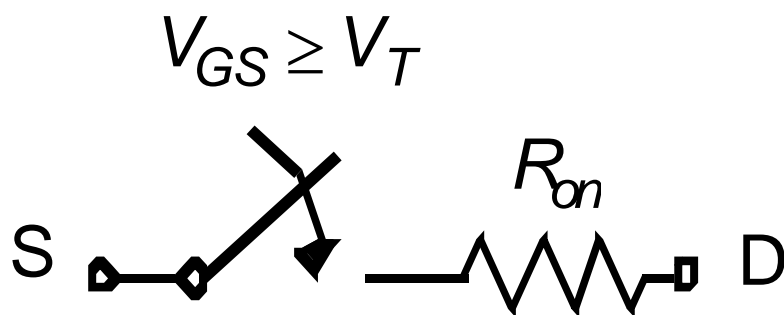


# What is a Transistor?

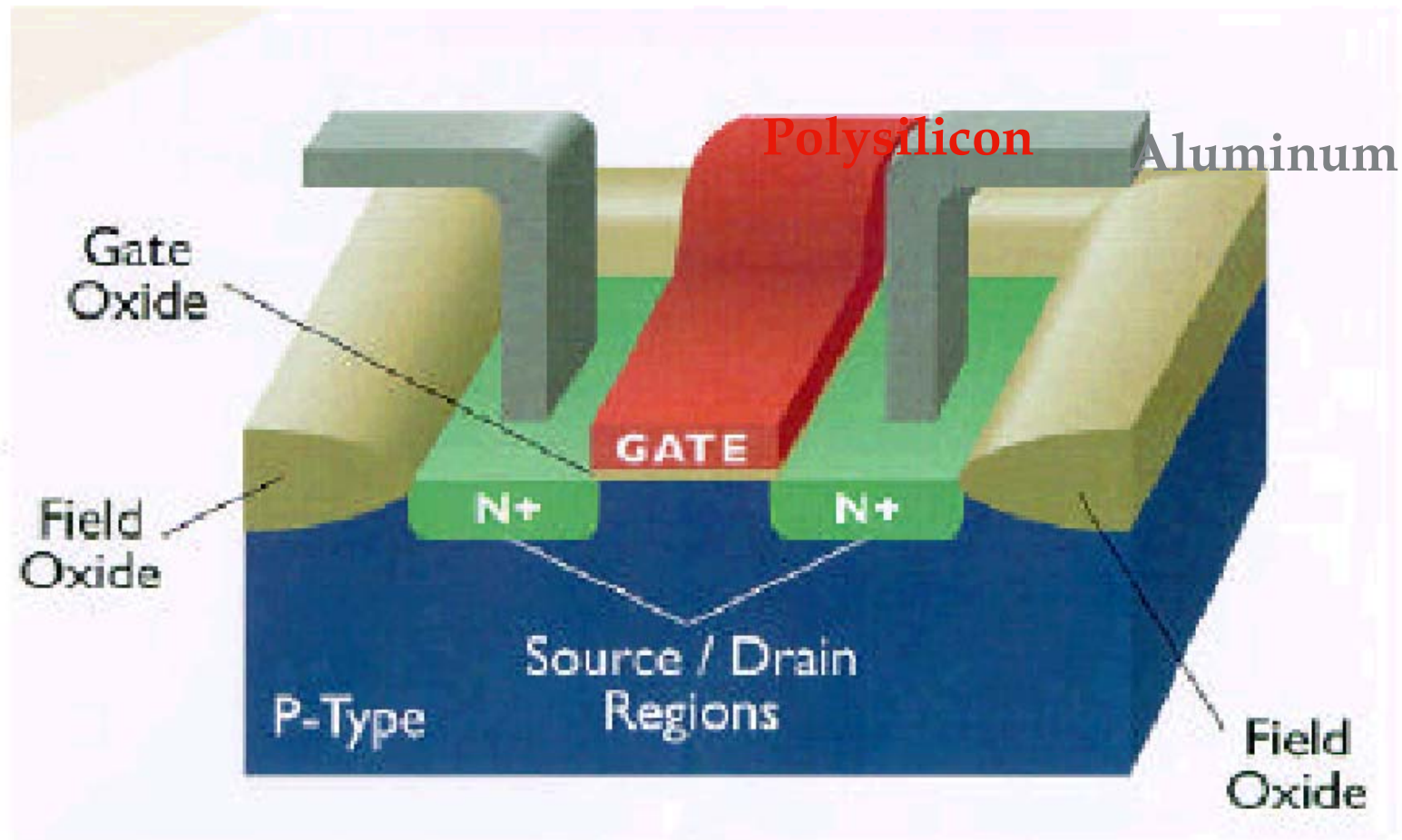
A Switch!



An MOS Transistor

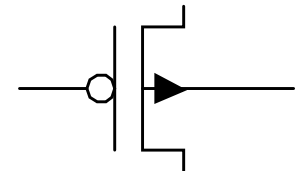
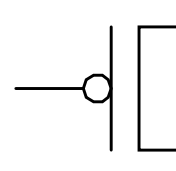
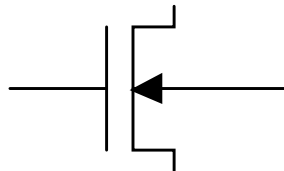
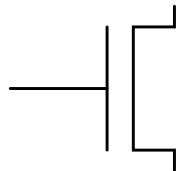


# The MOS Transistor

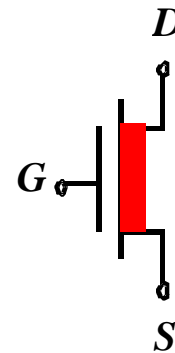
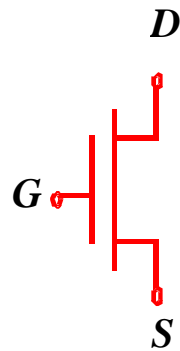


# Some Facts about MOS Transistor

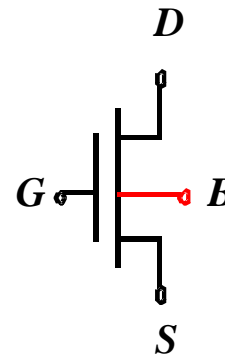
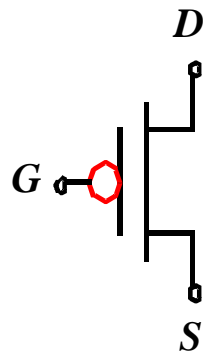
- MOS is a majority carrier device in which the current in a conducting channel between source and drain is controlled by voltage applied to the gate.
- Majority carriers: NMOS-electron and PMOS-hole
- When ON, the MOS transistor passes a finite amount of current in channel.
  - Depends on terminal voltages
  - Derive current-voltage (I-V) relationships
- Transistor's gate, source, drain have capacitance
- Different symbols for NMOS/PMOS:



# MOS Transistors - Types and Symbols

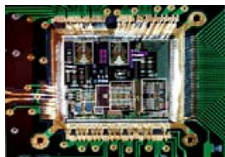


**NMOS Enhancement    NMOS Depletion**



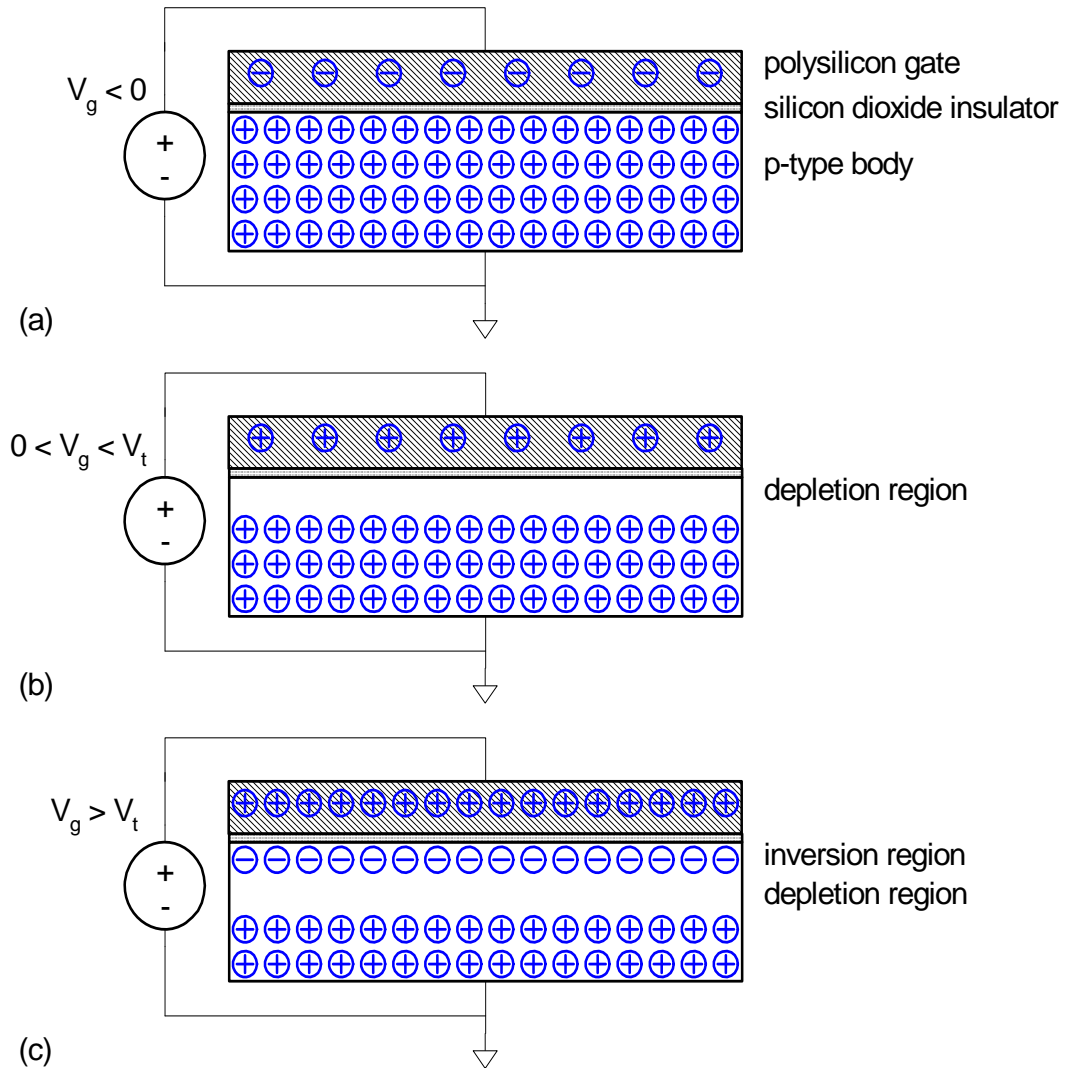
**PMOS Enhancement**

**NMOS with Bulk Contact**

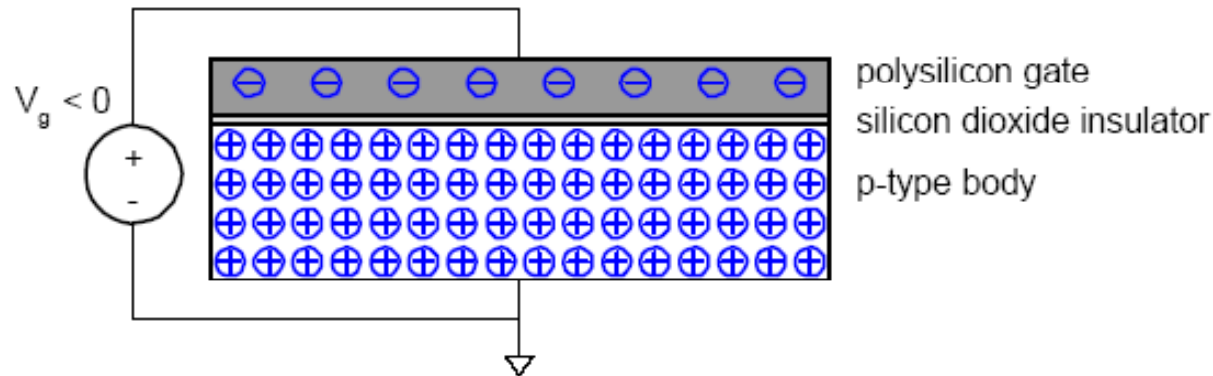


# MOS Modes of Operation

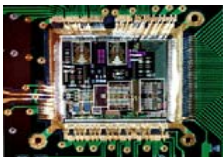
- Gate and body form MOS capacitor
- Three operating modes
  - Accumulation
  - Depletion
  - Inversion



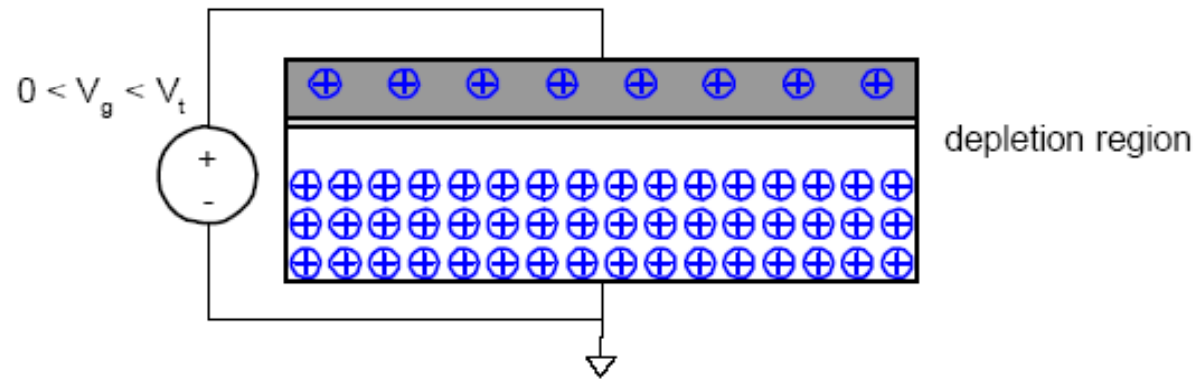
# MOS Modes of Operation : Accumulation



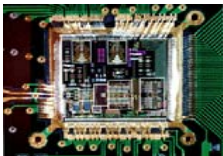
- When a negative voltage is applied to gate, there is negative charge on the gate.
- The mobile positive carriers are attracted to the region below the gate.



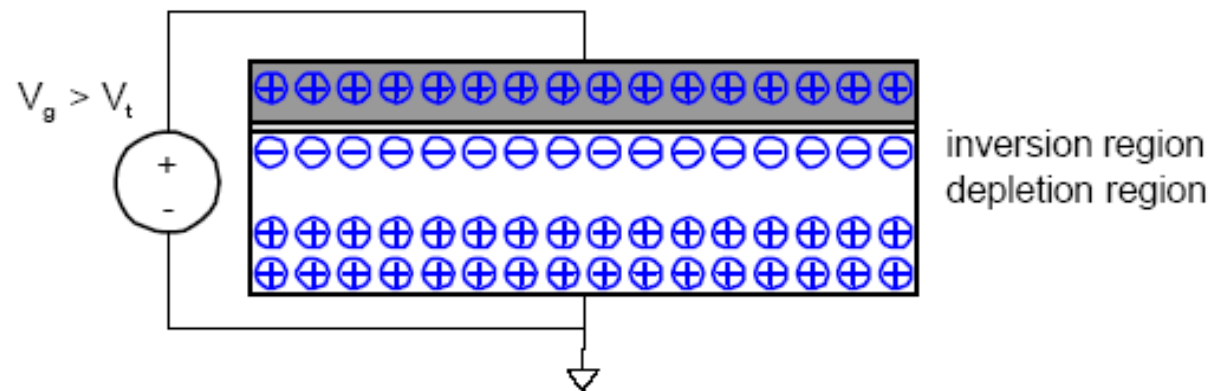
# MOS Modes of Operation : Depletion



- A low positive voltage at the gate results in some positive charge on the gate.
- The holes in the body i.e. mobile positive carriers are repelled from the region below the gate; thus forming a depletion region.



# MOS Modes of Operation : Inversion



- A higher positive potential (more than threshold voltage) attracts more positive charge to the gate.
- The holes in the body are repelled further and small number of electrons in the body are attracted to the region below the gate.
- This conductive electrons form inversion layer.





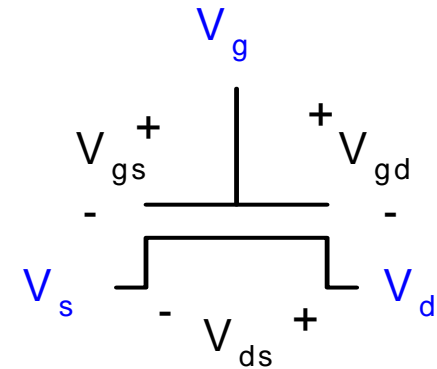
# MOS regions of operation

- Operations depends on  $V_g$ ,  $V_d$ ,  $V_s$

$$-V_{gs} = V_g - V_s$$

$$-V_{gd} = V_g - V_d$$

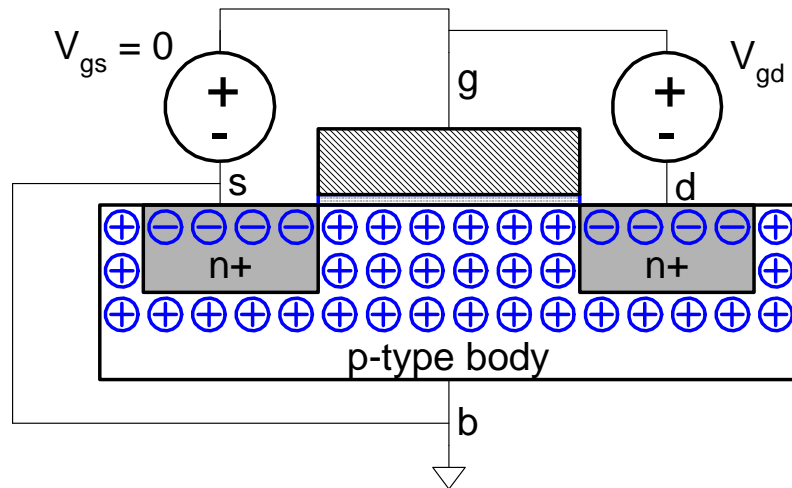
$$-V_{ds} = V_d - V_s = V_{gs} - V_{gd}$$



- Source and drain are symmetric diffusion terminals
  - By convention, source is terminal at lower voltage
  - Hence  $V_{ds} \geq 0$
- NMOS body is grounded.
- Three regions of operation
  - Cutoff
  - Linear
  - Saturation



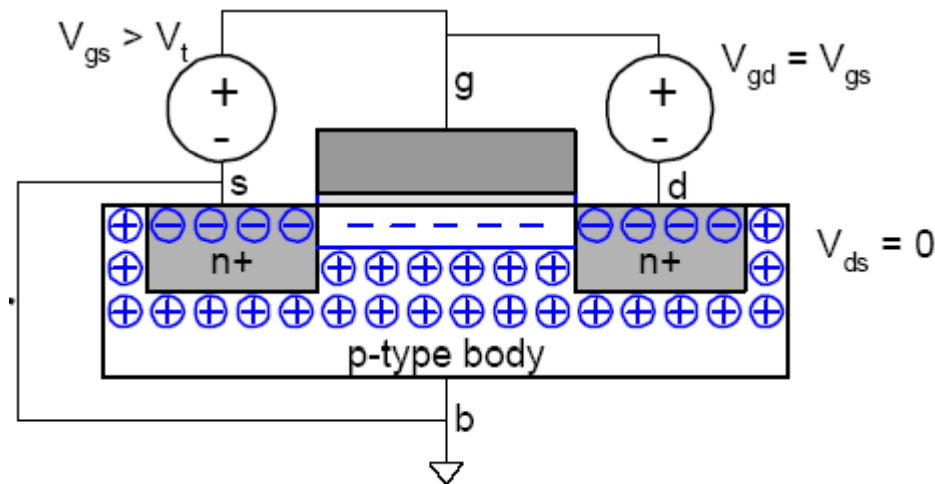
# NMOS regions of operation : Cutoff



- Gate to source voltage ( $V_{gs}$ ) is less than threshold voltage ( $V_T$ )
- Source and drain have free electrons.
- Body has free holes, but no free electrons.
- No channel
- $I_{ds} = 0$



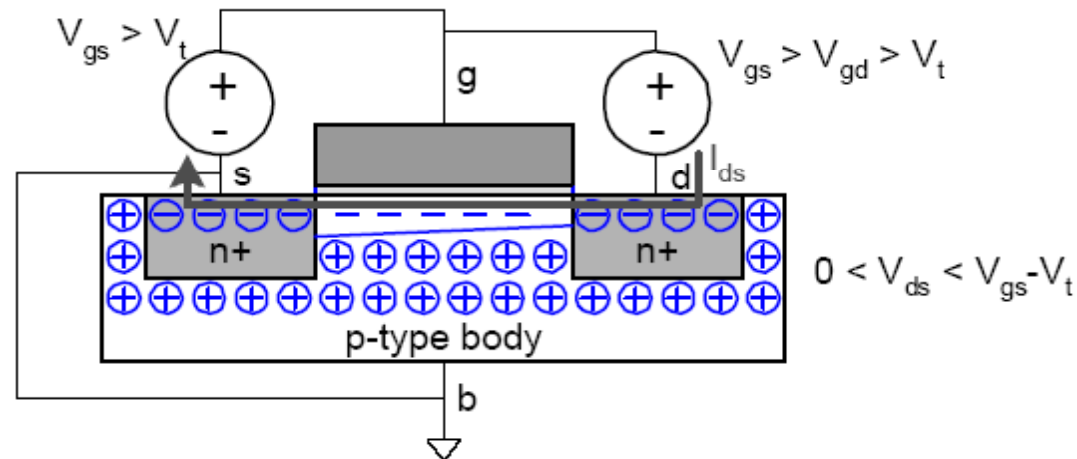
# NMOS regions of operation : Linear



- When,  $V_{gs} > V_T$ ,  $V_{gd} = V_{gs}$  and  $V_{ds} = 0$
- Inversion region of electrons form a channel
- Since  $V_{ds} = 0$ , there is no electric field to push current from drain to source.
- Number of carriers and conductivity can increase with the gate voltage, and  $I_{ds}$  can increase with  $V_{ds}$



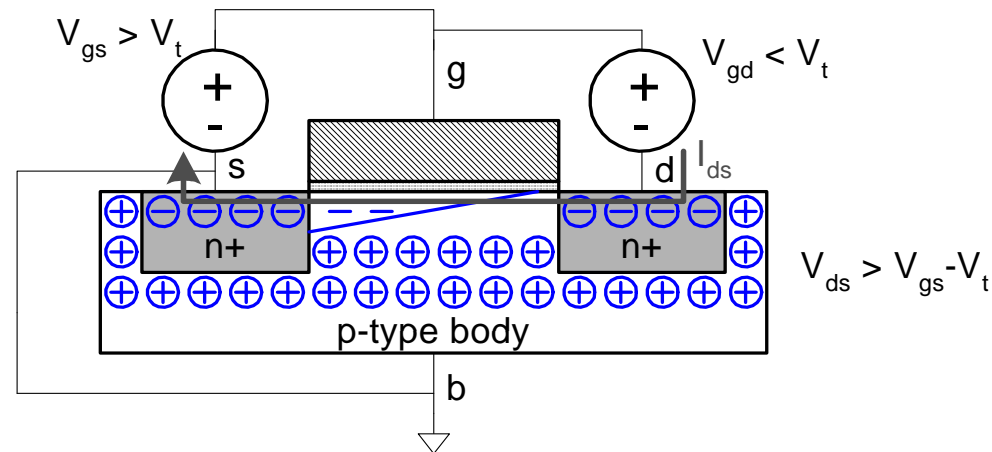
# NMOS regions of operation : Linear ...



- When  $V_{gs} > V_T$ ,  $V_{gs} > V_{gd} > V_T$ , and  $0 < V_{ds} < V_{gs} - V_T$
- Since  $V_{ds} > 0$ , there is electric field to push current from drain to source.
- Current flows from d to s (i.e.  $e^-$  from s to d)
- Drain-to-source current  $I_{ds}$  increases with  $V_{ds}$
- Linear mode of operation is also known as resistive and nonsaturated or unsaturated.



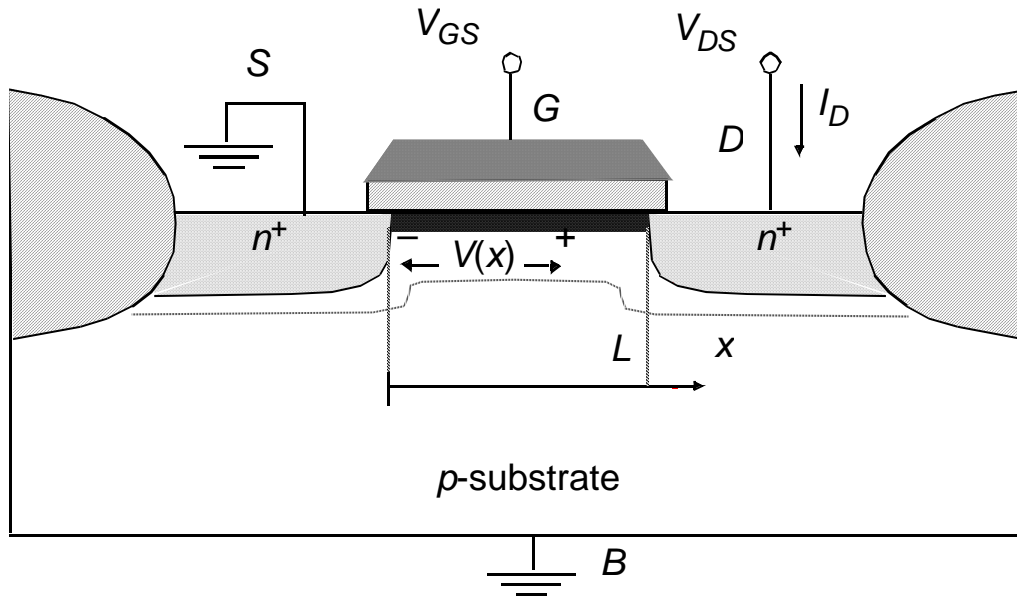
# NMOS regions of operation : Saturation



- When  $V_{gs} > V_T$ ,  $V_{gd} < V_T$ , and  $V_{ds} > V_{gs} - V_T$
- Channel is not inverted near drain and becomes pinched off
- There is still conduction due to drifting motion of the electron
- $I_{ds}$  independent of  $V_{ds}$  and depends on  $V_{gs}$  only.
- We say current saturates as current does not change much
- Similar to current source



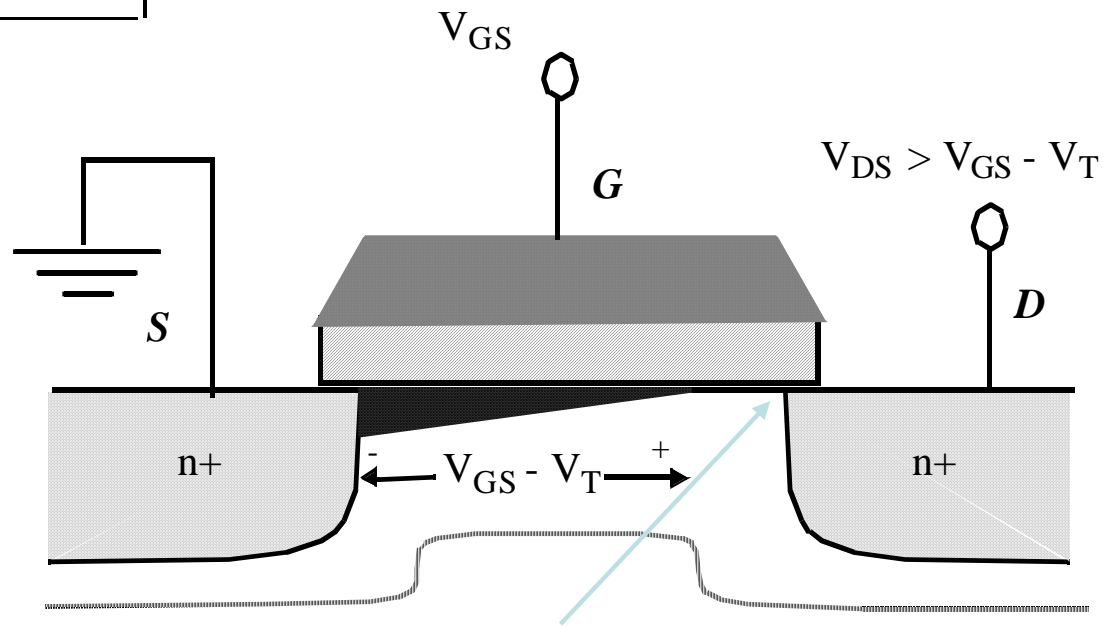
# Transistor : Pinch-off Condition



(Linear Region)

MOS transistor and its bias conditions

(Saturation Region)



Pinch-off



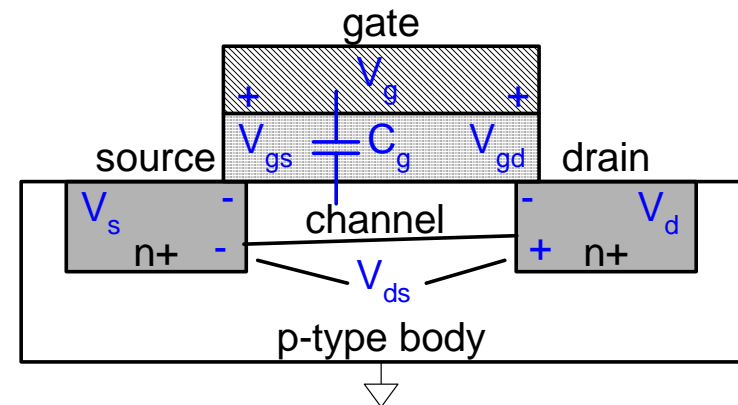
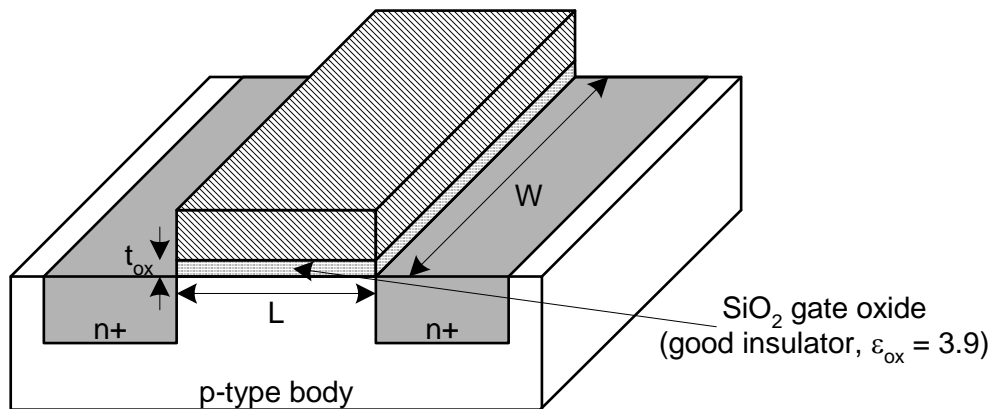
# I-V Characteristics

- Three regions of operation:
  - Cut-off
  - Linear
  - Saturation
- In Linear region,  $I_{ds}$  depends on
  - How much charge is in the channel?
  - How fast is the charge moving?



# I-V Characteristics : Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- The charge in channel,  $Q_{\text{channel}} = CV$
- $C = C_g = \epsilon_{\text{ox}} WL / t_{\text{ox}} = C_{\text{ox}} WL$  (where,  $C_{\text{ox}} = \epsilon_{\text{ox}} / t_{\text{ox}}$ )
- $V = V_{\text{gc}} - V_T = (V_{\text{gs}} - V_{\text{ds}}/2) - V_T$
- Where, average gate to channel voltage  $V_{\text{gc}} = (V_{\text{gs}} + V_{\text{ds}}) / 2 = (V_{\text{gs}} - V_{\text{ds}}/2)$





# I-V Characteristics : Carrier velocity

- Charge is carried by e- (for NMOS)
- Carrier velocity  $v$  proportional to lateral electric field between source and drain
  - $v = \mu E$  (where,  $\mu$  called mobility)
- Electric field between source-drain,
  - $E = V_{ds}/L$
- Time for carrier to cross channel:
  - $t = L / v$



# I-V Characteristics : Linear

- Now we know
  - How much charge  $Q_{\text{channel}}$  is in the channel
  - How much time  $t$  each carrier takes to cross
- The current between source-to-drain is the total amount charge in the channel divided by the time to cross channel.

$$\begin{aligned} I_{ds} &= \frac{Q_{\text{channel}}}{t} \\ &= \mu C_{\text{ox}} \frac{W}{L} \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} \\ &= \beta \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} \end{aligned} \quad \beta = \mu C_{\text{ox}} \frac{W}{L}$$



# I-V Characteristics : Saturation

- If  $V_{gd} < V_t$ , channel pinches off near drain
- The drain voltage at which current is no longer affected by it is known as drain saturation voltage.
  - When  $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

$$\begin{aligned} I_{ds} &= \beta \left( V_{gs} - V_t - \frac{V_{dsat}}{2} \right) V_{dsat} \\ &= \frac{\beta}{2} (V_{gs} - V_t)^2 \end{aligned}$$



# I-V Characteristics : Summary

- Shockley 1st order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{cutoff} \\ \beta \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & V_{ds} < V_{dsat} & \text{linear} \\ \frac{\beta}{2} (V_{gs} - V_t)^2 & V_{ds} > V_{dsat} & \text{saturation} \end{cases}$$

- The current at which transistor is fully ON  $I_{dsat}$ :

$$I_{dsat} = \beta/2 (V_{DD} - V_t)^2$$

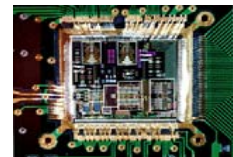
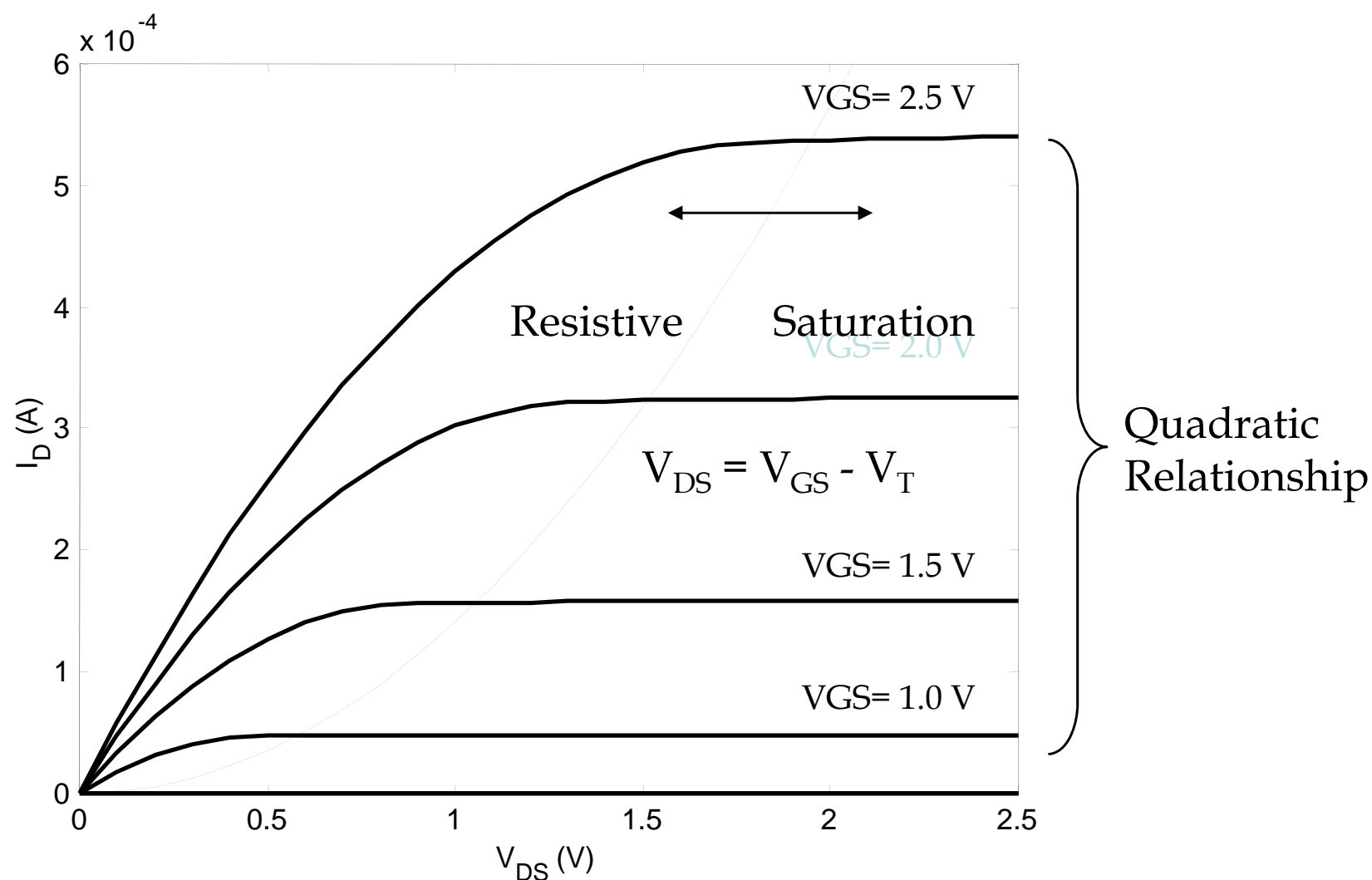


# MOSFET Operating Regions : Summary

- Strong Inversion  $V_{GS} > V_T$ 
  - Linear (Resistive)  $V_{DS} < V_{DSAT}$
  - Saturated (Constant Current)  $V_{DS} \geq V_{DSAT}$
- Weak Inversion (Sub-Threshold)  $V_{GS} \leq V_T$ 
  - Exponential in  $V_{GS}$  with linear  $V_{DS}$  dependence

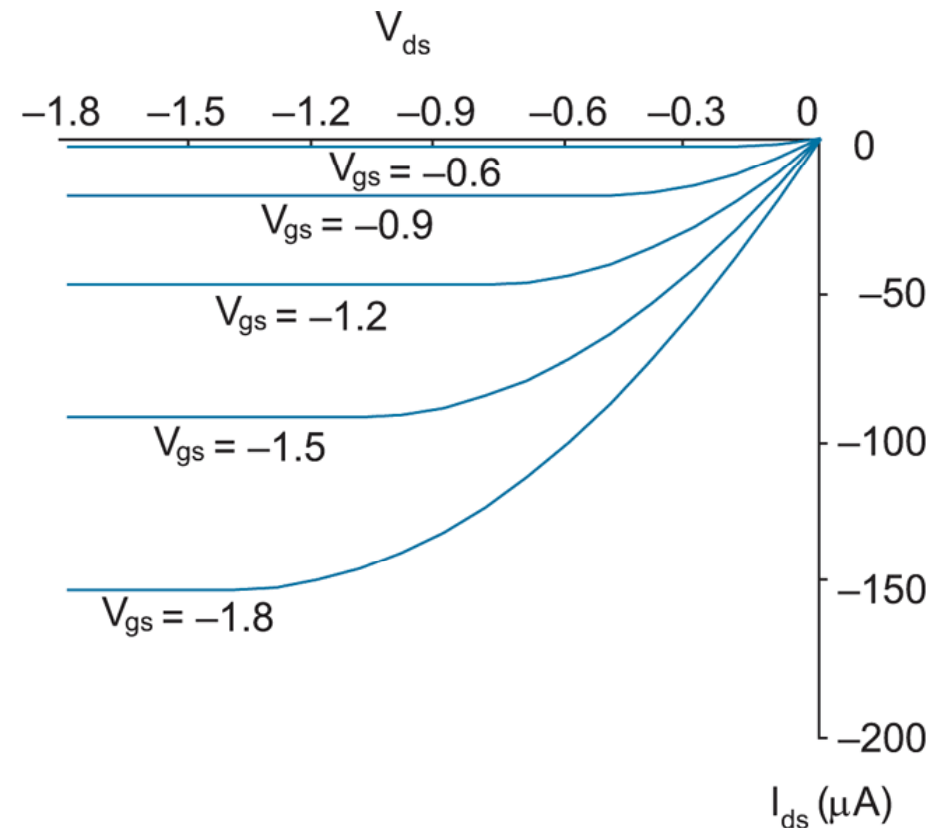


# Current-Voltage Relations



# I-V Characteristics : PMOS

- All dopings and voltages are inverted for PMOS
- Mobility  $\mu_p$  is determined by holes
  - Typically 2-3x lower than that of electrons  $\mu_n$
- Thus PMOS must be wider to provide same current
  - Typically,  $\mu_n / \mu_p = 2$

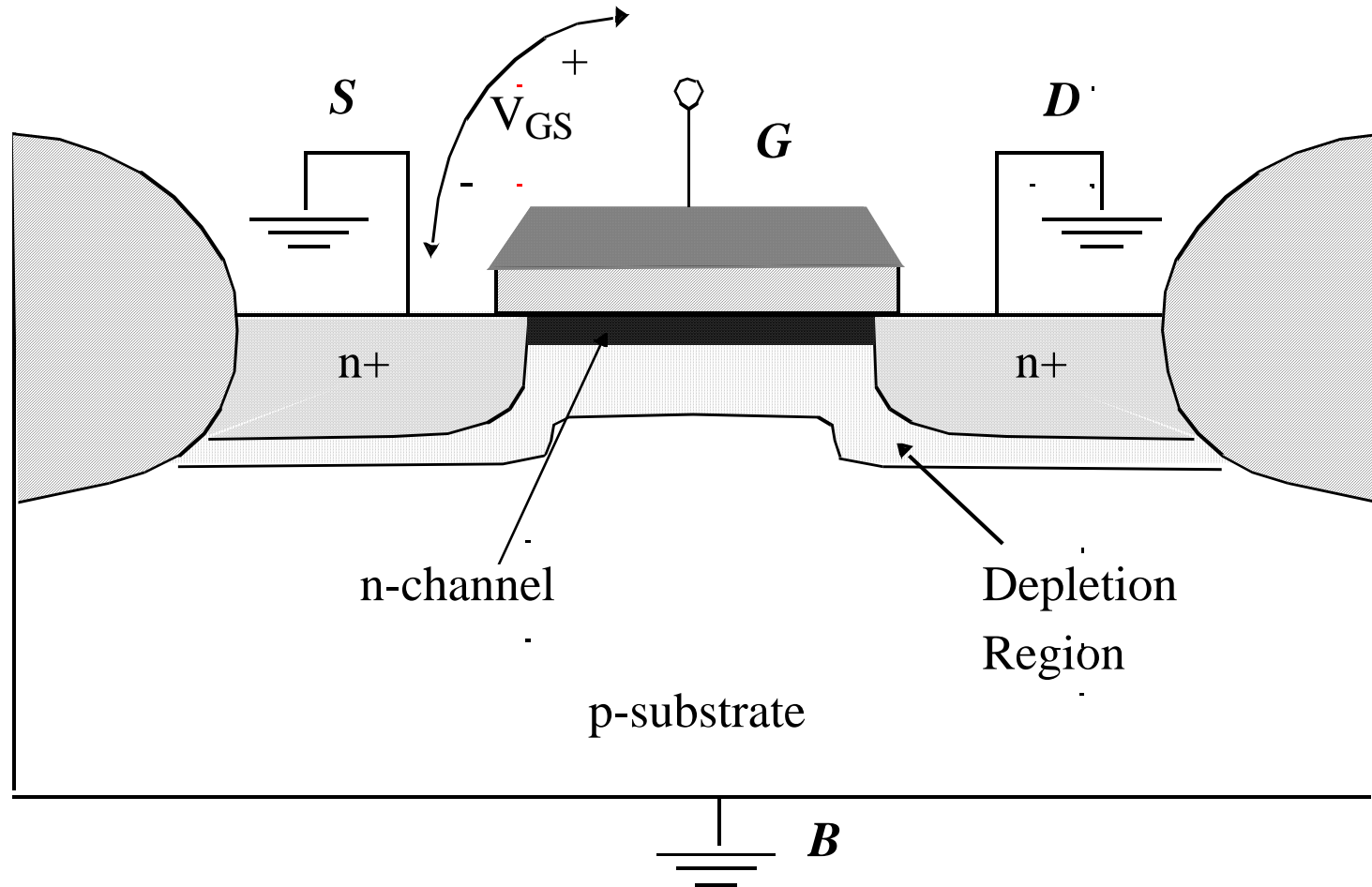


I-V characteristics of ideal pMOS transistor

Assume all variables negative!



# Threshold Voltage: Concept





# The Threshold Voltage

$$V_T = \phi_{ms} - 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}}$$

Workfunction Difference  
 Depletion Layer Charge  
 Surface Charge  
 Implants

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

Body Effect Coefficient

with

$$V_{T0} = \phi_{ms} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}}$$

and

$$\gamma = \frac{\sqrt{2q\epsilon_{si}N_A}}{C_{ox}}$$



# Current-Voltage Relations Long-Channel Device

**Linear Region:  $V_{DS} \leq V_{GS} - V_T$**

$$I_D = k'_n \frac{W}{L} \left( (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

with

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \epsilon_{ox}}{t_{ox}}$$

Process Transconductance  
Parameter

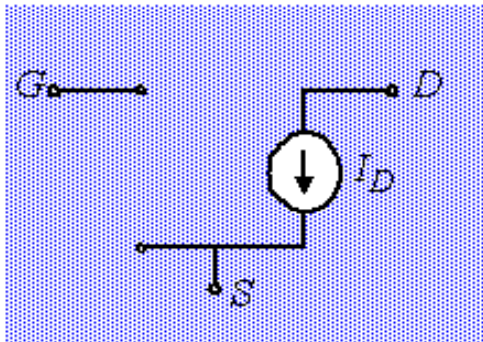
**Saturation Mode:  $V_{DS} \geq V_{GS} - V_T$**

$$I_D = \frac{k'_n W}{2 L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

Channel Length Modulation  
↙



# A model for manual analysis



$$V_{DS} > V_{GS} - V_T$$

$$I_D = \frac{k'_n W}{2 L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

$$V_{DS} < V_{GS} - V_T$$

$$I_D = k'_n \frac{W}{L} \left( (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

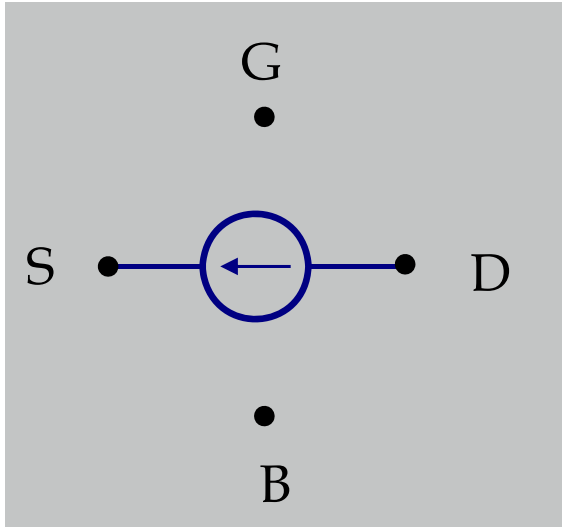
with

$$V_T = V_{T0} + \gamma (\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

**NOTE:** Solve Example 3.5, page-90, Rabaey book.



# A unified model for manual analysis



$$I_D = 0 \text{ for } V_{GT} \leq 0$$

$$I_D = k' \frac{W}{L} \left( V_{GT} V_{min} - \frac{V_{min}^2}{2} \right) (1 + \lambda V_{DS}) \text{ for } V_{GT} \geq 0$$

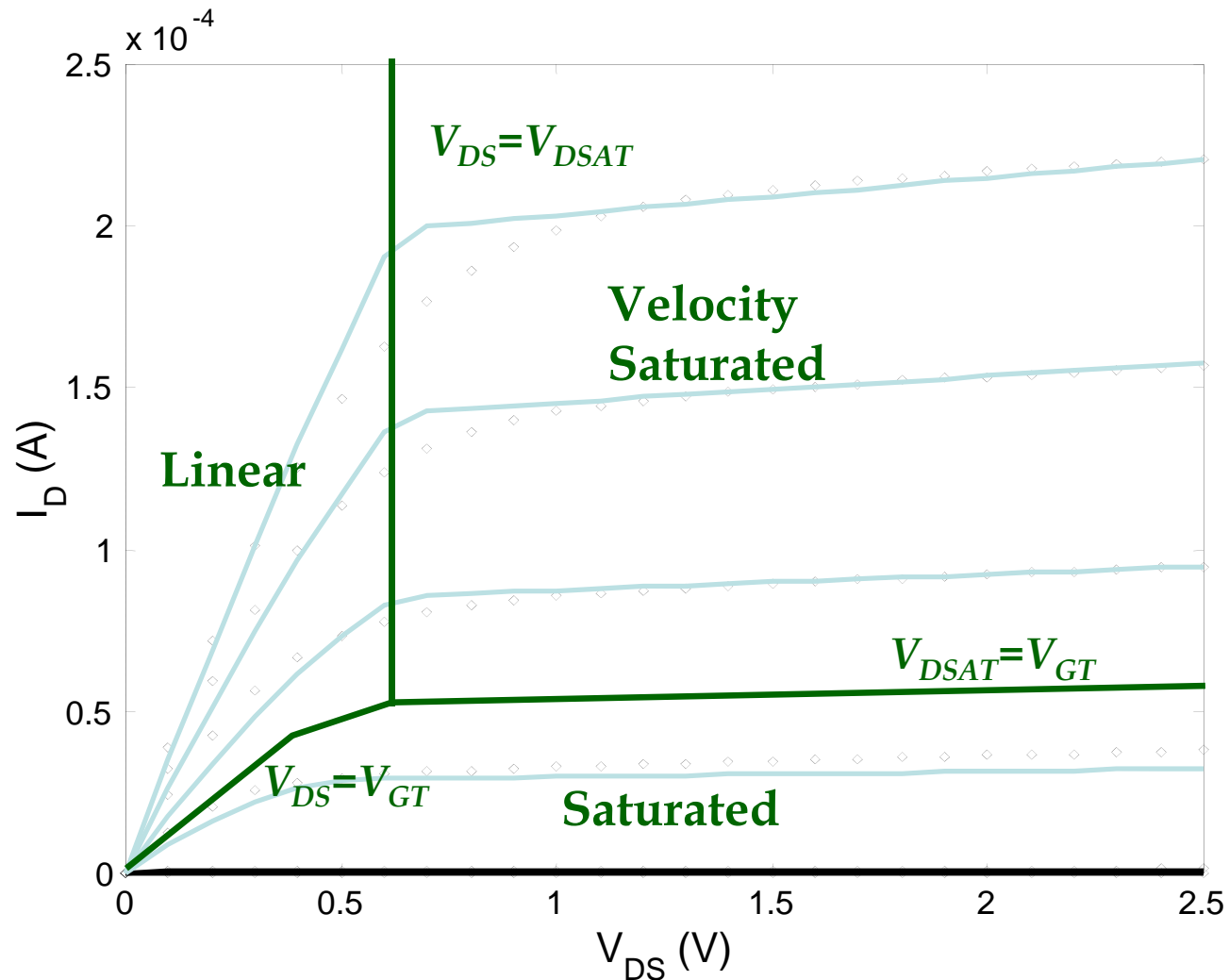
with  $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$ ,

$$V_{GT} = V_{GS} - V_T,$$

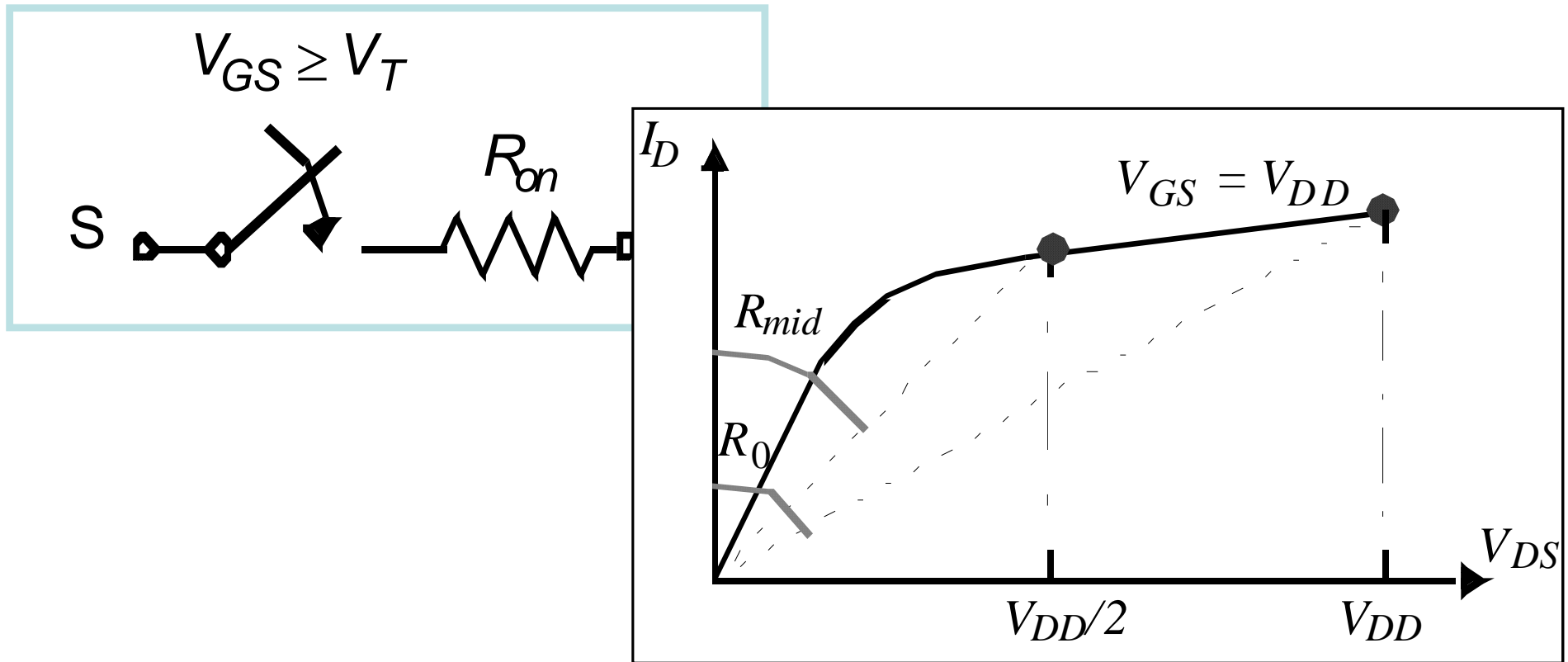
$$\text{and } V_T = V_{T0} + \gamma (\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$



# Simple Model versus SPICE

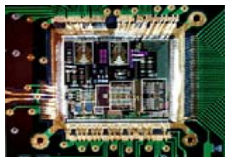


# The Transistor as a Switch

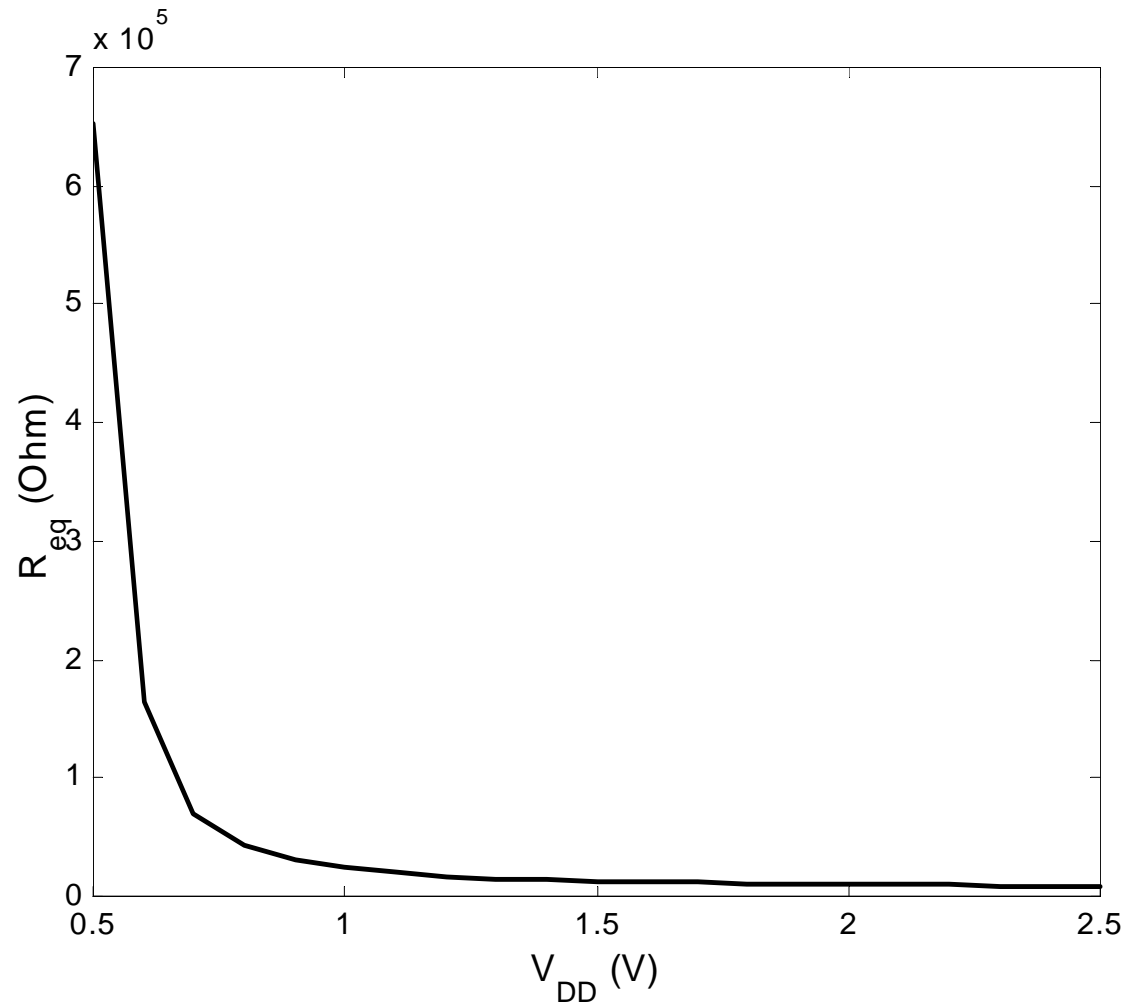


$$R_{eq} = \frac{1}{2} \left( \frac{V_{DD}}{I_{DSAT}(1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1 + \lambda V_{DD}/2)} \right) \approx \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left( 1 - \frac{5}{6} \lambda V_{DD} \right)$$

**NOTE:** Example 3.8, page-104, Rabaey book has the derivations.



# The Transistor as a Switch



# C-V Characteristics

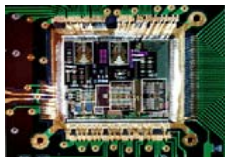
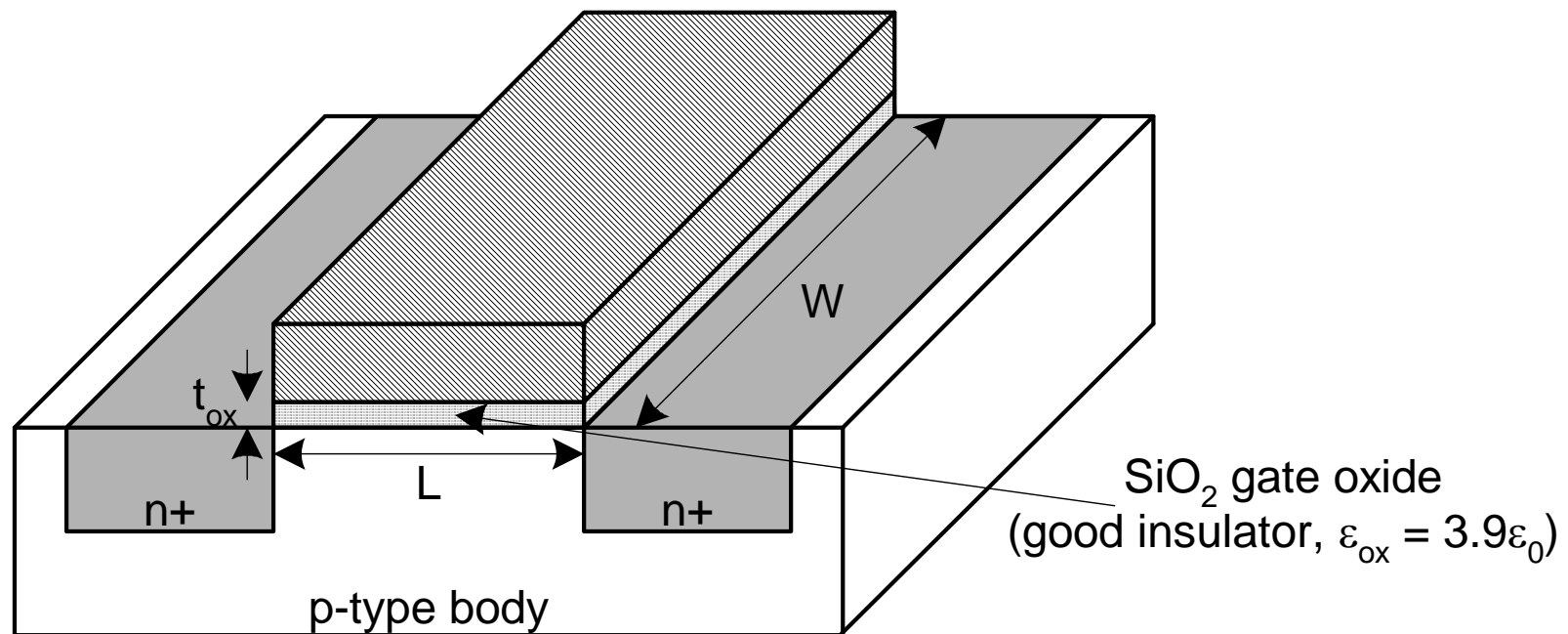
- Any two conductors separated by an insulator have capacitance
- Gate to channel capacitor is very important
  - Creates channel charge necessary for operation
- Source and drain have capacitance to body
  - Across reverse-biased diodes
  - Called diffusion capacitance because it is associated with source/drain diffusion
- In general these capacitances are nonlinear and voltage dependent, but can be approximated as simple capacitors.



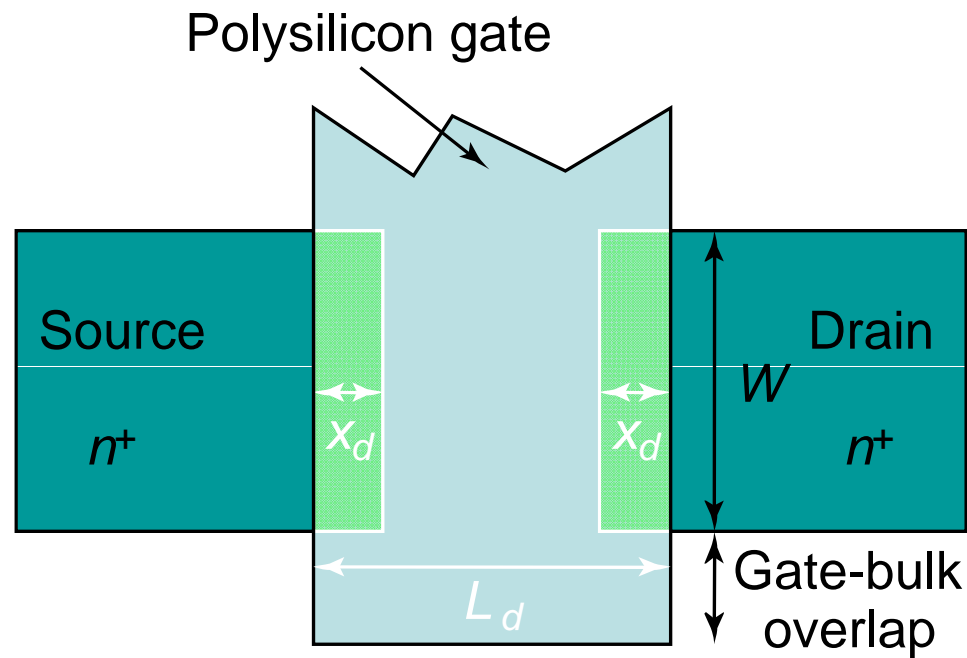


# C-V Characteristics : Gate Capacitance

- Approximate gate capacitance as terminating at the source, thus  $C_g = C_{gs}$ .
- $C_{gs} = \epsilon_{ox} WL / t_{ox} = C_{ox} WL = C_{permicron} W$
- $C_{permicron}$  is typically about 2 fF/ $\mu\text{m}$

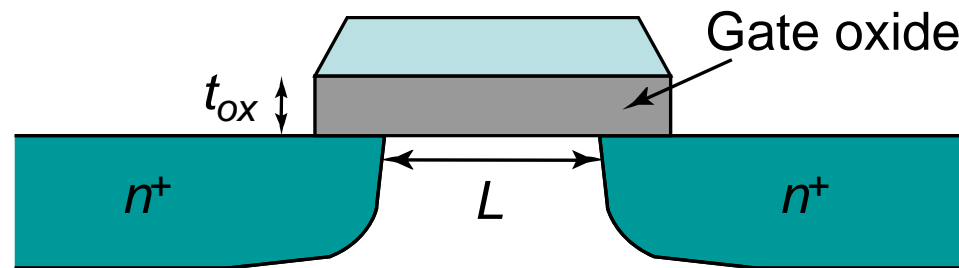


# C-V Characteristics : The Gate Capacitance

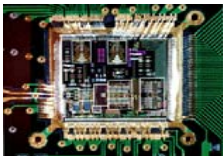


**Top view**

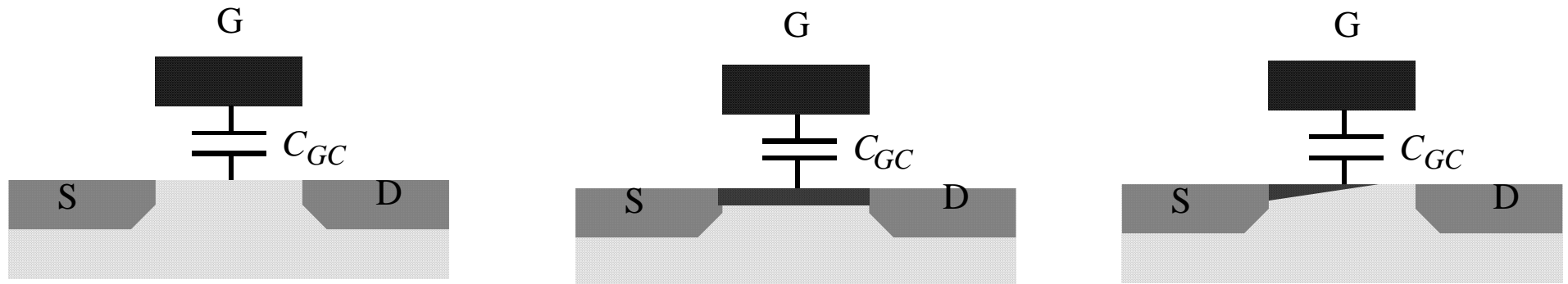
$$C_{gate} = \frac{\epsilon_{ox}}{t_{ox}} WL$$



**Cross section**



# C-V Characteristics : Gate Capacitance



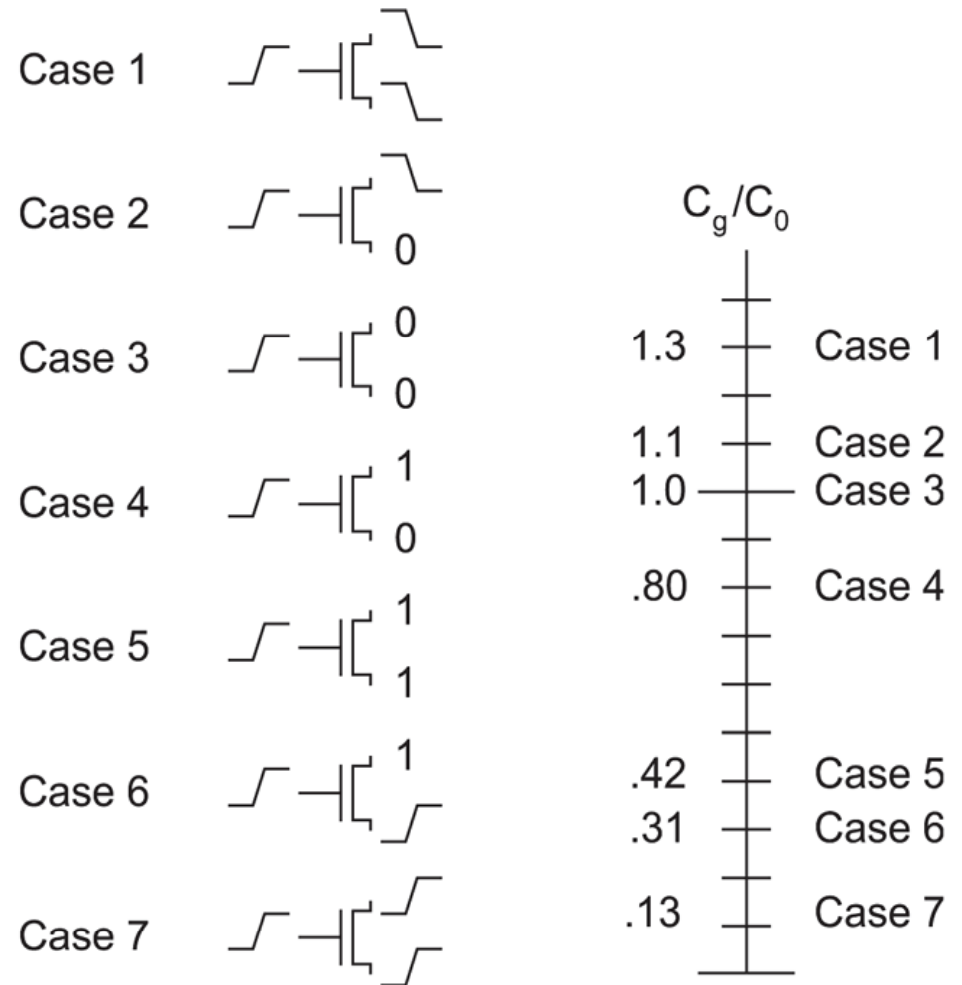
Operation Region	$C_{gb}$	$C_{gs}$	$C_{gd}$
Cutoff	$C_{ox}WL_{eff}$	0	0
Triode	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

Most important regions in digital design: saturation and cut-off



# C-V Characteristics : Gate Capacitance

- The effective gate capacitance varies with switching activity of the source and drain.
- The switching activity is dependent on the input data to the device.

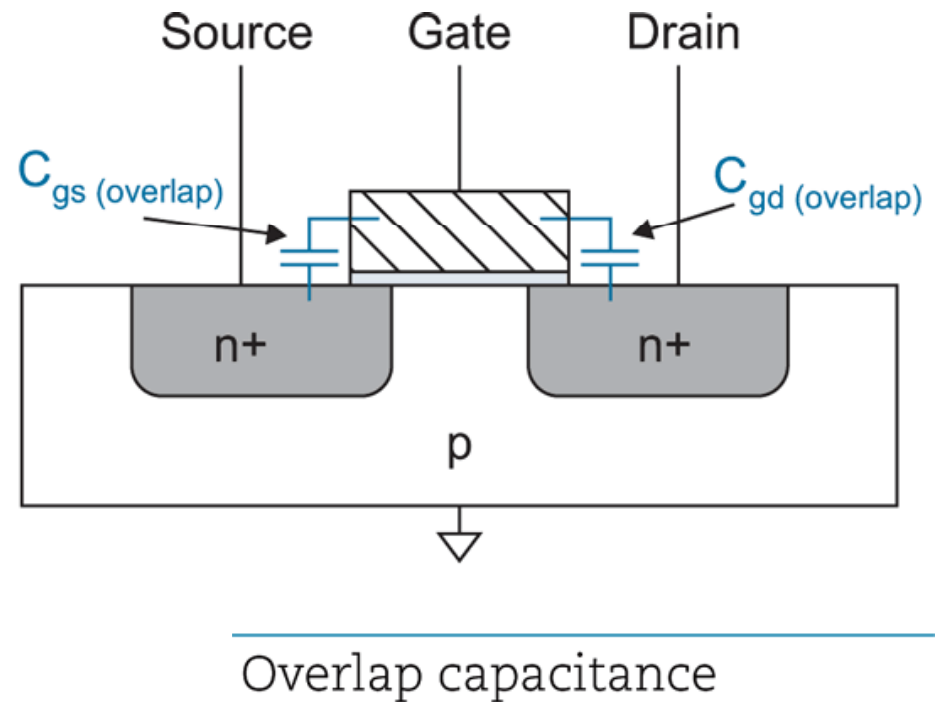


Data-dependent gate capacitance

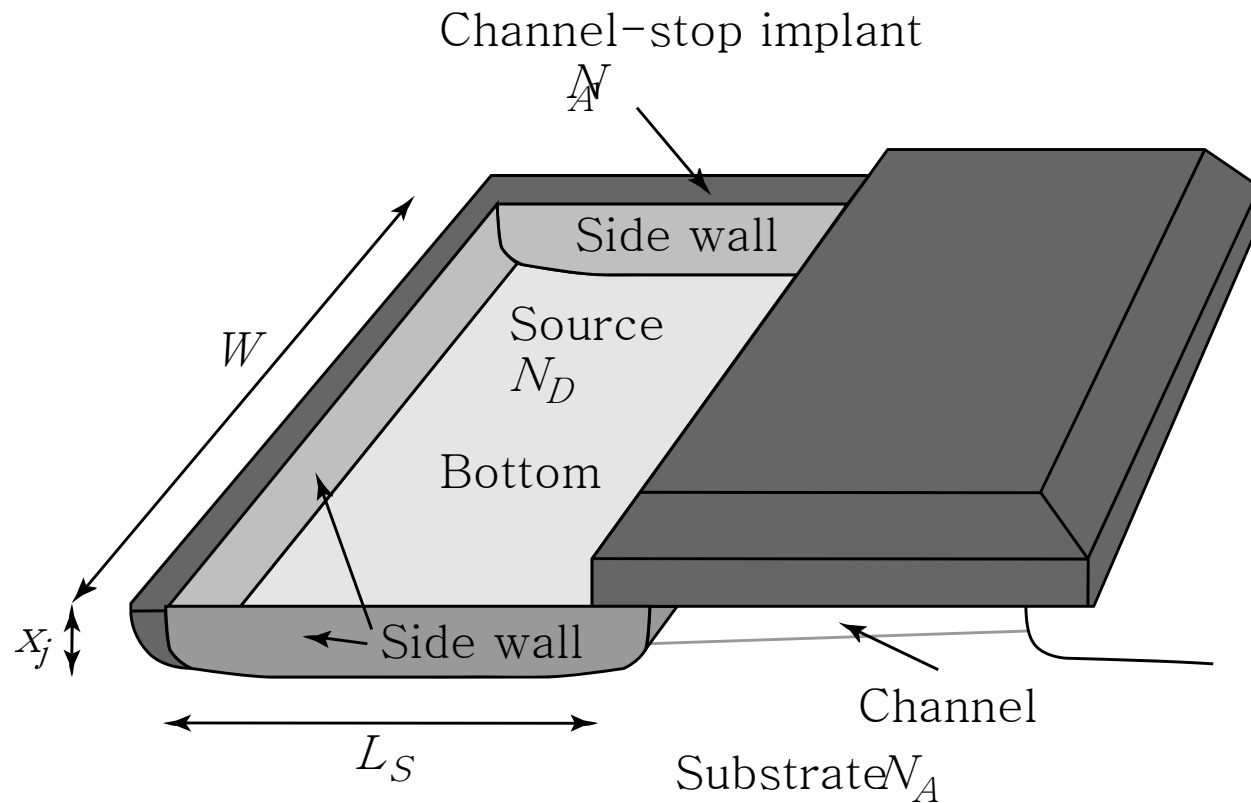


# C-V Characteristics : Overlap Capacitance

- Gate overlaps the source and drain by a small amount in real device.
- These capacitances are proportional to the width of the transistor.



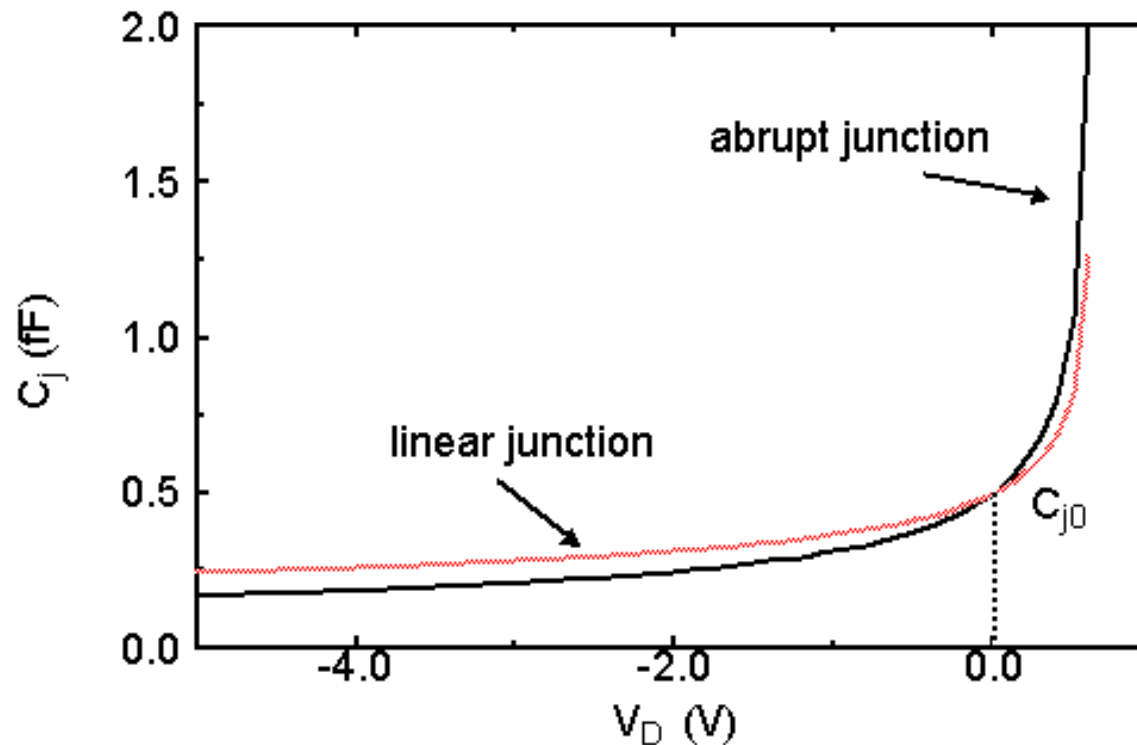
# C-V Characteristics : Diffusion Capacitance



$$\begin{aligned} C_{diff} &= C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER \\ &= C_j L_S W + C_{jsw} (2L_S + W) \end{aligned}$$

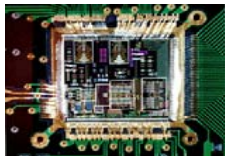


# C-V Characteristics : Junction Capacitance



$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

$m = 0.5$ : abrupt junction  
 $m = 0.33$ : linear junction



# C-V Characteristics :

## Linearizing the Junction Capacitance

Replace non-linear capacitance by large-signal equivalent linear capacitance which displaces equal charge over voltage swing of interest.

$$C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{high}) - Q_j(V_{low})}{V_{high} - V_{low}} = K_{eq} C_{j0}$$

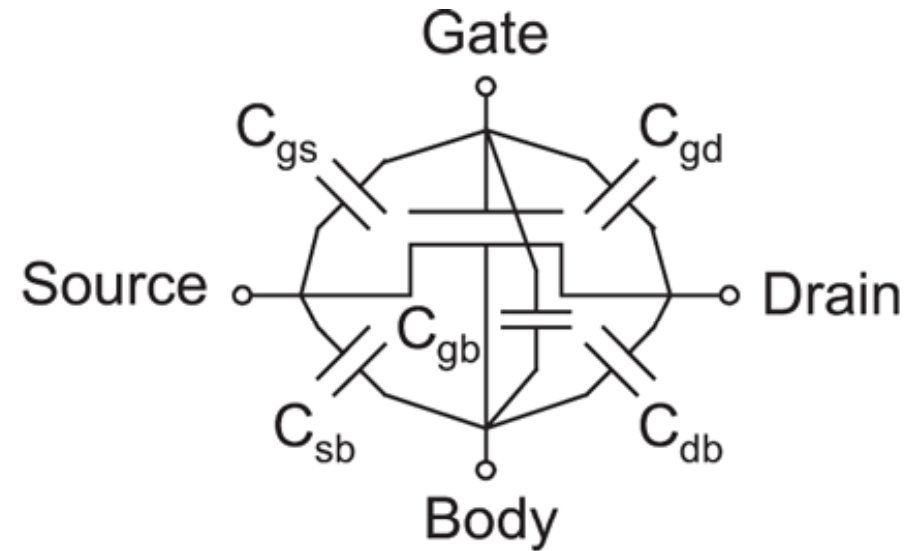
$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1 - m)} [(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$





# C-V Characteristics : Summary

- MOS is a four terminal device.
- Capacitance exists between each pair of terminals.
- Gate capacitance include both intrinsic and overlap components.
- The source and drain have parasitic diffusion capacitance to the body.



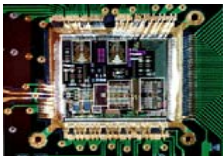
Capacitances of an MOS transistor

**NOTE:** Solve Example 3.10, page-112, Rabaey book.

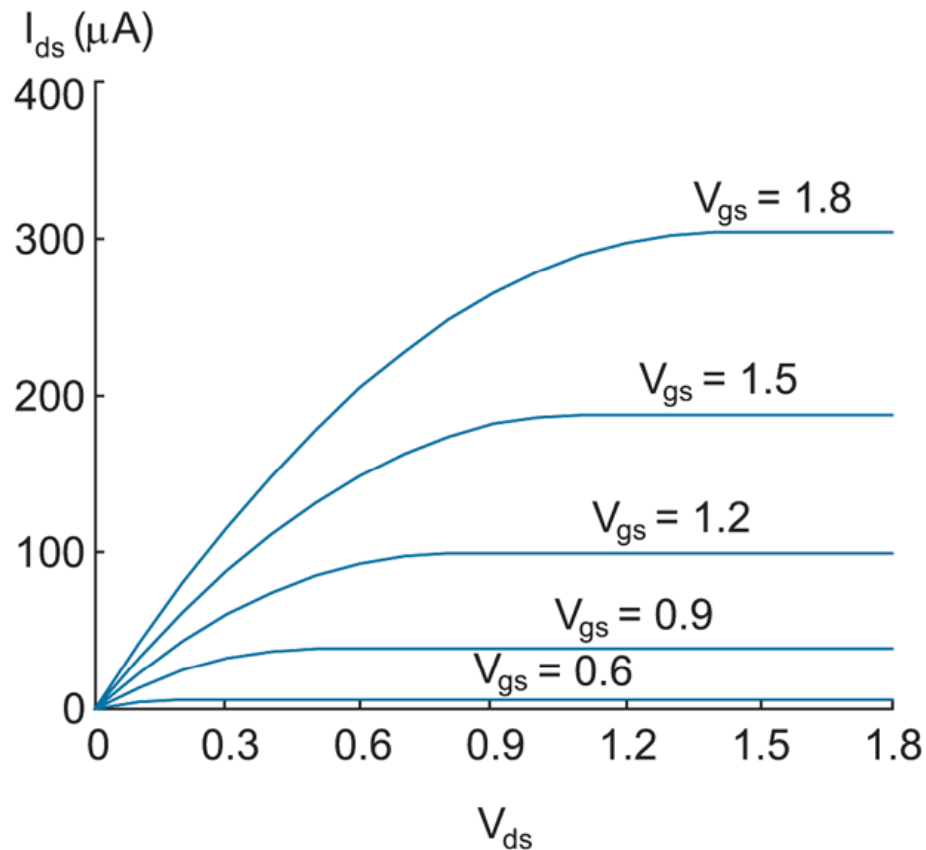


# Non-ideal I-V Effects

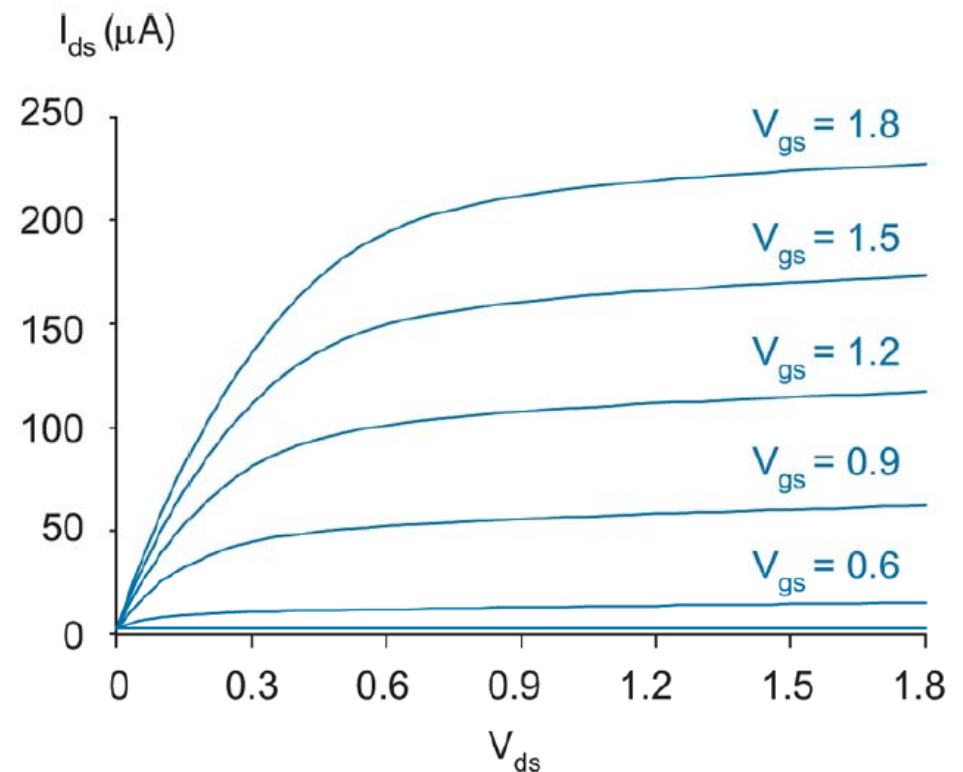
- Two effects make the saturation current increase less quadratically than expected:
  - Velocity saturation
  - Mobility degradation
- Few more effects that impact the characteristics of MOS are:
  - Channel length modulation
  - Body effect
  - Subthreshold conduction
  - Junction leakage
  - Gate leakage (tunneling)
  - Operating temperature
  - Device geometry



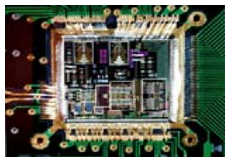
# Non-ideal I-V Effects : Vs Ideal



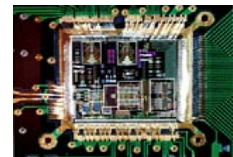
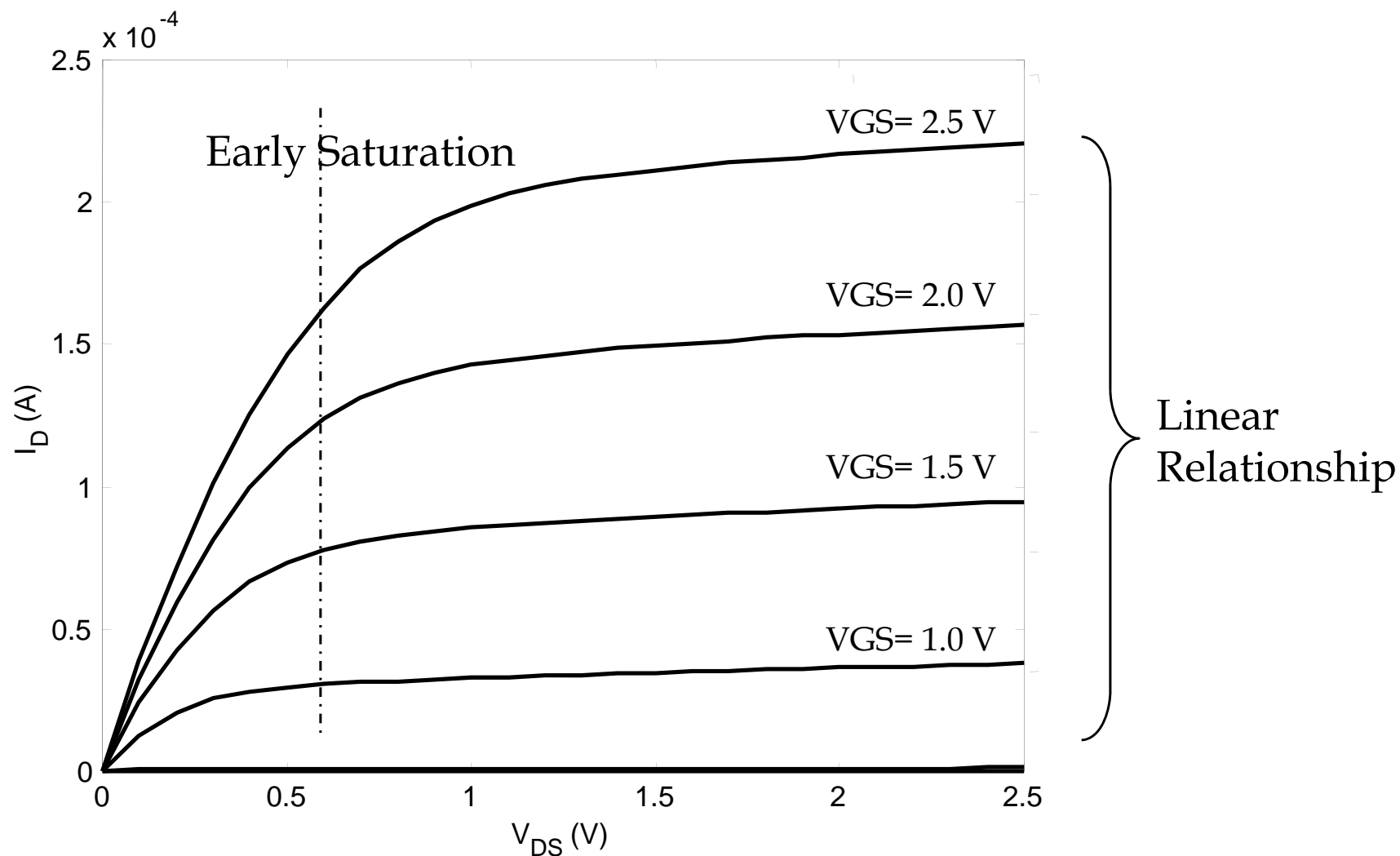
I-V Characteristic of Ideal NMOS



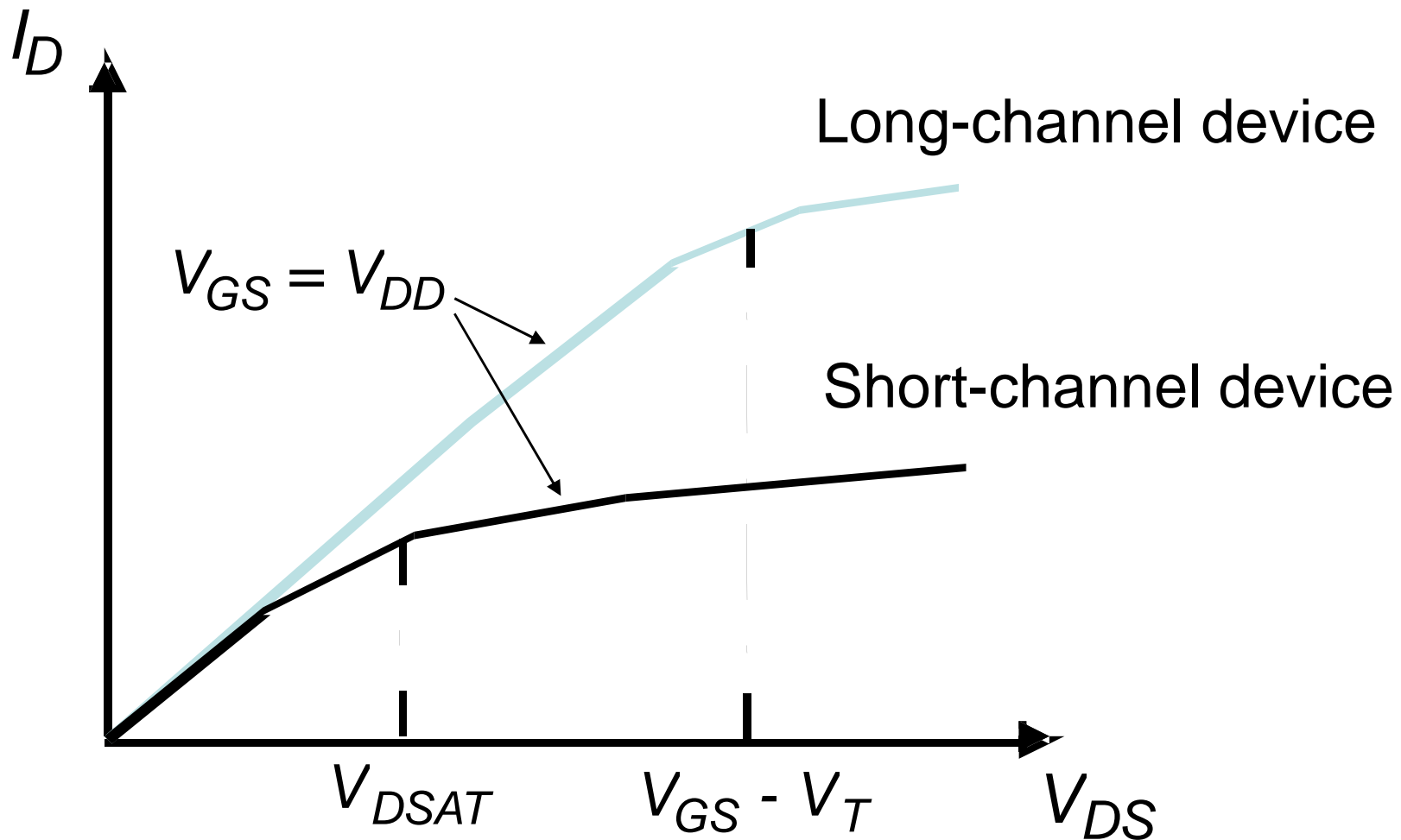
I-V Characteristic of Non-Ideal NMOS



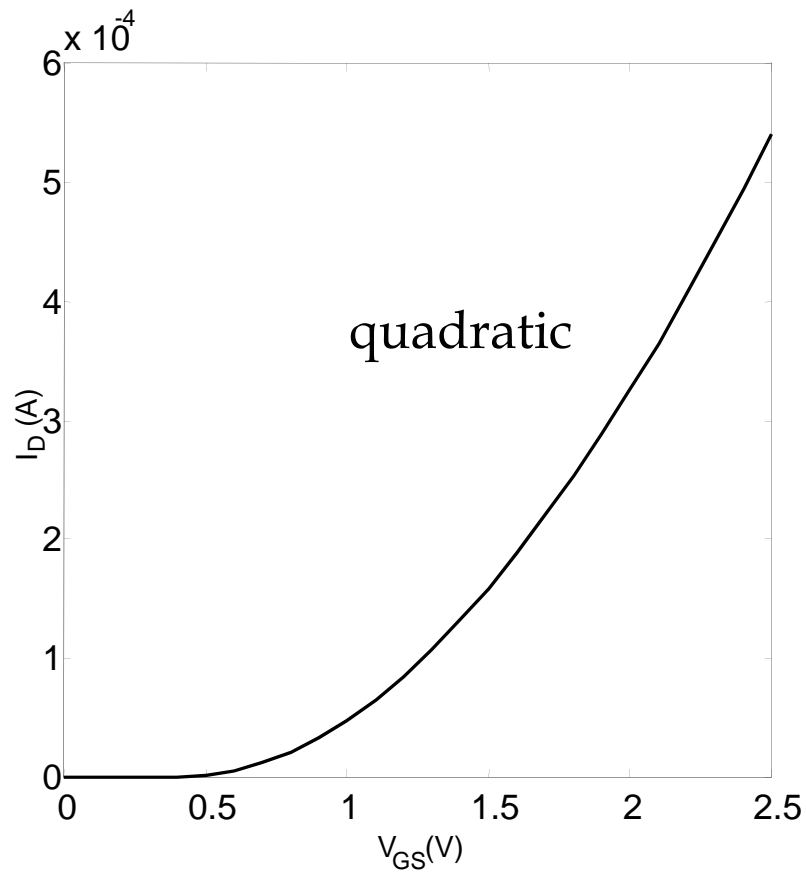
# Current-Voltage Relations: The Deep-Submicron Era



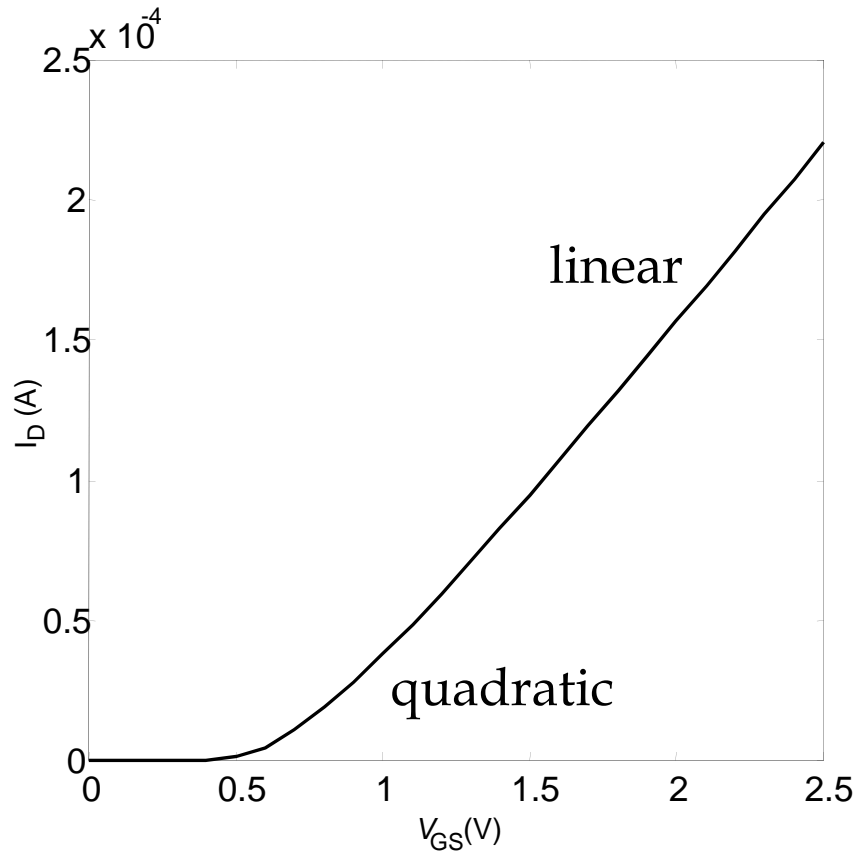
# Current-Voltage Relations: Perspective



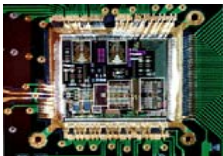
# $I_D$ versus $V_{GS}$



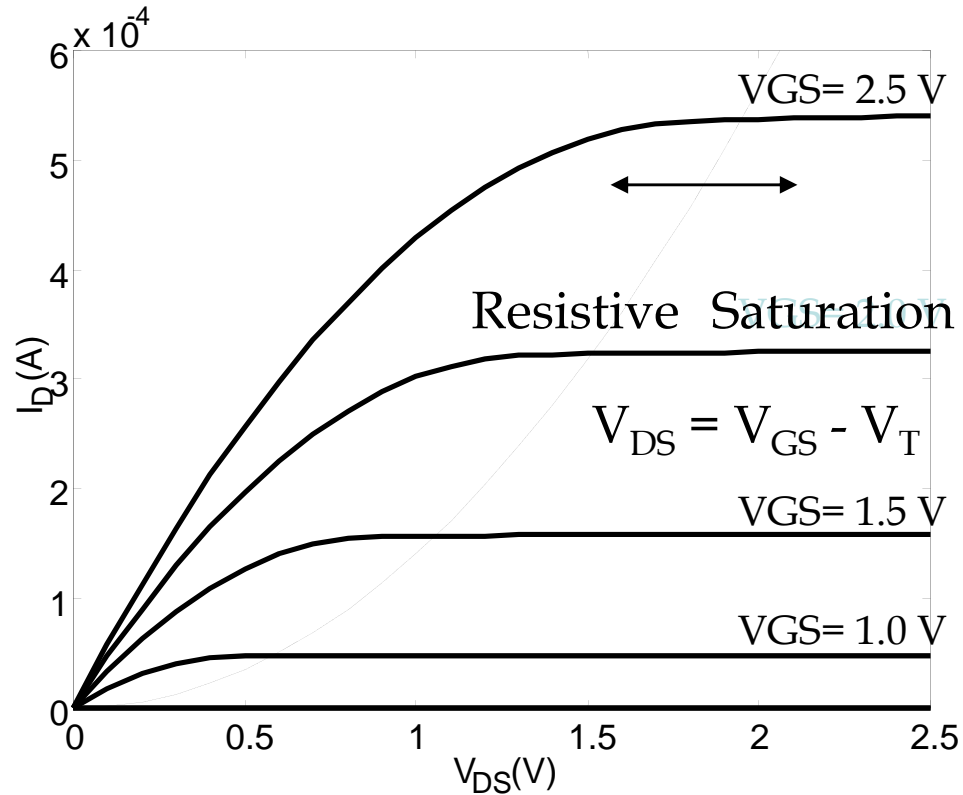
Long Channel



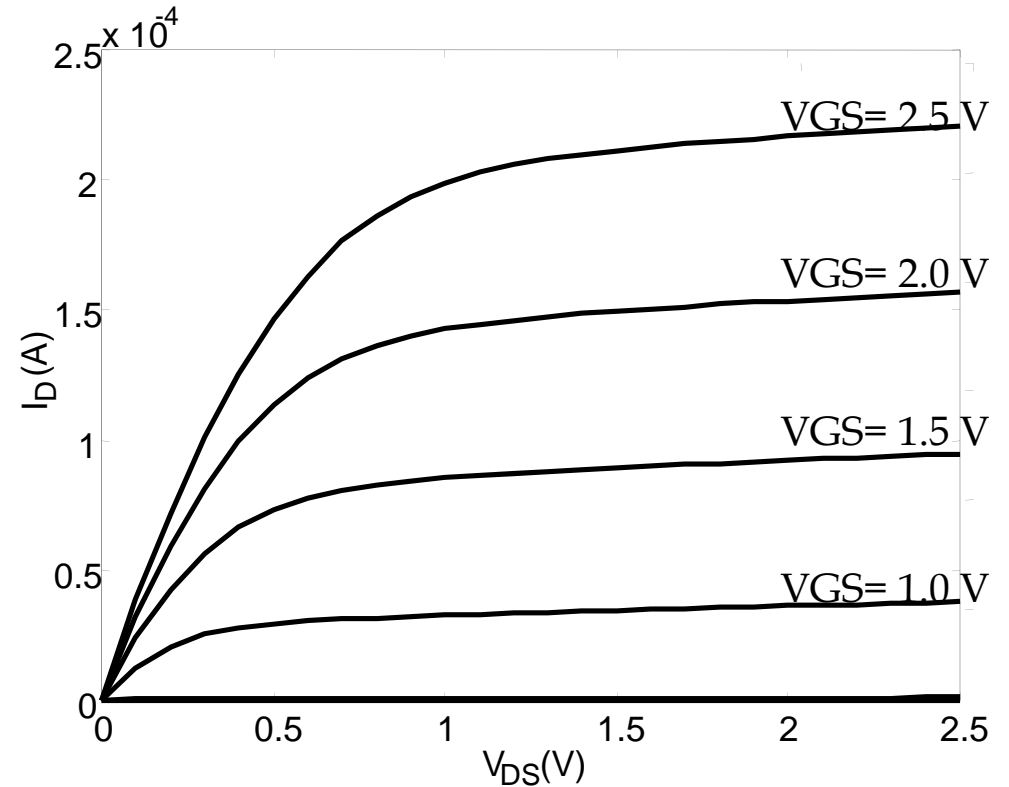
Short Channel



# $I_D$ versus $V_{DS}$



Long Channel

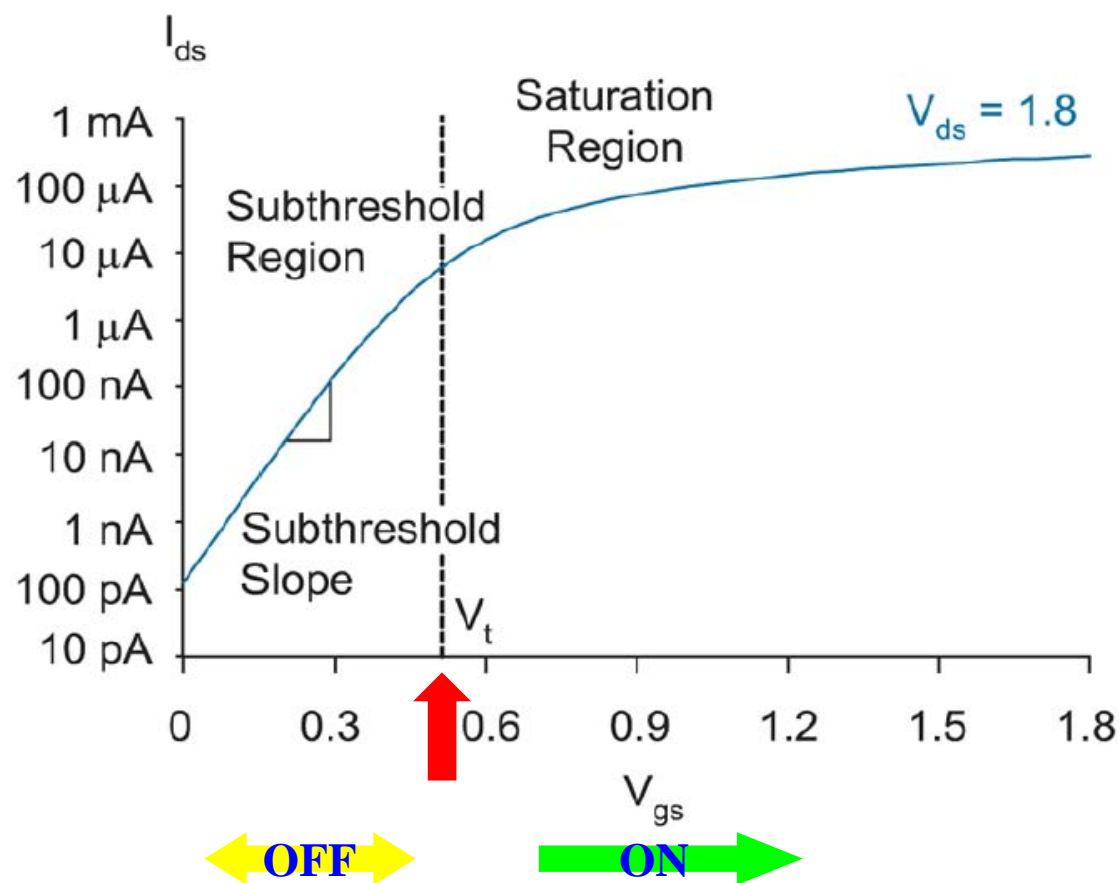


Short Channel



# Non-ideal I-V Effects : Study Region wise

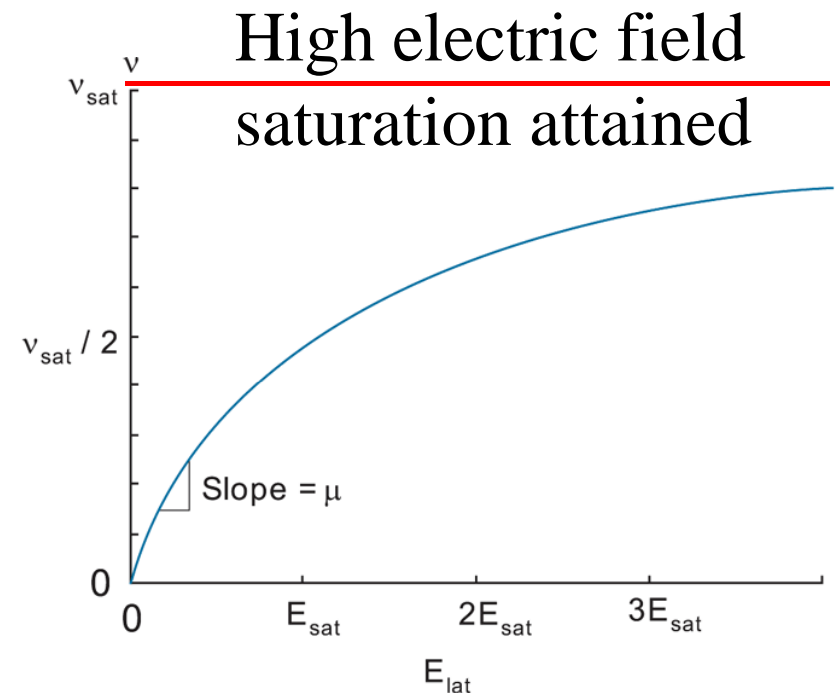
- In OFF state i.e. subthreshold region, there is some current flow, which has exponential variation.
- In ON State:
  - Linear Region: Linear variation
  - Saturation Region: Approximately quadratic variation





# Non-ideal I-V Effects : Velocity Saturation

- Two electric fields:
  - Lateral ( $V_{ds} / L$ )
  - Vertical ( $V_{gs} / t_{ox}$ )
- When lateral electric field is very high carrier velocity does not increase linearly with it.
- High vertical field also scatters the carriers.
- In turn reduces the carrier mobility; effect is called **mobility degradation**.

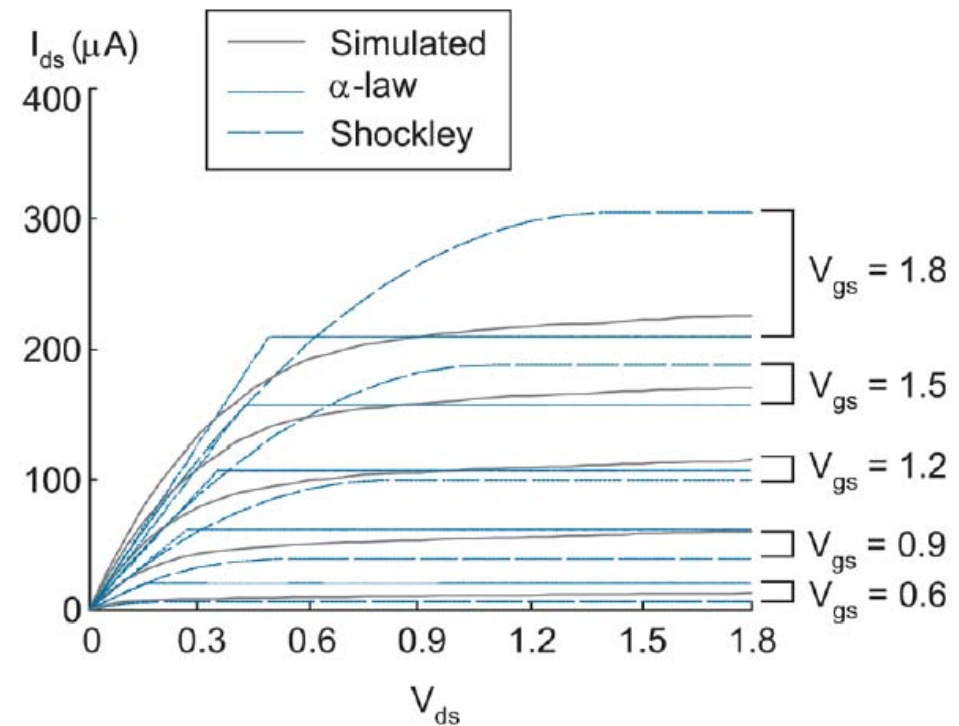


Carrier velocity vs. electric field



# Non-ideal I-V Effects : Velocity Saturation ...

- Carrier saturation velocity,  $v_{\text{sat}} = \mu E_{\text{sat}}$
- Typical Values:
  - For electron:  $6\text{-}10 \times 10^6 \text{ cm / s}$
  - For hole:  $4\text{-}8 \times 10^6 \text{ cm / s}$
- Alpha ( $\alpha$ ) – Power law model introduced a new parameter called velocity saturation index ( $\alpha$ ) to model it.



I-V characteristics for nMOS transistor with velocity saturation



# Non-ideal I-V Effects: Channel Length Modulation

- The reverse biased p-n junction between the drain and body form a depletion region.
- The length of depletion region  $L_d$  increases with the drain to body voltage  $V_{db}$ .
- The depletion region shortens the channel length,  $L_{eff} = L - L_d$ .
- It is very important for short channel transistors.



# Non-ideal I-V Effects : Body Effect

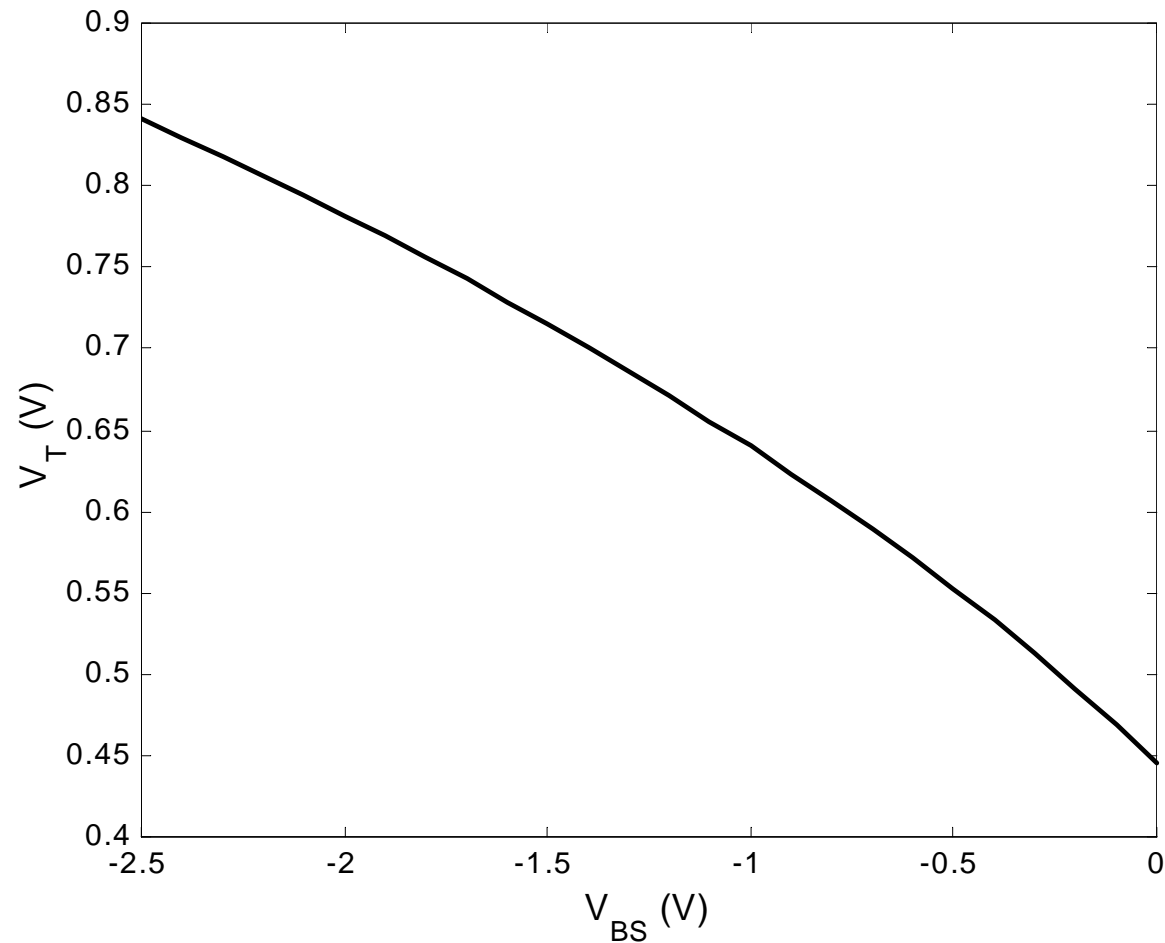
- The potential difference between source and body  $V_{sb}$  can affect the threshold voltage.
- It is modeled using surface potential and body effect coefficient, which in turn depend on the doping level.
- Sometimes intentionally body biased is used to decrease the subthreshold leakage.
- Results in increase in threshold as:

$$V_T = V_{T0} + \text{Change on } V_T$$

$$V_{th} = V_{FB} + \Phi_s + \gamma \sqrt{\Phi_s - V_{bs}} = V_{TH0} + \gamma (\sqrt{\Phi_s - V_{bs}} - \sqrt{\Phi_s})$$



# Non-ideal I-V Effects : The Body Effect



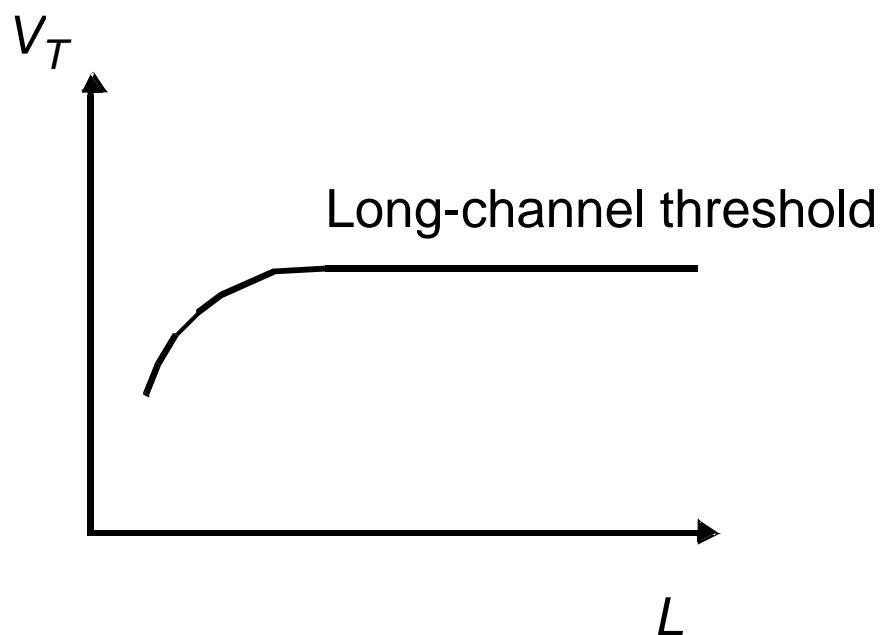
# Non-ideal I-V Effects : Subthreshold Conduction

- In OFF state, undesired leakage current flow.
- It contributes to power dissipation of idle circuits.
- Drain-Induced-Barrier-Lowering (DIBL) an prominent effect for short channel transistors also impacts subthreshold conduction by lowering  $V_T$ .
- This current increases as the  $V_T$  increases.
- It also increases as the temperature increases.
- If  $v_t$  is the thermal voltage and  $I_0$  is the current at  $V_T$  then the subthreshold current is :

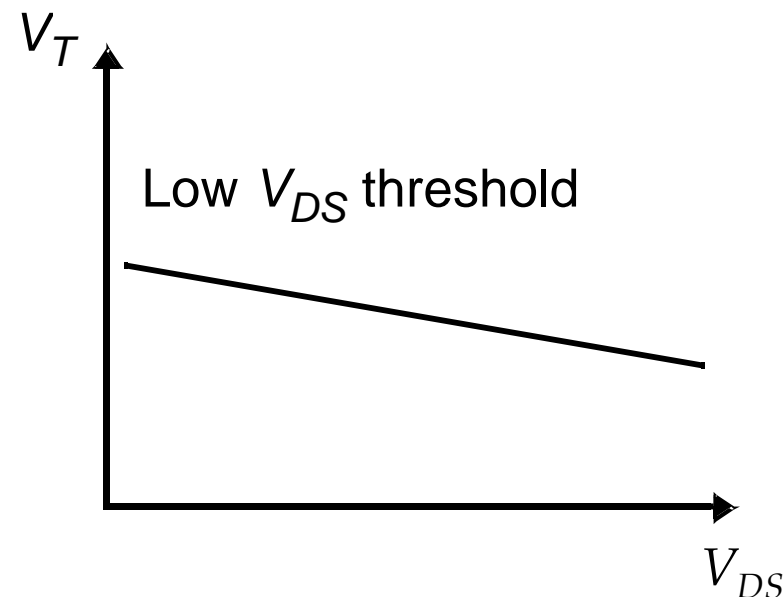
$$I_{ds} = I_0 \left[ 1 - \exp\left(-\frac{V_{ds}}{v_t}\right) \right] \cdot \exp\left(\frac{V_{gs} - V_{th} - V_{off}'}{nv_t}\right)$$



# Non-ideal I-V Effects : Subthreshold Conduction



Threshold as a function of the length (for low  $V_{DS}$ )

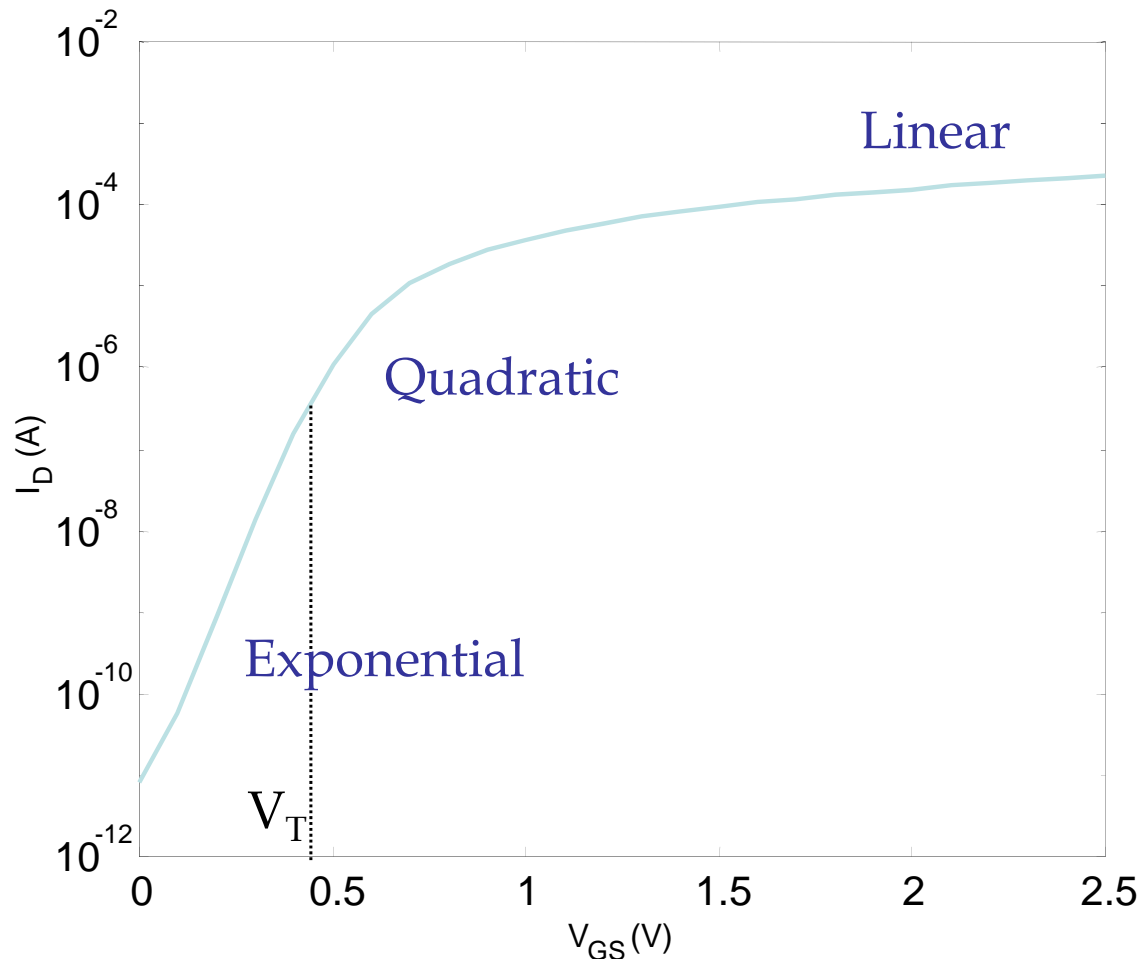


Drain-induced barrier lowering (for low  $L$ )

## Subthreshold Variations



# Non-ideal I-V Effects : Subthreshold Conduction



## The Slope Factor

$$I_D \sim I_0 e^{\frac{qV_{GS}}{nkT}}, \quad n = 1 + \frac{C_D}{C_{ox}}$$

$S$  is  $\Delta V_{GS}$  for  $I_{D2}/I_{D1} = 10$

$$S = n \left( \frac{kT}{q} \right) \ln(10)$$

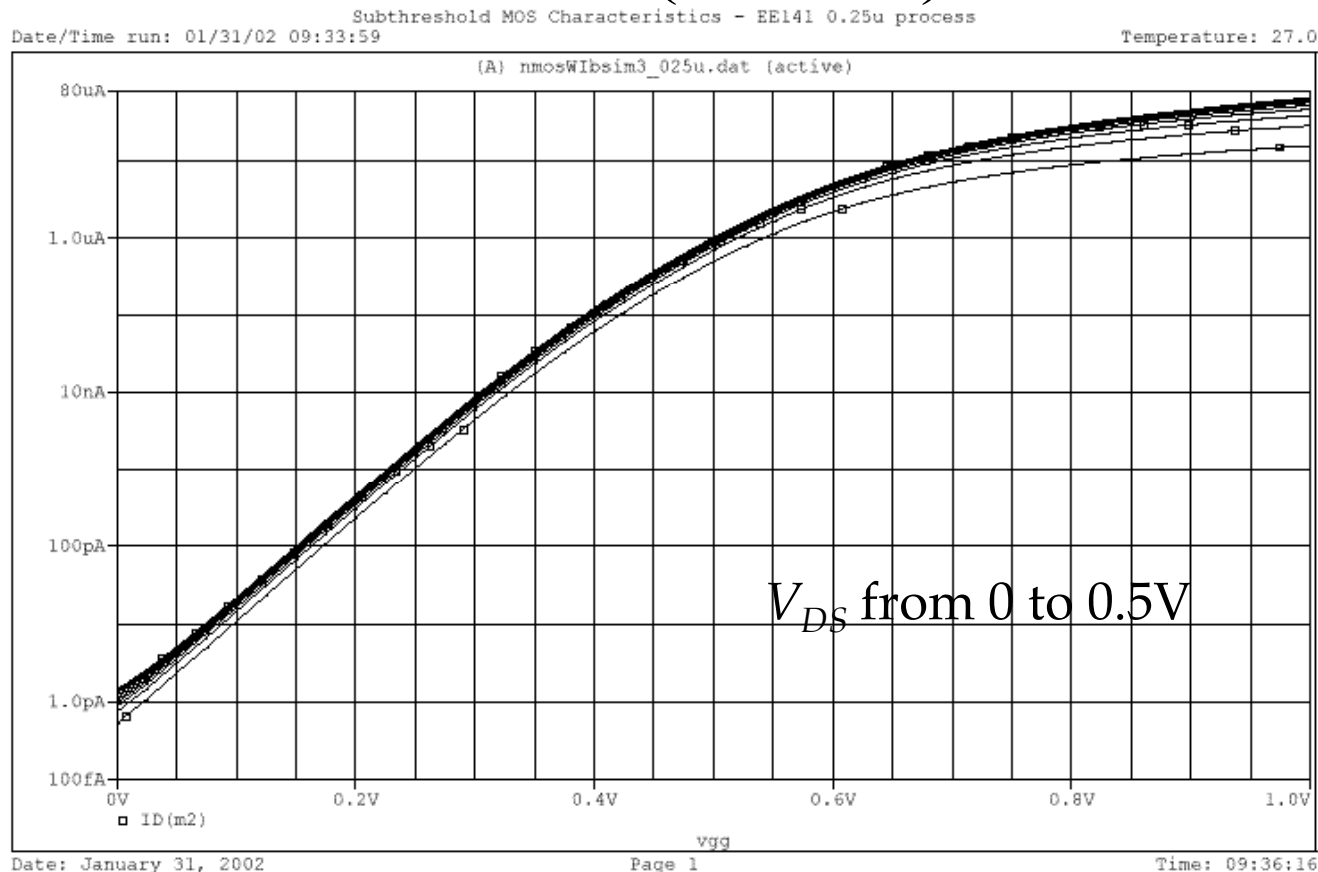
Typical values for  $S$ :  
60 .. 100 mV/decade





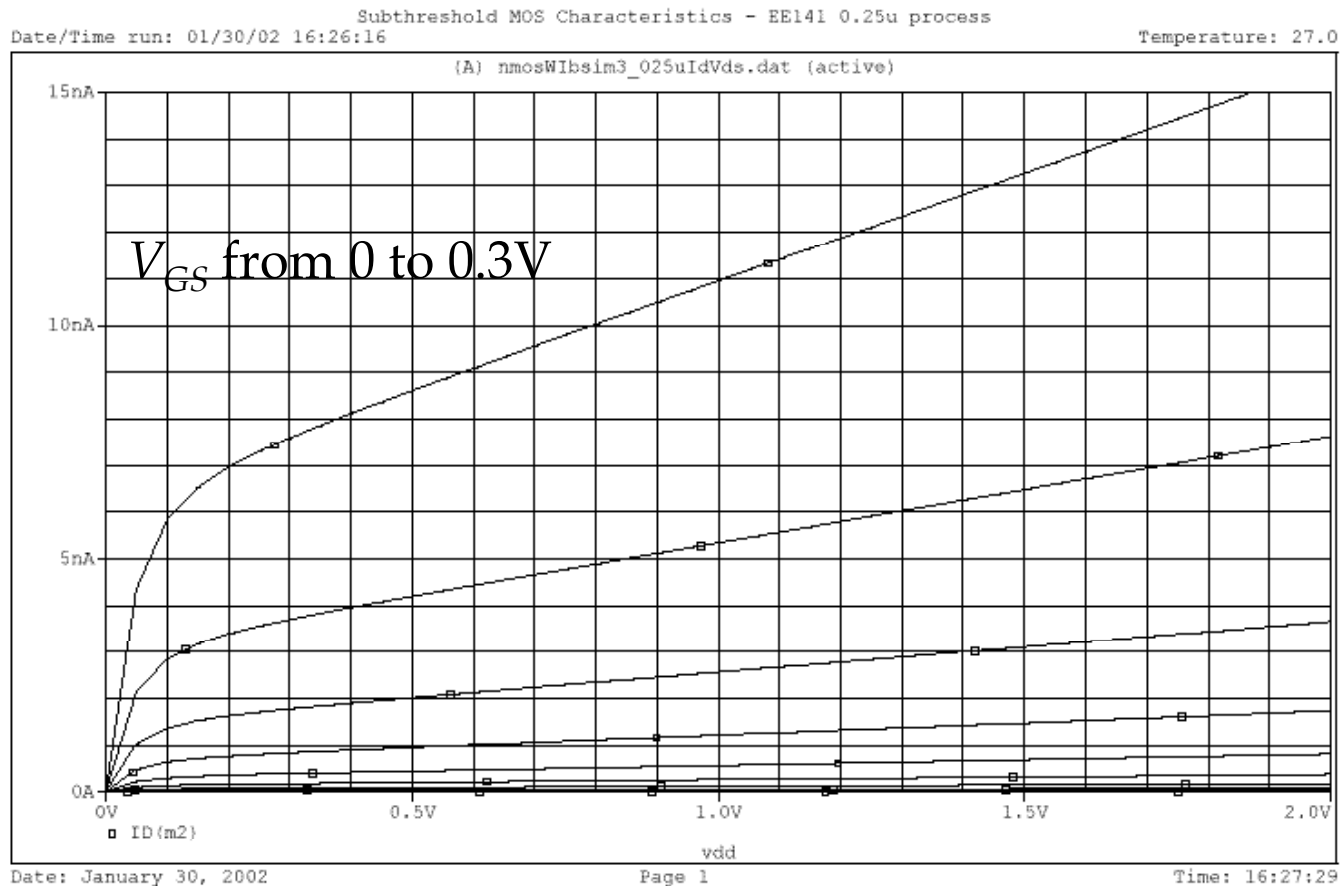
# Non-ideal I-V Effects : Subthreshold Conduction ( $I_D$ vs $V_{GS}$ )

$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left( 1 - e^{-\frac{qV_{DS}}{kT}} \right)$$



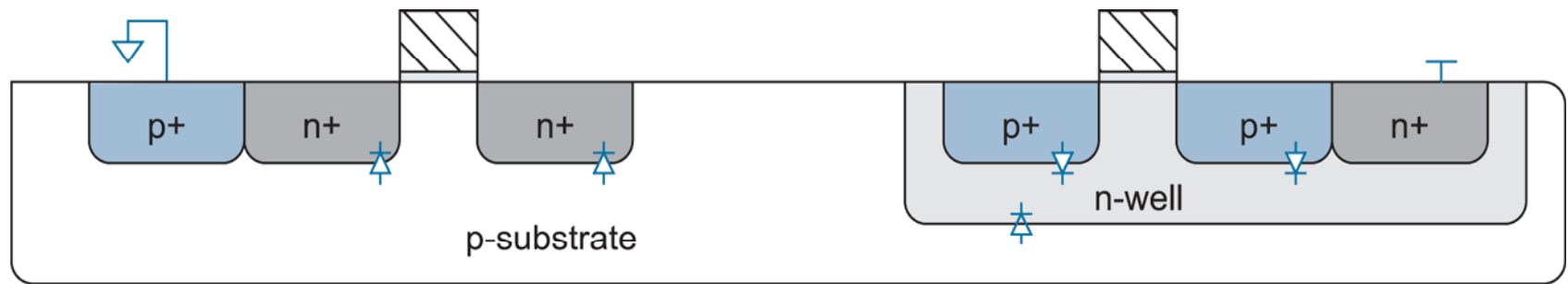
# Non-ideal I-V Effects : Subthreshold Conduction ( $I_D$ vs $V_{DS}$ )

$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left( 1 - e^{-\frac{qV_{DS}}{kT}} \right) (1 + \lambda \cdot V_{DS})$$

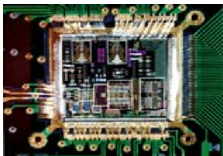


# Non-ideal I-V Effects : Junction Leakage

- The pn junctions between diffusion, substrate and well are all junction diodes.
- These are reversed biased as substrate is connected to GND and well connected to  $V_{dd}$ .
- However, reversed biased diode also conduct small amount of current.

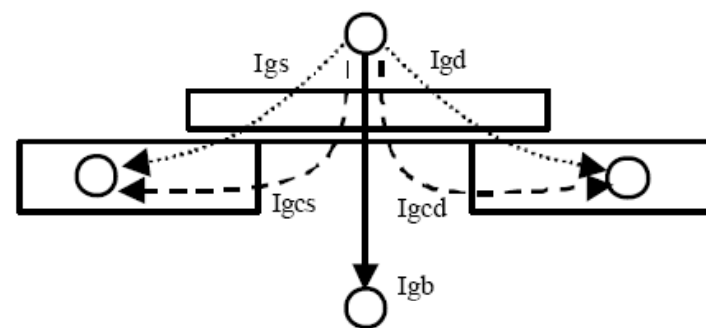


Reverse-biased diodes in CMOS circuits

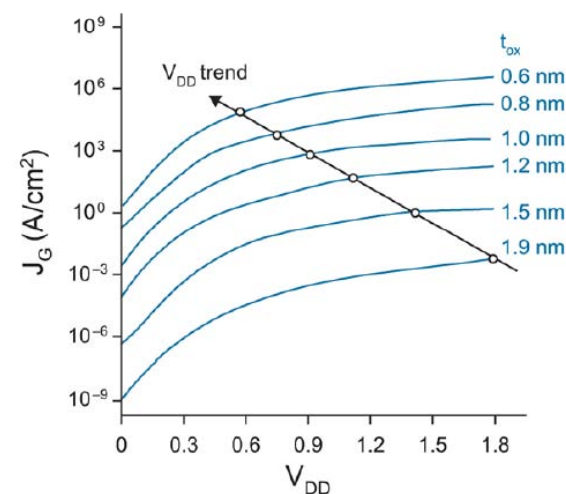


# Non-ideal I-V Effects : Tunneling

- There is a finite probability for carrier being pass through the gate oxide.
- This results in tunneling current thorough the gate oxide.
- The effect is predominate for lower oxide thickness.
- Substituting gate oxide with other dielectric with high-K is as an alternative.



Gate current components

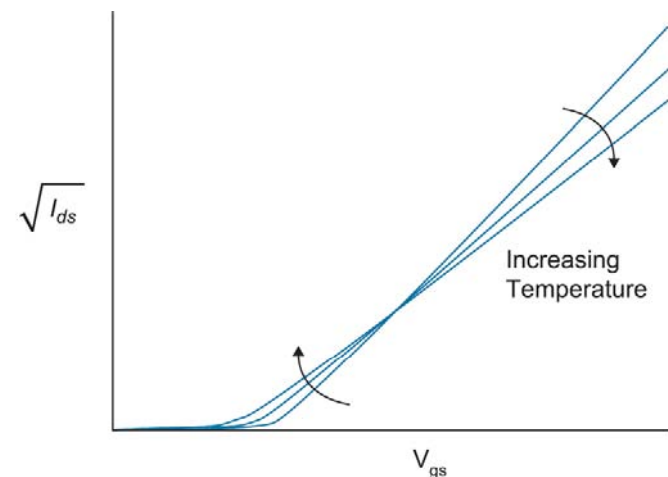


Gate leakage current from

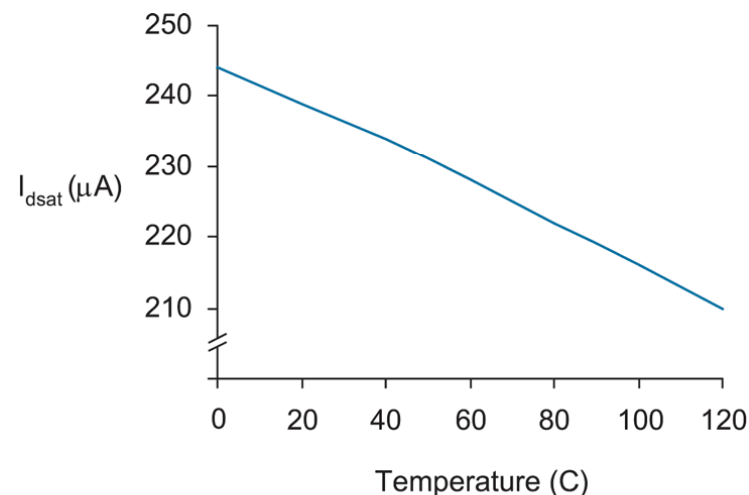


# Non-ideal I-V Effects : Temperature

- Carrier mobility decreases with temperature.
- The magnitude of threshold voltage is linear with the increase in temperature.
- The junction leakage increases with temperature.
- In summary: ON state current decreases and OFF state increases with temperature.
- Thus circuit performance is improved by cooling, hence heat sink, radiators, cooling fans !!



$\sqrt{I_{ds}}$  vs  $V_{gs}$  characteristics of nMOS transistor in saturation at various temperatures



$I_{dsat}$  vs. temperature



# Non-ideal I-V Effects : Geometry

- Width and length for each device should be appropriately chosen for current matching.
- The actual dimension of the device may differ due to several reasons:
  - Manufactures using mask of wrong dimension
  - More lateral diffusion of source and drain
- **NOTE:** Combination of threshold, effective channel length, channel length modulation, etc reduces the current carrying capacity by half.

